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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, UART/USART
Peripherals	LVR, POR, PWM, WDT
Number of I/O	46
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3234bv-24u6

2.2.4 Program counter

The Program Counter is a 16-bit wide which consists of two 8-bit registers, PCH and PCL. This counter indicates the address of the next instruction to be executed. In $\overline{\text{RESET}}$ state, the program counter has reset routine address (PCH:00h, PCL:00h).

2.2.5 Program status word

The Program Status Word (PSW) contains several bits that reflect the current state of the CPU and select Internal RAM (00h to 1Fh: Bank0 to Bank3). The PSW is described in *Figure 8*. It contains the Carry flag, the Auxiliary Carry flag, the Half Carry (for BCD operation), the General Purpose flag, the Register Bank Select flags, the Overflow flag, and Parity flag.

[Carry flag, CY]. This flag stores any carry or not borrow from the ALU of CPU after an arithmetic operation and is also changed by the Shift Instruction or Rotate Instruction.

[Auxiliary Carry flag, AC]. After operation, this flag is set when there is a carry from Bit 3 of ALU or there is no borrow from Bit 4 of ALU.

[Register Bank Select flags, RS0, RS1]. These flags select one of four banks (00~07H:bank0, 08~0Fh:bank1, 10~17h:bank2, 17~1Fh:bank3) in Internal RAM.

[Overflow flag, OV]. This flag is set to '1' when an overflow occurs as the result of an arithmetic operation involving signs. An overflow occurs when the result of an addition or subtraction exceeds +127 (7Fh) or -128 (80h). The CLRV instruction clears the overflow flag. There is no set instruction. When the BIT instruction is executed, Bit 6 of memory is copied to this flag.

[Parity flag, P]. This flag reflects the number of Accumulator's 1. If the number of Accumulator's 1 is odd, P=0; otherwise, P=1. The sum when adding Accumulator's 1 to P is always even.

2.2.6 Registers R0~R7

General purpose 8-bit registers that are locked in the lower portion of internal data area.

2.2.7 Data pointer register

Data Pointer Register is 16-bit wide which consists of two-8bit registers, DPH and DPL. This register is used as a data pointer for the data transmission with external data memory in the PSD module.

Figure 8. PSW (Program Status Word) register

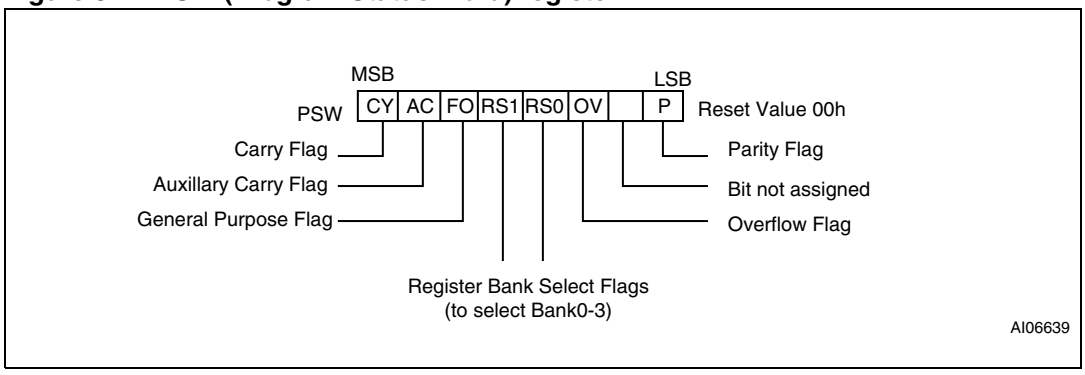


Table 3. RAM address (continued)

Byte address (in hexadecimal)									Byte address (in decimal)
-									-
22h	17	16	15	14	13	12	11	10	34
21h	0F	0E	0D	0C	0B	0A	09	08	33
20h	07	06	05	04	03	02	01	00	32
1Fh	Register bank 3								31
18h									24
17h	Register bank 2								23
10h									16
0Fh	Register bank 1								15
08h									8
07h	Register bank 0								7
00h									0

2.9 Addressing modes

The addressing modes in UPSD323xx devices instruction set are as follows

1. Direct addressing
2. Indirect addressing
3. Register addressing
4. Register-specific addressing
5. Immediate constants addressing
6. Indexed addressing

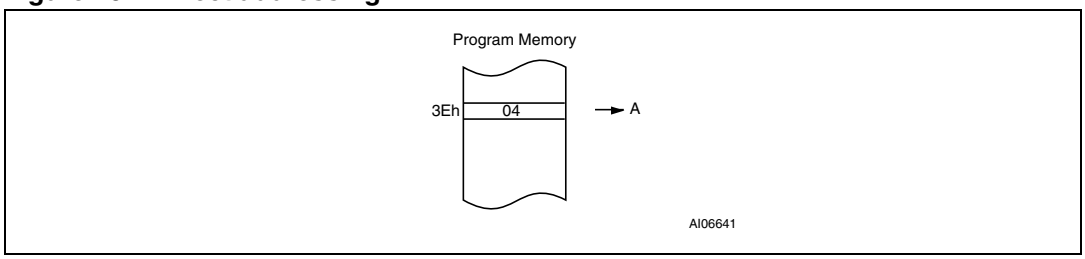
2.9.1 Direct addressing

In a direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs (80~FFH RAM) can be directly addressed.

Example:

mov A, 3EH ; A <----- RAM[3E]

Figure 10. Direct addressing



Note: In UPSD323xx devices, the stack resides in on-chip RAM, and grows upwards. The PUSH instruction first increments the Stack Pointer (SP), then copies the byte into the stack. PUSH and POP use only direct addressing to identify the byte being saved or restored, but the stack itself is accessed by indirect addressing using the SP register. This means the stack can go into the Upper 128 bytes of RAM, if they are implemented, but not into SFR space.

The Data Transfer instructions include a 16-bit MOV that can be used to initialize the Data Pointer (DPTR) for look-up tables in Program Memory.

The XCH A, <byte> instruction causes the Accumulator and ad-dressed byte to exchange data. The XCHD A, @Ri instruction is similar, but only the low nibbles are involved in the exchange. To see how XCH and XCHD can be used to facilitate data manipulations, consider first the problem of shifting and 8-digit BCD number two digits to the right. *Table 8* shows how this can be done using XCH instructions. To aid in understanding how the code works, the contents of the registers that are holding the BCD number and the content of the Accumulator are shown alongside each instruction to indicate their status after the instruction has been executed.

After the routine has been executed, the Accumulator contains the two digits that were shifted out on the right. Doing the routine with direct MOVs uses 14 code bytes. The same operation with XCHs uses only 9 bytes and executes almost twice as fast. To right-shift by an odd number of digits, a one-digit must be executed. *Table 9* shows a sample of code that will right-shift a BCD number one digit, using the XCHD instruction. Again, the contents of the registers holding the number and of the accumulator are shown alongside each instruction.

Table 6. Data transfer instructions that access internal data memory space

Mnemonic	Operation	Addressing modes			
		Dir.	Ind.	Reg.	Imm.
MOV A,<src>	A = <src>	X	X	X	X
MOV <dest>,A	<dest> = A	X	X	X	
MOV <dest>,<src>	<dest> = <src>	X	X	X	X
MOV DPTR,#data16	DPTR = 16-bit immediate constant				X
PUSH <src>	INC SP; MOV “@SP”,<src>	X			
POP <dest>	MOV <dest>,”@SP”; DEC SP	X			
XCH A,<byte>	Exchange contents of A and <byte>	X	X	X	
XCHD A,@Ri	Exchange low nibbles of A and @Ri		X		

First, pointers R1 and R0 are set up to point to the two bytes containing the last four BCD digits. Then a loop is executed which leaves the last byte, location 2EH, holding the last two digits of the shifted number. The pointers are decremented, and the loop is repeated for location 2DH. The CJNE instruction (Compare and Jump if Not equal) is a loop control that will be described later. The loop executed from LOOP to CJNE for R1 = 2EH, 2DH, 2CH, and 2BH. At that point the digit that was originally shifted out on the right has propagated to location 2AH. Since that location should be left with 0s, the lost digit is moved to the Accumulator.

Table 15. SFR memory map (continued)

88	TCON(1)	TMOD	TL0	TL1	TH0	TH1			8F
80	P0(1)	SP	DPL	DPH				PCON	87

1. Register can be bit addressing

Table 16. List of all SFRs

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
80	P0									FF	Port 0
81	SP									07	Stack Ptr
82	DPL									00	Data Ptr Low
83	DPH									00	Data Ptr High
87	PCON	SMOD	SMOD1	LVREN	ADSFINT	RCLK1	TCLK1	PD	IDLE	00	Power Ctrl
88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	Timer / Cntr Control
89	TMOD	Gate	C/T	M1	M0	Gate	C/T	M1	M0	00	Timer / Cntr mode Control
8A	TL0									00	Timer 0 Low
8B	TL1									00	Timer 1 Low
8C	TH0									00	Timer 0 High
8D	TH1									00	Timer 1 High
90	P1									FF	Port 1
91	P1SFS	P1S7	P1S6	P1S5	P1S4					00	Port 1 Select Register
93	P3SFS	P3S7	P3S6							00	Port 3 Select Register
94	P4SFS	P4S7	P4S6	P4S5	P4S4	P4S3	P4S2	P4S1	P4S0	00	Port 4 Select Register
95	ASCL									00	8-bit Prescaler for ADC clock
96	ADAT	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2	ADAT1	ADAT0	00	ADC Data Register
97	ACON			ADEN		ADS1	ADS0	ADST	ADSF	00	ADC Control Register
98	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00	Serial Control Register
99	SBUF									00	Serial Buffer
9A	SCON2	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00	2nd UART Ctrl Register
9B	SBUF2									00	2nd UART Serial Buffer
A0	P2									FF	Port 2

Table 17. PSD module register address offset (continued)

CSIOP addr offset	Register name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
C0	Primary Flash Protection	Sec7_ Prot	Sec6_ Prot	Sec5_ Prot	Sec4_ Prot	Sec3_ Prot	Sec2_ Prot	Sec1_ Prot	Sec0_ Prot		Bit = 1 sector is protected
C2	Secondary Flash Protection	Security _Bit	*	*	*	Sec3_ Prot	Sec2_ Prot	Sec1_ Prot	Sec0_ Prot		Security Bit = 1 device is secured
B0	PMMR0	*	*	PLD Mcells clk	PLD array-clk	PLD Turbo	*	APD enable	*	00	Control PLD power consumption
B4	PMMR2	*		PLD array Ale	PLD array Cntl2	PLD array Cntl1	PLD array Cntl0	*	*	00	Blocking inputs to PLD array
E0	Page									00	Page Register
E2	VM	Periph-mode	*	*	FL_ data	Boot_ data	FL_ code	Boot_ code	SR_ code		Configure 8032 Program and Data Space

1. (Register address = CSIOP address + address offset; where CSIOP address is defined by user in PSDsoft)
* indicates bit is not used and must be set to '0'.

6 Power-saving mode

Two software selectable modes of reduced power consumption are implemented.

6.1 Idle mode

In Idle mode, the following functions are switched Off.

- CPU (Halted)

The following functions remain Active during Idle mode:

- External Interrupts
- Timer 0, Timer 1, Timer 2
- DDC Interface
- PWM Units
- USB Interface
- USART
- 8-bit ADC
- I^2C Interface

Note: Interrupt or $\overline{RESET}$ terminates the Idle mode.

6.2 Power-down mode

- System Clock Halted
- LVD Logic Remains Active
- SRAM content remains unchanged
- The SFRs retain their value until a $\overline{RESET}$ is asserted

Note: The only way to exit Power-down mode is through a $\overline{RESET}$.

Table 25. Power-saving mode power consumption

Mode	Addr/data	Ports 1,3,4	PWM	I^2C	DDC	USB
Idle	Maintain Data	Maintain Data	Active	Active	Active	Active
Power-down	Maintain Data	Maintain Data	Disable	Disable	Disable	Disable

6.3 Power control register

The Idle and Power-down modes are activated by software via the PCON register.

Table 26. Pin status during Idle and Power-down mode

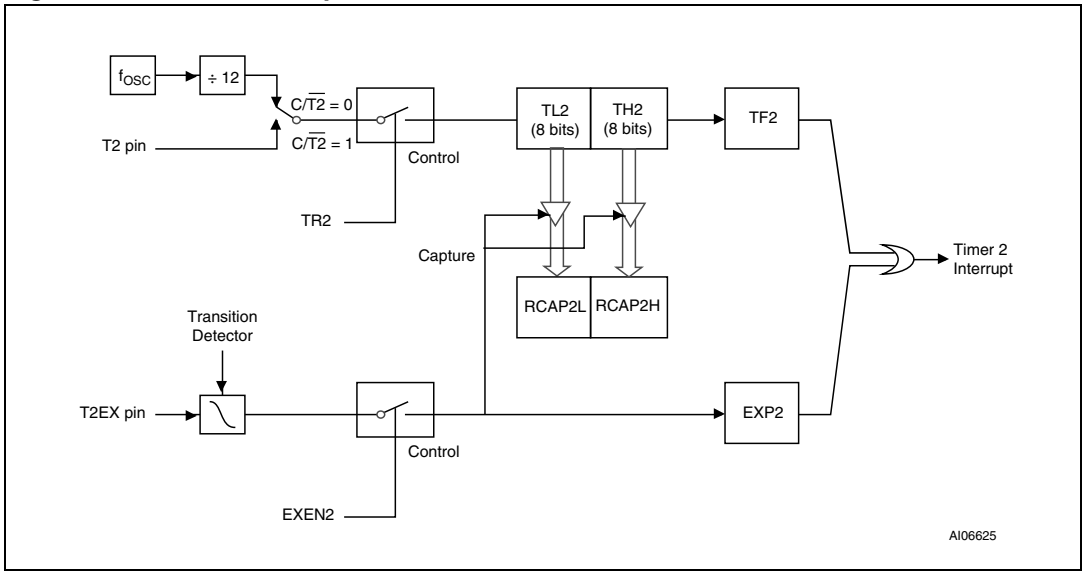
SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
87	PCON	SMOD	SMOD1	LVREN	ADSFINT	RCLK1	TCLK1	PD	IDLE	00	Power Ctrl

Table 42. Timer/counter2 operating modes

Mode	T2CON			T2MOD DECN	T2CON EXEN	P1.1 T2EX	Remarks	Input clock	
	RxCLK or TxCLK	CP/$\overline{RL2}$	TR2					Internal	External (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	x	Reload upon overflow	$f_{OSC}/12$	MAX $f_{OSC}/24$
	0	0	1	0	1	-	Reload trigger (falling edge)		
	0	0	1	1	x	0	Down counting		
	0	0	1	1	x	1	Up counting		
16-bit Capture	0	1	1	x	0	x	16-bit Timer/Counter (only up counting)	$f_{OSC}/12$	MAX $f_{OSC}/24$
	0	1	1	x	1	-	Capture (TH1,TL2) → (RCAP2H,RCAP2L)		
Baud Rate Generator	1	x	1	x	0	x	No overflow interrupt request (TF2)	$f_{OSC}/12$	MAX $f_{OSC}/24$
	1	x	1	x	1	-	Extra External Interrupt (Timer 2)		
Off	x	x	0	x	x	x	Timer 2 stops	—	—

1. ↓ = falling edge

Figure 24. Timer 2 in Capture mode



12 Standard serial interface (UART)

The UPSD323xx devices provides two standard 8032 UART serial ports. The first port is connected to pin P3.0 (RX) and P3.1 (TX). The second port is connected to pin P1.2 (RX) and P1.3(TX). The operation of the two serial ports are the same and are controlled by the SCON and SCON2 registers.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF (or SBUF2 for the second serial port). Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes: Mode 0, 1, 2 or 3.

Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the f_{OSC}.

Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a Start bit (0), 8 data bits (LSB first), and a Stop bit (1). On receive, the Stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2

11 bits are transmitted (through TxD) or received (through RxD): Start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a Stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the Parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the Stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a Start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a Stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

12.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a Stop bit. The port can be programmed such that when the Stop bit is received, the serial port interrupt will

be activated only if RB8 = 1. This feature is enabled by setting Bit SM2 in SCON. A way to use this feature in multi-processor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is '1' in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An ad-dress byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the Stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid Stop bit is received.

12.2 Serial port control register

The serial port control and status register is the Special Function Register SCON (SCON2 for the second port), shown in *Figure 26*. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the Serial Port Interrupt bits (TI and RI).

Table 43. Serial port control register (SCON)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 44. Description of the SCON bits

Bit	Symbol	Function
7	SM0	(SM1,SM0)=(0,0): Shift Register. Baud rate = $f_{OSC}/12$ (SM1,SM0)=(1,0): 8-bit UART. Baud rate = variable (SM1,SM0)=(0,1): 8-bit UART. Baud rate = $f_{OSC}/64$ or $f_{OSC}/32$ (SM1,SM0)=(1,1): 8-bit UART. Baud rate = variable
6	SM1	
5	SM2	Enables the multiprocessor communication features in Mode 2 and 3. In Mode 2 or 3, if SM2 is set to '1,' RI will not be activated if its received 8th data bit (RB8) is '0.' In Mode 1, if SM2=1, RI will not be activated if a valid Stop bit was not received. In Mode 0, SM2 should be '0'
4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception
3	TB8	The 8th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired
2	RB8	In Modes 2 and 3, this bit contains the 8th data bit that was received. In Mode 1, if SM2=0, RB8 is the Snap Bit that was received. In Mode 0, RB8 is not used

1. Reset DDC1 enable (by default, DDC1 enable is cleared as LOW after Power-on Reset).
2. Set SWENB as high (the default value is zero.)
3. Depending on the data size of EDID data, set EX_DAT as LOW (128 bytes) or HIGH (256 bytes).
4. By using bulky moving commands (DDCADR, RAMBUF involved) to move the entire EDID data to RAM buffer.
5. Reset SWENB to LOW.
6. Reset DDCADR to 00h.
7. Set DDC1 enable as HIGH.

In case SWENB is set as high, interrupt service routine is finished within 133 machine cycle in 40MHz System clock.

The maximum V_{SYNC} (V_{CLK}) frequency is 25Khz (40µs). And the 9th clock of V_{SYNC} (V_{CLK}) is interrupt period.

So the machine cycle be needed is calculated as below. For example,

- When 40MHz system clock, 40µs = 133 x (25ns x 12); 133 machine cycle.
- 12MHz system clock, 40µs = 40 x (83.3ns x 12); 40 machine cycle.
- 8MHz system clock, 40µs = 26 x (125ns x 12); 26 machine cycle.

Note: If EX_DAT equals to LOW, it is meant the lower part is occupied by DDC1 operation and the upper part is still free to the system. Nevertheless, the effect of the post increment just applies to the part related to DDC1 operation. In other words, the system program is still able to address the locations from 128 to 255 in the RAM buffer through MOVX command but without the facility of the post increment. For example, the case of accessing 200 of the RAM Buffer:

MOV R0, #200, and

MOVX A, @R0

Figure 41. Transmission protocol in the DDC1 interface

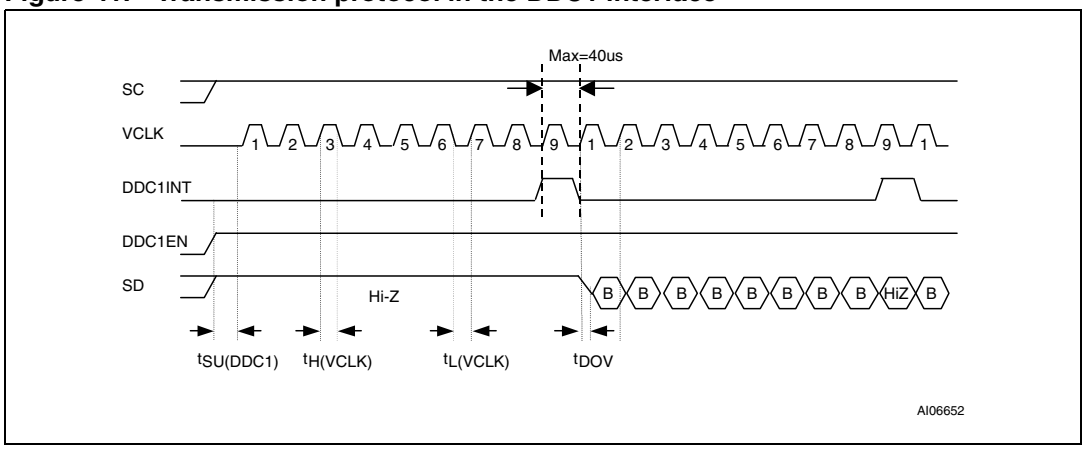
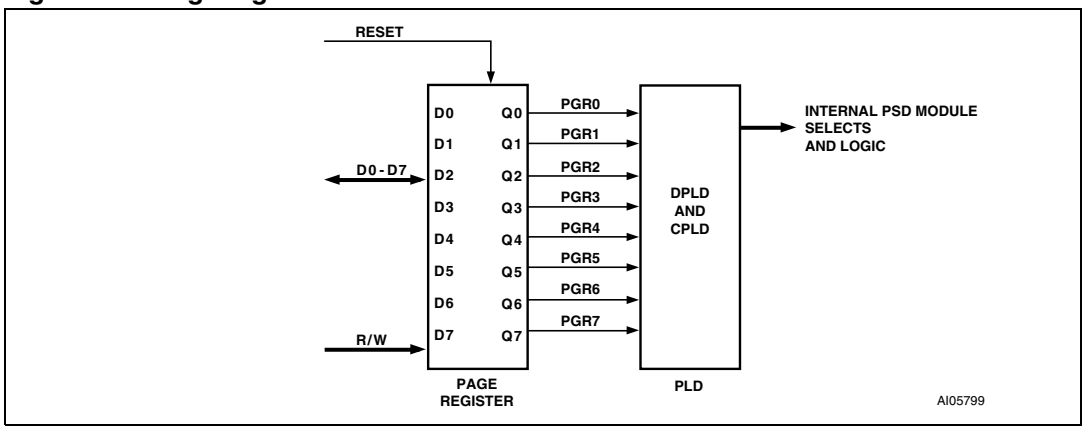


Figure 56. Page register

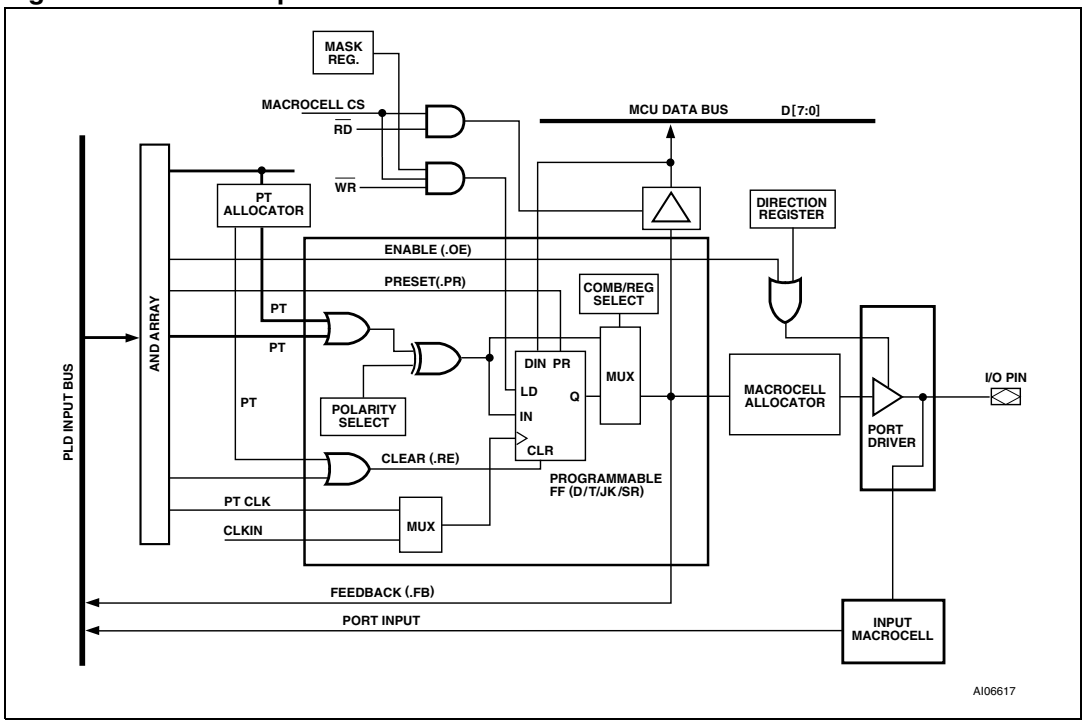


23.5.1 Loading and Reading the Output Macrocells (OMC)

The Output Macrocells (OMC) block occupies a memory location in the MCU address space, as defined by the CSIOP block (see *Section 24: I/O ports (PSD module)*). The flip-flops in each of the 16 Output Macrocells (OMC) can be loaded from the data bus by a MCU. Loading the Output Macrocells (OMC) with data from the MCU takes priority over internal functions. As such, the preset, clear, and clock inputs to the flip-flop can be overridden by the MCU. The ability to load the flip-flops and read them back is useful in such applications as loadable counters and shift registers, mailboxes, and handshaking protocols.

Data can be loaded to the Output Macrocells (OMC) on the trailing edge of WRITE Strobe ($\overline{WR}$, edge loading) or during the time that WRITE Strobe ($\overline{WR}$) is active (level loading). The method of loading is specified in PSDsoft Express Configuration.

Figure 59. CPLD output macrocell



23.5.2 OMC mask register

There is one Mask Register for each of the two groups of eight Output Macrocells (OMC). The Mask Registers can be used to block the loading of data to individual Output Macrocells (OMC). The default value for the Mask Registers is 00h, which allows loading of the Output Macrocells (OMC). When a given bit in a Mask Register is set to a '1,' the MCU is blocked from writing to the associated Output Macrocells (OMC). For example, suppose McellAB0-McellAB3 are being used for a state machine. You would not want a MCU write to McellAB to overwrite the state machine registers. Therefore, you would want to load the Mask Register for McellAB (Mask Macrocell AB) with the value 0Fh.

23.5.3 Output enable of the OMC

The Output Macrocells (OMC) block can be connected to an I/O port pin as a PLD output. The output enable of each port pin driver is controlled by a single product term from the

25 Power management

All PSD modules offer configurable power saving options. These options may be used individually or in combinations, as follows:

- The primary and secondary Flash memory, and SRAM blocks are built with power management technology. In addition to using special silicon design methodology, power management technology puts the memories into Standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory “wakes up,” changes and latches its outputs, then goes back to standby. The designer does *not* have to do anything special to achieve Memory Standby mode when no inputs are changing—it happens automatically.
- The PLD sections can also achieve Standby mode when its inputs are not changing, as described in the sections on the Power Management mode Registers (PMMR).
- As with the Power Management mode, the Automatic Power Down (APD) block allows the PSD module to reduce to Standby current automatically. The APD Unit can also block MCU address/data signals from reaching the memories and PLDs.
- Built in logic monitors the Address Strobe of the MCU for activity. If there is no activity for a certain time period (MCU is asleep), the APD Unit initiates Power-down mode (if enabled). Once in Power-down mode, all address/data signals are blocked from reaching memory and PLDs, and the memories are deselected internally. This allows the memory and PLDs to remain in Standby mode even if the address/data signals are changing state externally (noise, other devices on the MCU bus, etc.). Keep in mind that any unblocked PLD input signals that are changing states keeps the PLD out of Standby mode, but not the memories.
- PSD Chip Select Input ($\overline{\text{CSI}}$, PD2) can be used to disable the internal memories, placing them in Standby mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD Unit. There is a slight penalty in memory access time when PSD Chip Select Input ($\overline{\text{CSI}}$, PD2) makes its initial transition from deselected to selected.
- The PMMRs can be written by the MCU at run-time to manage power. The PSD module supports “blocking bits” in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs (see Figure *Figure 70* and *Figure 71*). Significant power savings can be achieved by blocking signals that are not used in DPLD or CPLD logic equations.

Other power-saving options

The PSD module offers other reduced power saving options that are independent of the Power-down mode. Except for the PSD Chip Select Input ($\overline{CSI}$, PD2) features, they are enabled by setting bits in PMMR0 and PMMR2.

Figure 68. Enable Power-down flowchart

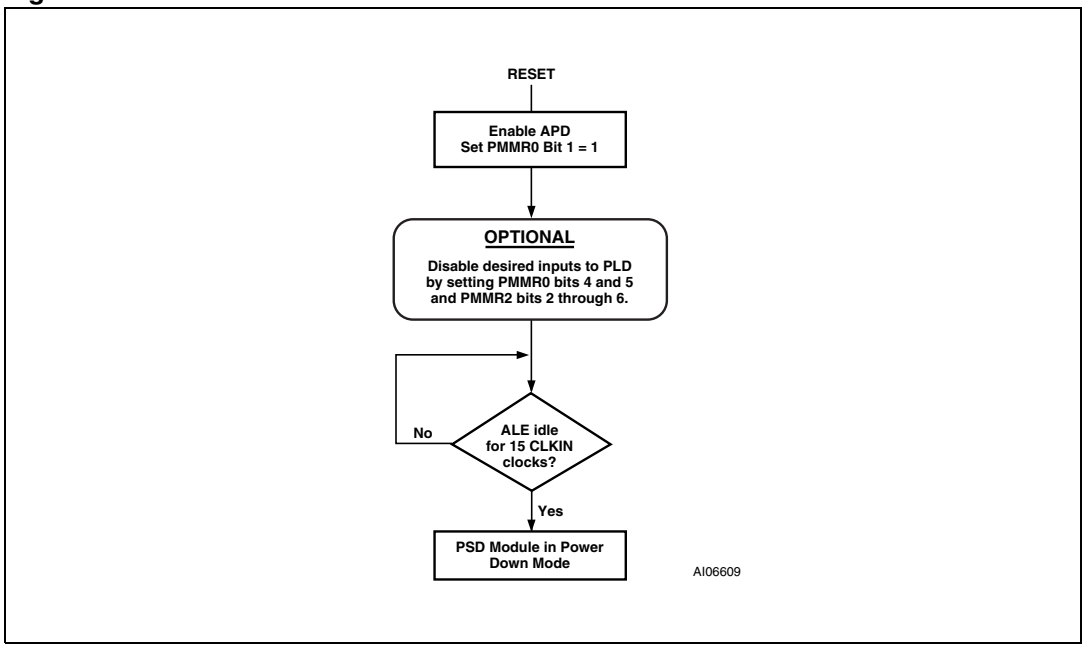


Table 102. Power-down mode's effect on ports

Port Function	Pin Level
MCU I/O	No Change
PLD Out	No Change
Address Out	Undefined
Peripheral I/O	Tri-State

25.1 PLD power management

The power and speed of the PLDs are controlled by the Turbo Bit (Bit 3) in PMMR0. By setting the bit to '1,' the Turbo mode is off and the PLDs consume the specified Standby current when the inputs are not switching for an extended time of 70 ns. The propagation delay time is increased by 10 ns (for a 5 V device) after the Turbo Bit is set to '1' (turned off) when the inputs change at a composite frequency of less than 15MHz. When the Turbo Bit is reset to '0' (turned on), the PLDs run at full power and speed. The Turbo Bit affects the PLD's DC power, AC power, and propagation delay. When the Turbo mode is off, the UPSD323xx devices' input clock frequency is reduced by 5 MHz from the maximum rated clock frequency.

Blocking MCU control signals with the bits of PMMR2 can further reduce PLD AC power consumption.

Table 106. Status during Power-on $\overline{\text{RESET}}$, Warm $\overline{\text{RESET}}$ and Power-down mode

Port Configuration	Power-On $\overline{\text{RESET}}$	Warm $\overline{\text{RESET}}$	Power-down mode
MCU I/O	Input mode	Input mode	Unchanged
PLD Output	Valid after internal PSD configuration bits are loaded	Valid	Depends on inputs to PLD (addresses are blocked in PD mode)
Address Out	Tri-stated	Tri-stated	Not defined
Peripheral I/O	Tri-stated	Tri-stated	Tri-stated

Register	Power-On $\overline{\text{RESET}}$	Warm $\overline{\text{RESET}}$	Power-down mode
PMMR0 and PMMR2	Cleared to '0'	Unchanged	Unchanged
Macrocells flip-flop status	Cleared to '0' by internal Power-on $\overline{\text{RESET}}$	Depends on .re and .pr equations	Depends on .re and .pr equations
VM Register(1)	Initialized, based on the selection in PSDsoft Configuration menu	Initialized, based on the selection in PSDsoft Configuration menu	Unchanged
All other registers	Cleared to '0'	Cleared to '0'	Unchanged

1. The SR_cod and Periphmode Bits in the VM Register are always cleared to '0' on Power-on $\overline{\text{RESET}}$ or Warm $\overline{\text{RESET}}$.

scan the status out serially using the standard JTAG channel. See Application Note *AN1153*.

$\overline{\text{TERR}}$ indicates if an error has occurred when erasing a sector or programming a byte in Flash memory. This signal goes Low (active) when an Error condition occurs, and stays Low until an “ISC_CLEAR” command is executed or a chip Reset ($\overline{\text{RESET}}$) pulse is received after an “ISC_DISABLE” command.

$\overline{\text{TSTAT}}$ behaves the same as Ready/$\overline{\text{Busy}}$ described in *Section 22.2.1: Ready/Busy (PC3)*. $\overline{\text{TSTAT}}$ is High when the PSD module device is in READ mode (primary and secondary Flash memory contents can be read). $\overline{\text{TSTAT}}$ is Low when Flash memory Program or Erase cycles are in progress, and also when data is being written to the secondary Flash memory.

$\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ can be configured as open-drain type signals during an “ISC_ENABLE” command.

27.3 Security and Flash memory protection

When the Security Bit is set, the device cannot be read on a Device Programmer or through the JTAG Port. When using the JTAG Port, only a Full Chip Erase command is allowed.

All other Program, Erase and Verify commands are blocked. Full Chip Erase returns the part to a non-secured blank state. The Security Bit can be set in PSDsoft Express Configuration.

All primary and secondary Flash memory sectors can individually be sector protected against erasures. The sector protect bits can be set in PSDsoft Express Configuration.

Table 118. DC characteristics (5 V devices) (continued)

Symbol	Parameter		Test conditions (in addition to those in *Table 113*)	Min.	Typ.	Max.	Unit
I_{FR}	XTAL feedback resistor current (XTAL1)		XTAL1 = V_{CC} XTAL2 = V_{SS}	–20		–50	µA
I_{LI}	Input leakage current		$V_{SS} < V_{IN} < V_{CC}$	–1		1	µA
I_{LO}	Output leakage current		$0.45 < V_{OUT} < V_{CC}$	–10		10	µA
I_{PD}(1)	Power-down mode		V_{CC} = 5.5 V LVD logic disabled			250	µA
			LVD logic enabled			380	µA
I_{CC_CPU} (2,3,6)	Active (12 MHz)		V_{CC} = 5 V		20	30	mA
	Idle (12 MHz)				8	10	mA
	Active (24 MHz)		V_{CC} = 5 V		30	38	mA
	Idle (24 MHz)				15	20	mA
	Active (40 MHz)		V_{CC} = 5 V		40	62	mA
	Idle (40 MHz)				20	30	mA
I_{CC_PSD} (DC)(6)	Operating supply current	PLD Only	PLD_TURBO = Off, f = 0 MHz(4)		0		µA/PT(5)
			PLD_TURBO = On, f = 0 MHz		400	700	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		15	30	mA
			Read-only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC_PSD} (AC)(6)	PLD AC Base			Note 5			
	Flash memory AC adder				2.5	3.5	mA/MHz
	SRAM AC adder				1.5	3.0	mA/MHz

1. I_{PD} (Power-down mode) is measured with:
XTAL1=V_{SS}; XTAL2=not connected; $\overline{\text{RESET}}$=V_{CC}; Port 0 =V_{CC}; all other pins are disconnected. PLD not in Turbo mode.
2. I_{CC_CPU} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS}+0.5 V, V_{IH} = Vcc – 0.5 V, XTAL2 = not connected; $\overline{\text{RESET}}$=V_{SS}; Port 0=V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (approximately 1mA).
3. I_{CC_CPU} (Idle mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS}+0.5 V, V_{IH} = V_{CC}– 0.5 V, XTAL2 = not connected; Port 0 = V_{CC};
4. $\overline{\text{RESET}}$=V_{CC}; all other pins are disconnected.
5. PLD is in non-Turbo mode and none of the inputs are switching.
6. See *Figure 70* for the PLD current calculation.
7. I/O current = 0 mA, all I/O pins are disconnected.

Table 121. External program memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{LHLL}	ALE pulse width	43		$2\ t_{CLCL} - 40$		ns
t_{AVLL}	Address set-up to ALE	17		$t_{CLCL} - 25$		ns
t_{LLAX}	Address hold after ALE	17		$t_{CLCL} - 25$		ns
t_{LLIV}	ALE Low to valid instruction in		80		$4\ t_{CLCL} - 87$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	22		$t_{CLCL} - 20$		ns
t_{PLPH}	$\overline{PSEN}$ pulse width	95		$3\ t_{CLCL} - 30$		ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in		60		$3\ t_{CLCL} - 65$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}[2]	Input instruction float after $\overline{PSEN}$		32		$t_{CLCL} - 10$	ns
t_{PXAV}[2]	Address valid after $\overline{PSEN}$	37		$t_{CLCL} - 5$		ns
t_{AVIV}	Address to valid instruction in		148		$5\ t_{CLCL} - 60$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	–10		–10		ns

1. Conditions (in addition to those in *Table 114*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)
2. Interfacing the UPSD323xx devices to devices with float times up to 35 ns is permissible. This limited bus contention does not cause any damage to Port 0 drivers.

Table 122. External clock drive (with the 5 V MCU module)

Symbol	Parameter[1]	40 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 24 to 40 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	Oscillator period			25	41.7	ns
t_{WLWH}	High time			10	$t_{CLCL} - t_{CLCX}$	ns
t_{LLAX2}	Low time			10	$t_{CLCL} - t_{CLCX}$	ns
t_{RHDX}	Rise time				10	ns
t_{RHDX}	Fall time				10	ns

1. Conditions (in addition to those in *Table 113*, V_{CC} = 4.5 to 5.5 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF; C_L for other outputs is 80 pF

Table 125. External data memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{WLWH}	$\overline{WR}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{LLAX2}	Address hold after ALE	56		2 t_{CLCL} – 27		ns
t_{RHDX}	$\overline{RD}$ to valid data in		118		5 t_{CLCL} – 90	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		63		2 t_{CLCL} – 20	ns
t_{LLDV}	ALE to valid data in		200		8 t_{CLCL} – 133	ns
t_{AVDV}	Address to valid data in		220		9 t_{CLCL} – 155	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	75	175	3 t_{CLCL} – 50	t_{CLCL} + 50	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	67		4 t_{CLCL} – 97		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	17	67	t_{CLCL} – 25	t_{CLCL} + 25	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 37		ns
t_{QVWH}	Data set-up before $\overline{WR}$	170		7 t_{CLCL} – 122		ns
t_{WHQX}	Data hold after $\overline{WR}$	15		t_{CLCL} – 27		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 114*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)

Table 126. A/D analog specification

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AV_{REF}	Analog power supply input voltage range		V_{SS}		V_{CC}	V
V_{AN}	Analog input voltage range		V_{SS} – 0.3		AV_{REF} + 0.3	V
I_{AVDD}	Current following between V_{CC} and V_{SS}				200	µA
CA_{IN}	Overall accuracy				±2	l.s.b.
N_{NLE}	Non-linearity error				±2	l.s.b.
N_{DNLE}	Differential non-linearity error				±2	l.s.b.
N_{ZOE}	Zero-offset error				±2	l.s.b.
N_{FSE}	Full scale error				±2	l.s.b.
N_{GE}	Gain error				±2	l.s.b.
t_{CONV}	Conversion time	at 8 MHz clock			20	µs