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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, UART/USART
Peripherals	LVR, POR, PWM, WDT
Number of I/O	46
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3234bv-24u6t

1 UPSD323xx description

The UPSD323xx Series combines a fast 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix including USB, to form an ideal embedded controller. At its core is an industry-standard 8032 MCU operating up to 40MHz.

A JTAG serial interface is used for In-System Programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development.

The USB 1.1 low-speed interface has one Control endpoint and two Interrupt endpoints suitable for HID class drivers.

The 8032 core is coupled to Programmable System Device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64 Kbytes using on-chip programmable decode logic.

Dual Flash memory banks provide a robust solution for remote product updates in the field through In-Application Programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips.

General purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft Express, available from the web at **www.st.com/psm**, at no charge.

The UPSD323xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
P4.7	PWM4	18	I/O	General I/O port pin	Programmable 8-bit Pulse Width modulation output 4
	USB–	8	I/O	Pull-up resistor required (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices)	
	V_{REF}	70	O	Reference Voltage input for ADC	
	RD_	65	O	READ signal, external bus	
	WR_	62	O	WRITE signal, external bus	
	PSEN_	63	O	$\overline{PSEN}$ signal, external bus	
	ALE	4	O	Address Latch signal, external bus	
	RESET_	68	I	Active low $\overline{RESET}$ input	
	XTAL1	48	I	Oscillator input pin for system clock	
	XTAL2	49	O	Oscillator output pin for system clock	
PA0		35	I/O	General I/O port pin	PLD macrocell outputs PLD inputs Latched address out (A0-A7) Peripheral I/O mode
PA1		34	I/O	General I/O port pin	
PA2		32	I/O	General I/O port pin	
PA3		28	I/O	General I/O port pin	
PA4		26	I/O	General I/O port pin	
PA5		24	I/O	General I/O port pin	
PA6		22	I/O	General I/O port pin	
PA7		21	I/O	General I/O port pin	
PB0		80	I/O	General I/O port pin	PLD macrocell outputs PLD inputs Latched address out (A0-A7)
PB1		78	I/O	General I/O port pin	
PB2		76	I/O	General I/O port pin	
PB3		74	I/O	General I/O port pin	
PB4		73	I/O	General I/O port pin	
PB5		72	I/O	General I/O port pin	
PB6		67	I/O	General I/O port pin	
PB7		66	I/O	General I/O port pin	

Table 3. RAM address (continued)

Byte address (in hexadecimal)									Byte address (in decimal)
-									-
22h	17	16	15	14	13	12	11	10	34
21h	0F	0E	0D	0C	0B	0A	09	08	33
20h	07	06	05	04	03	02	01	00	32
1Fh	Register bank 3								31
18h									24
17h	Register bank 2								23
10h									16
0Fh	Register bank 1								15
08h									8
07h	Register bank 0								7
00h									0

2.9 Addressing modes

The addressing modes in UPSD323xx devices instruction set are as follows

1. Direct addressing
2. Indirect addressing
3. Register addressing
4. Register-specific addressing
5. Immediate constants addressing
6. Indexed addressing

2.9.1 Direct addressing

In a direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs (80~FFH RAM) can be directly addressed.

Example:

mov A, 3EH ; A <----- RAM[3E]

Figure 10. Direct addressing

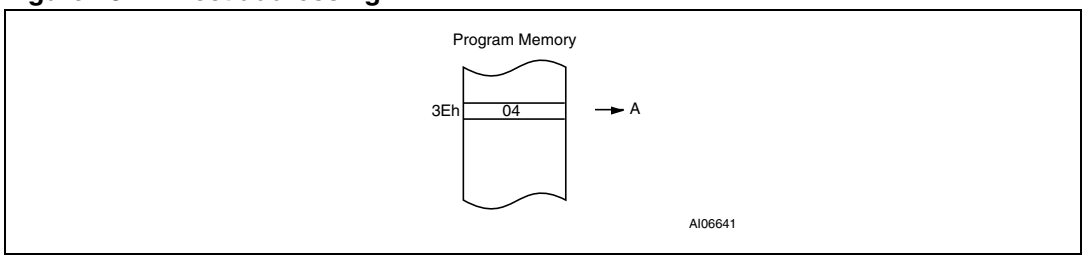


Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
C9	T2MOD								DCEN	00	Timer 2 mode
CA	RCAP2L									00	Timer 2 Reload low
CB	RCAP2H									00	Timer 2 Reload High
CC	TL2									00	Timer 2 Low byte
CD	TH2									00	Timer 2 High byte
D0	PSW	CY	AC	FO	RS1	RS0	OV		P	00	Program Status Word
D1	S1SETUP									00	DDC I^2C (S1) Setup
D2	S2SETUP									00	I^2C (S2) Setup
D4	RAMBUF									XX	DDC Ram Buffer
D5	DDCDAT									00	DDC Data xmit register
D6	DDCADR									00	Addr pointer register
D7	DDCCON	—	EX_DAT	SWENB	DDC_AX	DDCINT	DDC1EN	SWHINT	M0	00	DDC Control Register
D8	S1CON	CR2	ENI1	STA	STO	ADDR	AA	CR1	CR0	00	DDC I^2C Control Reg
D9	S1STA	GC	Stop	Intr	TX-Md	Bbusy	Blost	ACK_R	SLV	00	DDC I^2C Status
DA	S1DAT									00	Data Hold Register
DB	S1ADR									00	DDC I^2C address
DC	S2CON	CR2	EN1	STA	STO	ADDR	AA	CR1	CR0	00	I^2C Bus Control Reg
DD	S2STA	GC	Stop	Intr	TX-Md	Bbusy	Blost	ACK_R	SLV	00	I^2C Bus Status
DE	S2DAT									00	Data Hold Register
DF	S2ADR									00	I^2C address
E0	ACC									00	Accumulator

Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
E1	USCL									00	8-bit Prescaler for USB logic
E6	UDT1	UDT1.7	UDT1.6	UDT1.5	UDT1.4	UDT1.3	UDT1.2	UDT1.1	UDT1.0	00	USB Endpt1 Data Xmit
E7	UDT0	UDT0.7	UDT0.6	UDT0.5	UDT0.4	UDT0.3	UDT0.2	UDT0.1	UDT0.0	00	USB Endpt0 Data Xmit
E8	UISTA	SUSPND	—	RSTF	TXD0F	RXD0F	RXD1F	EOPF	RESUMF	00	USB Interrupt Status
E9	UIEN	SUSPND IE	RSTE	RSTFI E	TXD0IE	RXD0IE	TXD1IE	EOPIE	RESUMI E	00	USB Interrupt Enable
EA	UCON0	TSEQ0	STALL0	TX0E	RX0E	TP0SIZ3	TP0SiZ2	TP0SIZ1	TP0SIZ0	00	USB Endpt0 Xmit Control
EB	UCON1	TSEQ1	EP12SEL	—	FRESUM	TP1SIZ3	TP1SiZ2	TP1SIZ1	TP1SIZ0	00	USB Endpt1 Xmit Control
EC	UCON2	—	—	—	SOUT	EP2E	EP1E	STALL2	STALL1	00	USB Control Register
ED	USTA	RSEQ	SETUP	IN	OUT	RP0SIZ3	RP0SIZ2	RP0SIZ1	RP0SIZ0	00	USB Endpt0 Status
EE	UADR	USBEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0	00	USB Address Register
EF	UDR0	UDR0.7	UDR0.6	UDR0.5	UDR0.4	UDR0.3	UDR0.2	UDR0.1	UDR0.0	00	USB Endpt0 Data Recv
F0	B									00	B Register

Table 17. PSD module register address offset

CSIOP addr offset	Register name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
00	Data In (Port A)	Reads Port pins as input									
02	Control (Port A)	Configure pin between I/O or Address Out mode. Bit = 0 selects I/O								00	
04	Data Out (Port A)	Latched data for output to Port pins, I/O Output mode								00	
06	Direction (Port A)	Configures Port pin as input or output. Bit = 0 selects input								00	
08	Drive (Port A)	Configures Port pin between CMOS, Open Drain or Slew rate. Bit = 0 selects CMOS								00	
0A	Input Macrocell (Port A)	Reads latched value on Input Macrocells									
0C	Enable Out (Port A)	Reads the status of the output enable control to the Port pin driver. Bit = 0 indicates pin is in input mode.									

5.5 External Int1 interrupt

- The INT1 can be either level active or transition active depending on Bit IT1 in register TCON. The flag that actually generates this interrupt is Bit IE1 in TCON.
- When an external interrupt is generated, the corresponding request flag is cleared by the hardware when the service routine is vectored to only if the interrupt was transition activated.
- If the interrupt was level activated then the interrupt request flag remains set until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.
- The ADC can take over the External INT1 to generate an interrupt on conversion being completed

5.6 DDC interrupt

- The DDC interrupt is generated either by Bit INTR in the S1STA register for DC2B protocol or by Bit DDC interrupt in the DDCCON register for DDC1 protocol or by Bit SWHINT Bit in the DDCCON register when DDC protocol is changed from DDC1 to DDC2.
- Flags except the INTR have to be cleared by the software. INTR flag is cleared by hardware.

5.7 USB interrupt

- The USB interrupt is generated when endpoint0 has transmitted a packet or received a packet, when Endpoint1 or Endpoint2 has transmitted a packet, when the suspend or resume state is detected and every EOP received.
- When the USB interrupt is generated, the corresponding request flag must be cleared by software. The interrupt service routine will have to check the various USB registers to determine the source and clear the corresponding flag.
- Please see the dedicated interrupt control registers for the USB peripheral for more information.

5.8 USART interrupt

- The USART Interrupt is generated by RI (receive interrupt) OR TI (transmit interrupt).
- When the USART Interrupt is generated, the corresponding request flag must be cleared by software. The interrupt service routine will have to check the various USART registers to determine the source and clear the corresponding flag.
- Both USART's are identical, except for the additional interrupt controls in the Bit 4 of the additional interrupt control registers (A7h, B7h)

9 Supervisory

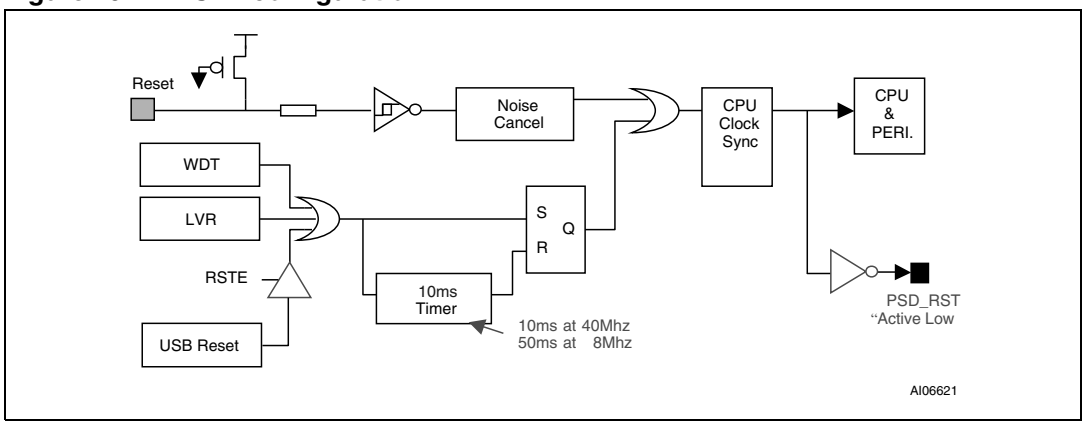
There are four ways to invoke a reset and initialize the UPSD323xx devices.

1. Via the external $\overline{\text{RESET}}$ pin
2. Via the internal LVR block
3. Via USB bus reset signaling
4. Via Watchdog Timer (WDT)

The $\overline{\text{RESET}}$ mechanism is illustrated in *Figure 19*.

Each $\overline{\text{RESET}}$ source will cause an internal reset signal active. The CPU responds by executing an internal reset and puts the internal registers in a defined state. This internal reset is also routed as an active low reset input to the PSD module.

Figure 19. $\overline{\text{RESET}}$ configuration



9.1 External reset

The $\overline{\text{RESET}}$ pin is connected to a Schmitt trigger for noise reduction. A $\overline{\text{RESET}}$ is accomplished by holding the $\overline{\text{RESET}}$ pin LOW for at least 1ms at power up while the oscillator is running. Refer to AC spec on other $\overline{\text{RESET}}$ timing requirements.

9.2 Low V_{DD} voltage reset

An internal reset is generated by the LVR circuit when the V_{DD} drops below the reset threshold. After V_{DD} reaching back up to the reset threshold, the $\overline{\text{RESET}}$ signal will remain asserted for 10ms before it is released. On initial power-up the LVR is enabled (default). After power-up the LVR can be disabled via the LVREN Bit in the PCON Register.

Note: The LVR logic is still functional in both the Idle and Power-down modes.

The reset threshold:

- 5 V operation: 4 V ± 0.25 V
- 3.3 V operation: 2.5 V ± 0.2 V

This logic supports approximately 0.1 V of hysteresis and 1 µs noise-cancelling delay.

11 Timer/counters (Timer 0, Timer 1 and Timer 2)

The UPSD323xx devices has three 16-bit Timer/Counter registers: Timer 0, Timer 1 and Timer 2. All of them can be configured to operate either as timers or event counters and are compatible with standard 8032 architecture.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency or 1/12 of the oscillator frequency (f_{OSC}).

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 f_{OSC} clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the f_{OSC}. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full cycle. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes from which to select.

11.1 Timer 0 and Timer 1

The “Timer” or “Counter” function is selected by control bits C/ T in the Special Function Register TMOD. These Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for Timers/ Counters. Mode 3 is different. The four operating modes are de-scribed in the following text.

Table 36. Control register (TCON)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 37. Description of the TCON bits

Bit	Symbol	Function
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine
6	TR1	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter on or off
5	TF0	Timer 0 overflow flag. Set by hardier on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine
4	TR0	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter on or off
3	IE1	Interrupt 1 Edge Flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed
2	IT1	Interrupt 1 Type Control Bit. Set/cleared by software to specify falling-edge/low-level triggered external interrupt

Table 68. Description of the UISTA bits (continued)

Bit	Symbol	R/W	Function
4	TXD0F	R/W	Endpoint0 Data Transmit Flag. This bit is set after the data stored in Endpoint 0 transmit buffers has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX0E must also be set. If TXD0F Bit is not cleared, a NAK handshake will be returned in the next IN transactions. RESET clears this bit.
3	RXD0F	R/W	Endpoint0 Data Receive Flag. This bit is set after the USB module has received a data packet and responded with ACK handshake packet. Software must clear this flag after all of the received data has been read. Software must also set RX0E Bit to one to enable the next data packet reception. If RXD0F Bit is not cleared, a NAK handshake will be returned in the next OUT transaction. RESET clears this bit.
2	TXD1F	R/W	Endpoint1 / Endpoint2 Data Transmit Flag. This bit is shared by Endpoints 1 and Endpoints 2. It is set after the data stored in the shared Endpoint 1/ Endpoint 2 transmit buffer has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX1E must also be set. If TXD1F Bit is not cleared, a NAK handshake will be returned in the next IN transaction. RESET clears this bit.
1	EOPF	R/W	End of Packet Flag. This bit is set when a valid End of Packet sequence is detected on the D+ and D-line. Software must clear this flag. RESET clears this bit.
0	RESUMF	R/W	Resume Flag. This bit is set when USB bus activity is detected while the SUSPND Bit is set. Software must clear this flag. RESET clears this bit.

Table 69. USB Endpoint0 transmit control register (UCON0: 0EAh)

7	6	5	4	3	2	1	0
TSEQ0	STALL0	TX0E	RX0E	TP0SIZ3	TP0SIZ2	TP0SIZ1	TP0SIZ0

Table 82. Transceiver AC characteristics

Symb	Parameter	Test Conditions(1)	Min	Max	Unit
tDRATE	Low Speed Data Rate	Ave. bit rate (1.5Mb/s ± 1.5%)	1.4775	1.5225	Mbit/s
tDJR1	Receiver Data Jitter Tolerance	To next transition, *Figure 46*(5)	–75	75	ns
tDJR2	Differential Input Sensitivity	For paired transition, *Figure 46*(5)	–45	45	ns
tDEOP	Differential to EOP Transition Skew	*Figure 47*(5)	–40	100	ns
tEOPR1	EOP Width at Receiver	Rejects as EOP(5,6)	165	—	ns
tEOPR2	EOP Width at Receiver	Accepts as EOP(5)	675	—	ns
tEOPT	Source EOP Width	—	–1.25	1.50	µs
tUDJ1	Differential Driver Jitter	To next transition, *Figure 48*	–95	95	ns
tUDJ2	Differential Driver Jitter	To paired transition, *Figure 48*	–150	150	ns
tR	USB Data Transition Rise Time	Notes 2, 3, 4	75	300	ns
tF	USB Data Transition Fall Time	Notes 2, 3, 4	75	300	ns
tRFM	Rise/Fall Time Matching	t_R / t_F	80	120	%
V_{CRS}	Output Signal Crossover Voltage	—	1.3	2.0	V

1. V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to 70°C.
2. Level guaranteed for range of V_{CC} = 4.5 V to 5.5 V.
3. With RPU, external idle resistor, 7.5κ±2%, D- to V_{CC}.
4. C_L of 50 pF (75 ns) to 350 pF (300 ns).
5. Measured at crossover point of differential data signals.
6. USB specification indicates 330 ns.

Table 83. Methods of programming different functional blocks of the PSD module

Functional Block	JTAG programming	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD array (DPLD and CPLD)	Yes	Yes	No
PSD module configuration	Yes	Yes	No

22.5.4 Data polling flag (DQ7)

When erasing or programming in Flash memory, the Data Polling flag bit (DQ7) outputs the complement of the bit being entered for programming/writing on the DQ7 Bit. Once the Program instruction or the WRITE operation is completed, the true logic value is read on the Data Polling flag bit (DQ7) (in a READ operation).

- Data Polling is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction). It must be performed at the address being programmed or at an address within the Flash memory sector being erased.
- During an Erase cycle, the Data Polling flag bit (DQ7) outputs a '0.' After completion of the cycle, the Data Polling flag bit (DQ7) outputs the last bit programmed (it is a '1' after erasing).
- If the byte to be programmed is in a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors to be erased are protected, the Data Polling flag bit (DQ7) is reset to '0' for about 100µs, and then returns to the previous addressed byte. No erasure is performed.

22.5.5 Toggle flag (DQ6)

The Flash memory offers another way for determining when the Program cycle is completed. During the internal WRITE operation and when either the FS0-FS7 or CSBOOT0-CSBOOT3 is true, the Toggle flag bit (DQ6) toggles from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory.

When the internal cycle is complete, the toggling stops and the data READ on the Data Bus D0-D7 is the addressed memory byte. The device is now accessible for a new READ or WRITE operation. The cycle is finished when two successive Reads yield the same output data.

- The Toggle flag bit (DQ6) is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction).
- If the byte to be programmed belongs to a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors selected for erasure are protected, the Toggle flag bit (DQ6) toggles to '0' for about 100µs and then returns to the previous addressed byte.

22.5.6 Error flag (DQ5)

During a normal Program or Erase cycle, the Error flag bit (DQ5) is to '0.' This bit is set to '1' when there is a failure during Flash memory Byte Program, Sector Erase, or Bulk Erase cycle.

In the case of Flash memory programming, the Error flag bit (DQ5) indicates the attempt to program a Flash memory bit from the programmed state, '0', to the erased state, '1,' which is not valid. The Error flag bit (DQ5) may also indicate a Time-out condition while attempting to program a byte.

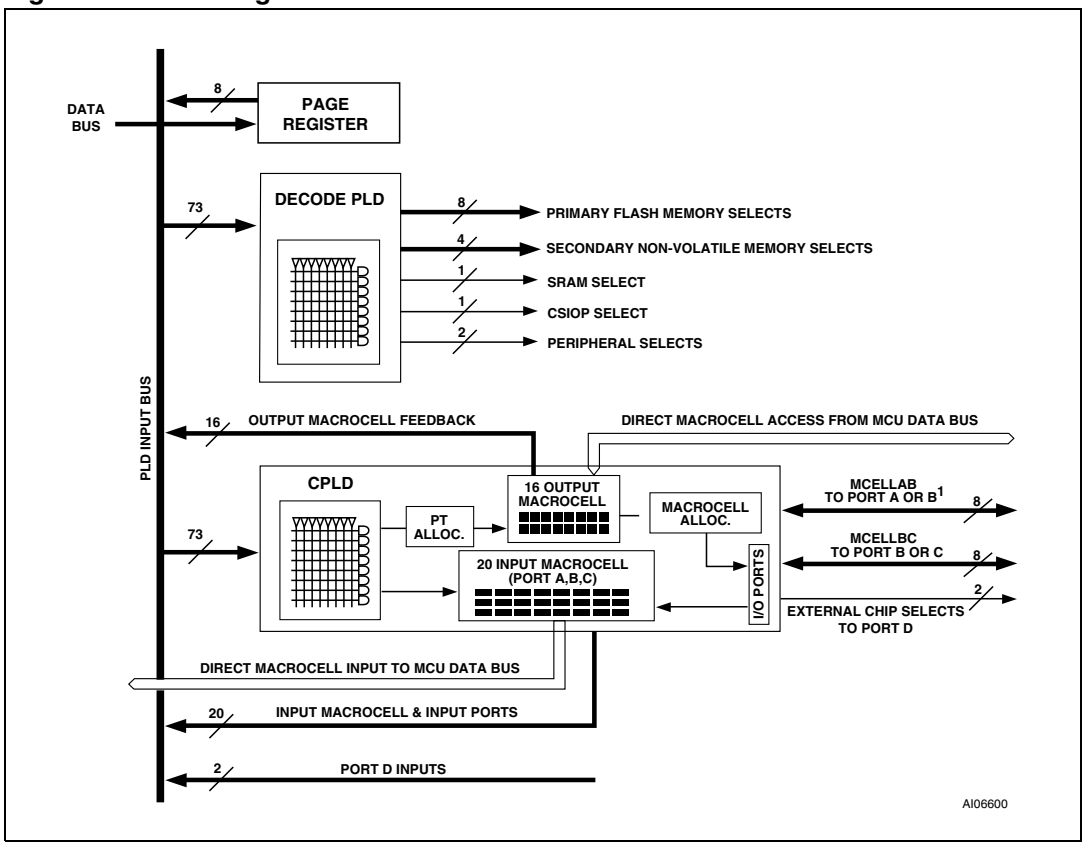
In case of an error in a Flash memory Sector Erase or Byte Program cycle, the Flash memory sector in which the error occurred or to which the programmed byte belongs must no longer be used. Other Flash memory sectors may still be used. The Error Flag bit (DQ5) is reset after a Reset Flash instruction.

See *Section 25: Power management* for details on how to set the Turbo Bit.

Additionally, five bits are available in PMMR2 to block MCU control signals from entering the PLDs. This reduces power consumption and can be used only when these MCU control signals are not used in PLD logic equations.

Each of the two PLDs has unique characteristics suited for its applications. They are described in the following sections.

Figure 57. PLD diagram



1. Port A is not available in the 52-pin package

23.2 Decode PLD (DPLD)

The DPLD, shown in *Figure 91*, is used for decoding the address for PSD module and external components. The DPLD can be used to generate the following decode signals:

- 8 Sector Select (FS0-FS7) signals for the primary Flash memory (three product terms each)
- 4 Sector Select (CSBOOT0-CSBOOT3) signals for the secondary Flash memory (three product terms each)
- 1 internal SRAM Select (RS0) signal (two product terms)
- 1 internal CSIOP Select signal (selects the PSD module registers)
- 2 internal Peripheral Select signals (Peripheral I/O mode).

29 AC/DC parameters

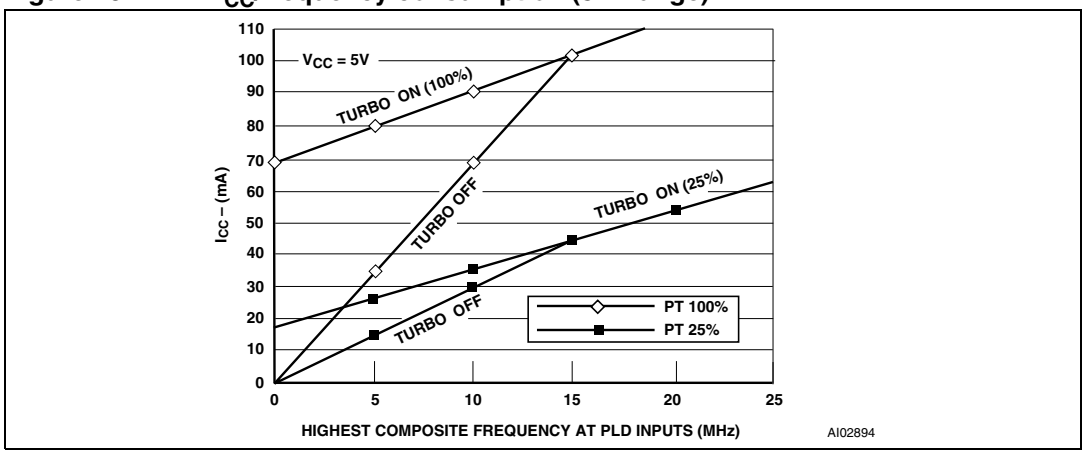
These tables describe the AD and DC parameters of the UPSD323xx devices:

- DC Electrical Specification
- AC Timing Specification
- PLD Timing
  - Combinatorial Timing
  - Synchronous Clock mode
  - Asynchronous Clock mode
  - Input Macrocell Timing
- MCU module Timing
  - READ Timing
  - WRITE Timing
  - Power-down and $\overline{\text{RESET}}$ Timing

The following are issues concerning the parameters presented:

- In the DC specification the supply current is given for different modes of operation.
- The AC power component gives the PLD, Flash memory, and SRAM mA/MHz specification. *Figure 70* and *Figure 71* show the PLD mA/MHz as a function of the number of Product Terms (PT) used.
- In the PLD timing parameters, add the required delay when Turbo Bit is '0.'

Figure 70. PLD I_{CC}/frequency consumption (5 V range)



31 EMC characteristics

Susceptibility test are performed on a sample basis during product characterization.

31.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

31.1.1 ESD

Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 Standard.

31.1.2 FTB

A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 Standard.

A device reset allows normal operations to be resumed. The test results are given in *Table 110*, based on the EMS levels and classes defined in Application Note AN1709.

31.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the user's application.

31.2.1 Software recommendations

The software flowchart must include the management of 'runaway' conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (e.g., control registers)

31.2.2 Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see Application Note AN1015).

Table 117. Major parameters (continued)

Parameters/conditions/ comments	5 V test conditions	5.0 V value	3.3 V test conditions	3.3 V value	Unit
Standby current, typical (Power-down mode, requires reset to exit mode; without Low-Voltage Detect (LVD) Supervisor)	180 µA with LVD	110	100 µA with LVD	60	µA
I/O sink/source current Ports A, B, C, and D	V_{OL} = 0.25 V (max); V_{OH} = 3.9 V (min)	I_{OL} = 8 (max); I_{OH} = –2 (min)	V_{OL} = 0.15 V (max); V_{OH} = 2.6 V (min)	I_{OL} = 4 (max); I_{OH} = –1 (min)	mA
PLD macrocells (For registered or combinatorial logic)	–	16	–	16	–
PLD inputs (Inputs from pins, macrocell feedback, or MCU addresses)	–	69	–	69	–
PLD outputs (Output to pins or internal feedback)	–	16	–	16	–
PLD propagation delay, typical (PLD input to output, Turbo mode)	–	15	–	22	ns

Table 119. DC characteristics (3 V devices)

Symbol	Parameter	Test conditions (in addition to those in *Table 114*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], A, B, C, D, XTAL1, $\overline{RESET}$)	3.0 V < V_{CC} < 3.6 V	0.7V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input high voltage (Port 4[Bit 2])	3.0 V < V_{CC} < 3.6 V	2.0		V_{CC} + 0.5	V
V_{IL}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	3.0 V < V_{CC} < 3.6 V	V_{SS}– 0.5		0.3 V_{CC}	V
V_{IL1}	Input low voltage (Ports A, B, C, D)	3.0 V < V_{CC} < 3.6 V	–0.5		0.8	V
	Input low voltage (Port 4[Bit 2])	3.0 V < V_{CC} < 3.6 V	V_{SS}– 0.5		0.8	V
V_{OL}	Output low voltage (Ports A,B,C,D)	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1	V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.45	V
V_{OL1}	Output low voltage (Ports 1,2,3,4, $\overline{WR}$, $\overline{RD}$)	I_{OL} = 1.6 mA			0.45	V
		I_{OL} = 100 µA			0.3	V
V_{OL2}	Output low voltage (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA			0.45	V
		I_{OL} = 200 µA			0.3	V
V_{OH}	Output high voltage (Ports A,B,C,D)	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99		V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6		V
V_{OH2}	Output high voltage (Port 0 in ext. Bus mode, ALE, $\overline{PSEN}$)	I_{OH} = –800 µA	2.0			V
		I_{OH} = –80 µA	2.7			V
V_{LVR}	Low voltage reset	0.1 V hysteresis	2.3	2.5	2.7	V
V_{OP}	XTAL open bias voltage (XTAL1, XTAL2)	I_{OL} = 3.2 mA	1.0		2.0	V
V_{LKO}	V_{CC}(min) for Flash Erase and Program		1.5		2.2	V
I_{IL}	Logic '0' input current (Ports 1,2,3,4)	V_{IN} = 0.45 V (0 V for Port 4[pin 2])	–1		–50	µA
I_{TL}	Logic 1-to-0 transition current (Ports 1,2,3,4)	V_{IN} = 3.5 V (2.5 V for Port 4[pin 2])	–25		–250	µA
I_{RST}	Reset pin pull-up current ($\overline{RESET}$)	V_{IN} = V_{SS}	–10		–55	µA
I_{FR}	XTAL feedback resistor current (XTAL1)	XTAL1 = V_{CC} XTAL2 = V_{SS}	–20		–50	µA
I_{LI}	Input leakage current	V_{SS} < V_{IN} < V_{CC}	–1		1	µA
I_{LO}	Output leakage current	0.45 < V_{OUT} < V_{CC}	–10		10	µA

Table 124. External data memory AC characteristics (with the 5 V MCU module)

Symbol	Parameter[1]	40 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 24 to 40 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	120		6 t_{CLCL} – 30		ns
t_{WLWH}	$\overline{WR}$ pulse width	120		6 t_{CLCL} – 30		ns
t_{LLAX2}	Address hold after ALE	10		t_{CLCL} – 15		ns
t_{RHDX}	$\overline{RD}$ to valid data in		75		5 t_{CLCL} – 50	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		38		2 t_{CLCL} – 12	ns
t_{LLDV}	ALE to valid data in		150		8 t_{CLCL} – 50	ns
t_{AVDV}	Address to valid data in		150		9 t_{CLCL} – 75	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	60	90	3 t_{CLCL} – 15	t_{CLCL} + 15	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	70		4 t_{CLCL} – 30		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	10	40	t_{CLCL} – 15	t_{CLCL} + 15	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 20		ns
t_{QVWH}	Data set-up before $\overline{WR}$	125		7 t_{CLCL} – 50		ns
t_{WHQX}	Data hold after $\overline{WR}$	5		t_{CLCL} – 20		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 113*, V_{CC} = 4.5 to 5.5 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF; C_L for other outputs is 80 pF

Figure 77. Synchronous clock mode timing – PLD

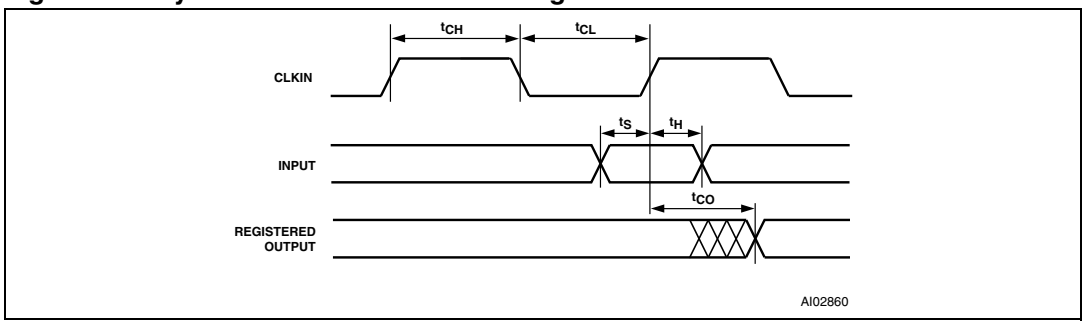


Table 129. CPLD macrocell synchronous clock mode timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT Aloc	Turbo Off	Slew rate(1)	Unit
f_{MAX}	Maximum frequency external feedback	$1/(t_S+t_{CO})$		40.0				MHz
	Maximum frequency internal feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		66.6				MHz
	Maximum frequency pipelined data	$1/(t_{CH}+t_{CL})$		83.3				MHz
t_S	Input setup time		12		+ 2	+ 10		ns
t_H	Input hold time		0					ns
t_{CH}	Clock high time	Clock input	6					ns
t_{CL}	Clock low time	Clock input	6					ns
t_{CO}	Clock to output delay	Clock input		13			– 2	ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns
t_{MIN}	Minimum clock period (2)	$t_{CH}+t_{CL}$	12					ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount.
2. CLKIN (PD1) $t_{CLCL} = t_{CH} + t_{CL}$.