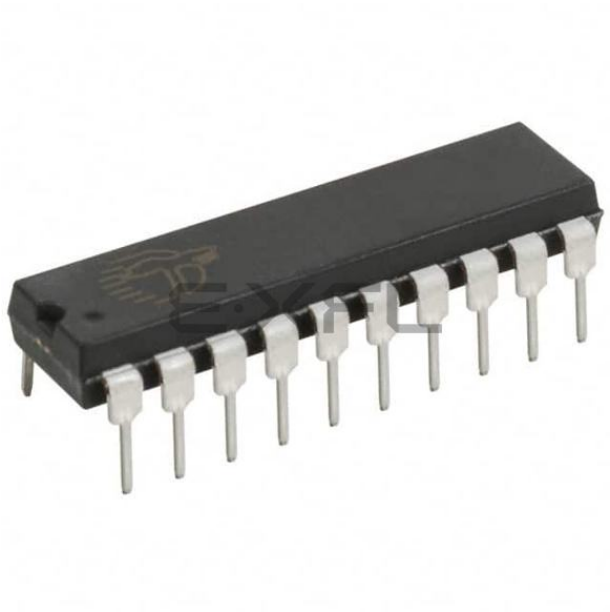

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	M8A
Program Memory Type	OTP (4kB)
Controller Series	CY7C630xx
RAM Size	128 x 8
Interface	USB
Number of I/O	12
Voltage - Supply	4V ~ 5.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c63001c-pxc

4.0 Pin Definitions (continued)

Name	I/O	20-Pin	24-pin	Die Pad #	Description
CEXT	I/O	9	11	11	Connects to external R/C timing circuit for optional 'suspend' wakeup
D+	I/O	14	16	16	USB data+
D–	I/O	13	15	15	USB data–
V_{PP}	–	8	10	10	Programming voltage supply, tie to ground during normal operation
V_{CC}	–	12	14	14	Voltage supply
V_{SS}	–	7	9	9	Ground

5.0 Pin Description

Name	Description
V_{CC}	1 pin. Connects to the USB power source or to a nominal 5V power supply. Actual V_{CC} range can vary between 4.0V and 5.25V.
V_{SS}	1 pin. Connects to ground.
V_{PP}	1 pin. Used in programming the on-chip EPROM. This pin should be tied to ground during normal operations.
XTALIN	1 pin. Input from an external ceramic resonator.
XTALOUT	1 pin. Return path for the ceramic resonator (leave unconnected if driving XTALIN from an external oscillator).
P0.0–P0.7, P1.0–P1.7	16 pins. P0.0–P0.7 are the 8 I/O lines in Port 0. P1.0–P1.7 are the 8 I/O lines in Port 1. P1.0–P1.3 are supported in the CY7C63001C. All I/O pins include bit-programmable pull-up resistors. However, the sink current of each pin can be programmed to one of sixteen levels. Besides functioning as GPIO lines, each pin can be programmed as an interrupt input. The interrupt is edge-triggered, with programmable polarity.
D+, D–	2 pins. Bidirectional USB data lines. An external pull-up resistor must be connected between the D pin and V_{CC} to select low-speed USB operation.
CEXT	1 pin. Open-drain output with Schmitt trigger input. The input is connected to a rising edge-triggered interrupt. CEXT may be connected to an external RC to generate a wake-up from Suspend mode. See Section 6.4.

6.0 Functional Description

The Cypress CY7C630/101C USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, joystick, and gamepad. These USB microcontrollers conform to the low-speed (1.5 Mbps) requirements of the USB specification version 1.1. Each microcontroller is a self-contained unit with: a USB interface engine, USB transceivers, an 8-bit RISC microcontroller, a clock oscillator, timers, and program memory. Each microcontroller supports one USB device address and two endpoints.

The 6-MHz clock is doubled to 12 MHz to drive the microcontroller. A RISC architecture with 35 instructions provides the best balance between performance and product cost.

6.1 Memory Organization

The memory in the USB Controller is organized into user program memory in EPROM space and data memory in SRAM space.

6.1.1 Program Memory Organization

The CY7C63001C and CY7C63101C each offer 4 Kbytes of EPROM. The program memory space is divided into two functional groups: interrupt vectors and program code.

The interrupt vectors occupy the first 16 bytes of the program space. Each vector is 2 bytes long. After a reset, the Program Counter points to location zero of the program space. Figure 6-1 shows the organization of the Program Memory Space.

6.1.2 Security Fuse Bit

The Cypress USB microcontroller includes a security fuse bit. When the security fuse is programmed, the EPROM program memory outputs 0xFF to the EPROM programmer, thus protecting the user's code.

8.0 Electrical Characteristics (continued) f_{OSC} = 6 MHz; Operating Temperature = 0 to 70°C, V_{CC} = 4.0 to 5.25 volts

	Parameter	Min	Max	Units	Conditions
	General Purpose I/O Interface				
R_{up}	Pull-up Resistance	8	24	k :	
$I_{sink0(0)}$	Port 0 Sink Current (0), lowest current	0.1	0.3	mA	Vout = 2.0V DC, Port 0 only[5]
$I_{sink0(F)}$	Port 0 Sink Current (F), highest current	0.5	1.5	mA	Vout = 2.0V DC, Port 0 only[5]
$I_{sink1(0)}$	Port 1 Sink Current (0), lowest current	1.6	4.8	mA	Vout = 2.0V DC, Port 1 only[5]
$I_{sink1(F)}$	Port 1 Sink Current (F), highest current	8 5	24	mA mA	Vout = 2.0V DC, Port 1 only[5] Vout = 0.4V DC, Port 1 only[5]
I_{range}	Sink Current max./min.	4.5	5.5		Vout = 2.0V DC, Port 0 or 1[5, 8]
I_{lin}	Differential Nonlinearity		0.5	I_{SB}	Port 0 or Port 1[9]
T_{ratio}	Tracking Ratio Port1 to Port0	14.4	19.6		Vout = 2.0V[10]
t_{sink}	Current Sink Response Time		0.8	Ps	Full scale transition
I_{max}	Port 1 Max Sink Current		60	mA	Summed over all Port 1 bits
P_{max}	Port 1 & Cext Sink Mode Dissipation		25	mW	Per pin
V_{ith}	Input Threshold Voltage	45%	65%	V_{CC}	All ports and Cext[11]
V_H	Input Hysteresis Voltage	6%	12%	V_{CC}	Port 0 and Port 1[12]
V_{HCext}	Input Hysteresis Voltage, Cext	12%	30%	V_{CC}	Cext Pin Only[12]
Iin	Input Leakage Current, GPIO Pins	–1	1	PA	Port 0 and Port 1, Vout = 0 or V_{CC}[13]
I_{inCx}	Input Leakage Current, Cext Pin		50	nA	V_{Cext} = 0 or V_{CC}
I_{Cext}	Sink Current, Cext Pin	6	18	mA	V_{Cext} = V_{CC}
V_{ol1}	Output LOW Voltage, Cext Pin		0.4	V	V_{CC} = Min., I_{ol} = 2 mA
V_{ol2}	Output LOW Voltage, Cext Pin		2.0	V	V_{CC} = Min., I_{ol} = 5 mA

Notes:
8. $I_{range} = I_{sink(F)}/I_{sink(0)}$ for each port 0 or 1 output.
9. Measured as largest step size vs. nominal according to measured full scale and zero programmed values.
10. $T_{ratio} = I_{sink1(n)}/I_{sink0(n)}$ for the same n.
11. Low to High transition.
12. This parameter is guaranteed, but not tested.
13. With Ports configured in Hi-Z mode.

9.0 Switching Characteristics

Parameter	Description	Min.	Max.	Unit	Conditions
	Clock				
t_{CYC}	Input Clock Cycle Time	166.67	166.67	ns	
t_{CH}	Clock HIGH Time	0.45 t_{CYC}		ns	
t_{CL}	Clock LOW Time	0.45 t_{CYC}		ns	
	USB Driver Characteristics				
t_r	USB Data Transition Rise Time	75	300	ns	See Notes 5, 6, and 14
t_f	USB Data Transition Fall Time	75	300	ns	See Notes 5, 6, and 14
t_{rfm}	Rise/Fall Time Matching	80	125	%	t_r/t_f
V_{crs}	Output Signal Crossover Voltage	1.3	2.0	V	See Note 5
	USB Data Timing				
t_{drate}	Low Speed Data Rate	1.4775	1.5225	Mb/s	Ave. Bit Rate (1.5 Mb/s ± 1.5%)
t_{djr1}	Receiver Data Jitter Tolerance	–75	75	ns	To Next Transition, Figure 9-3[15]
t_{djr2}	Receiver Data Jitter Tolerance	–45	45	ns	For Paired Transitions, Figure 9-3[15]
t_{deop}	Differential to EOP Transition Skew	–40	100	ns	Figure 9-4[15]
t_{eopr}	EOP Width at Receiver	670		ns	Accepts as EOP[15]
t_{lst}	Width of SE0 Interval During Differential Transition		210	ns	
t_{eopt}	Source EOP Width	1.25	1.50	μs	
t_{udj1}	Differential Driver Jitter	–95	95	ns	To next transition, Figure 9-5
t_{udj2}	Differential Driver Jitter	–150	150	ns	To paired transition, Figure 9-5

Notes:
14. C_{load} of 200 (75 ns) to 600 pF (300 ns).
15. Measured at crossover point of differential data signals.

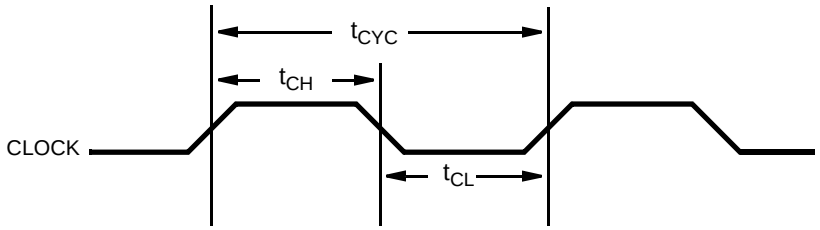


Figure 9-1. Clock Timing

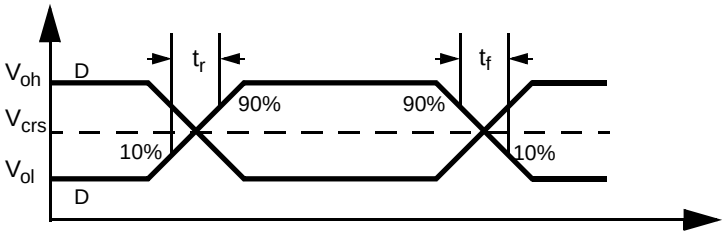


Figure 9-2. USB Data Signal Timing and Voltage Levels

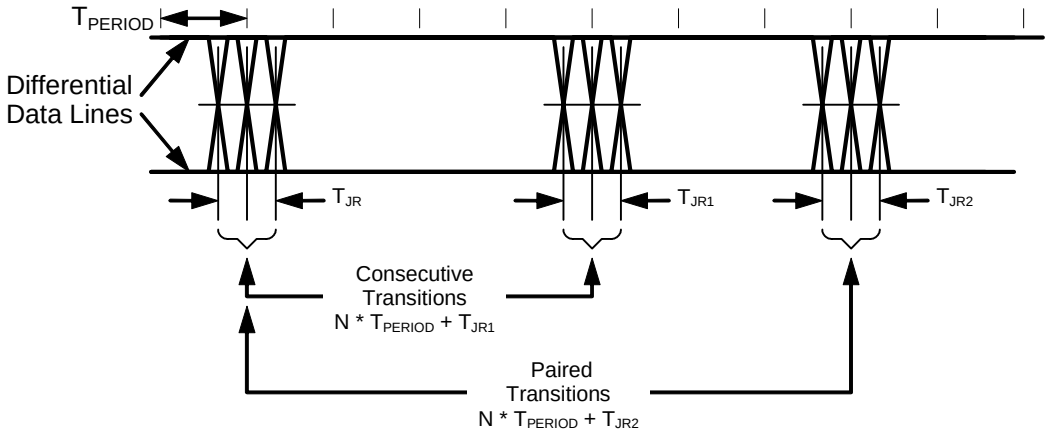


Figure 9-3. Receiver Jitter Tolerance

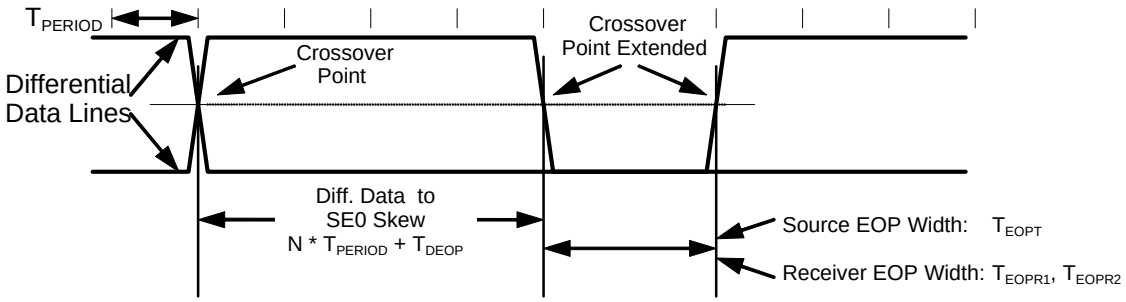


Figure 9-4. Differential to EOP Transition Skew and EOP Width

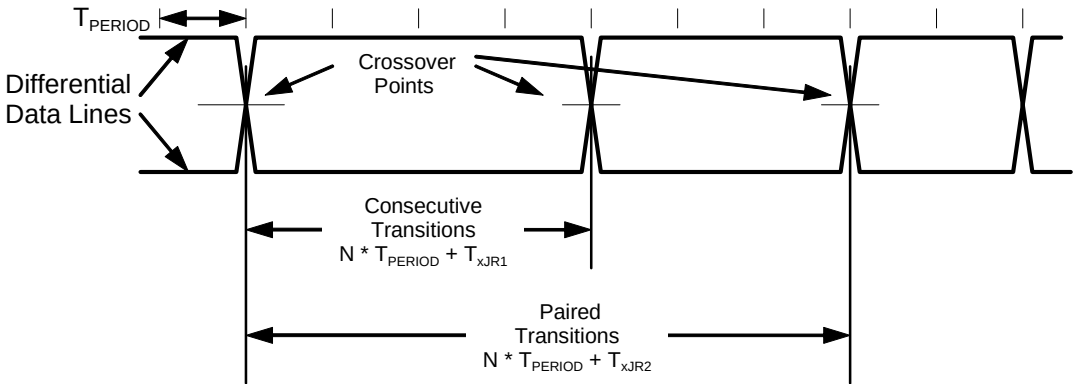
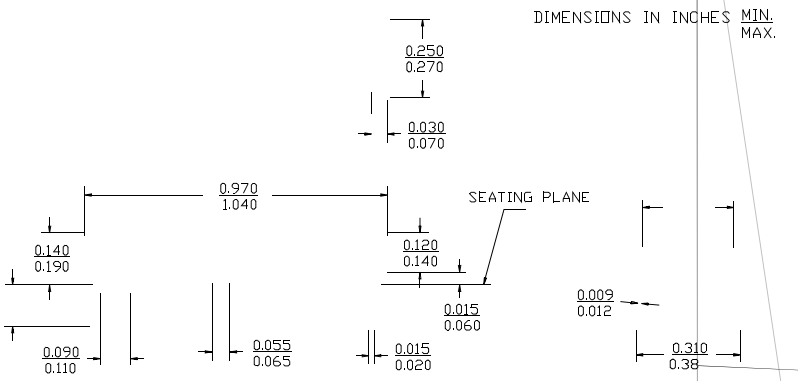


Figure 9-5. Differ ential Data Jitter

10.0 Ordering Information

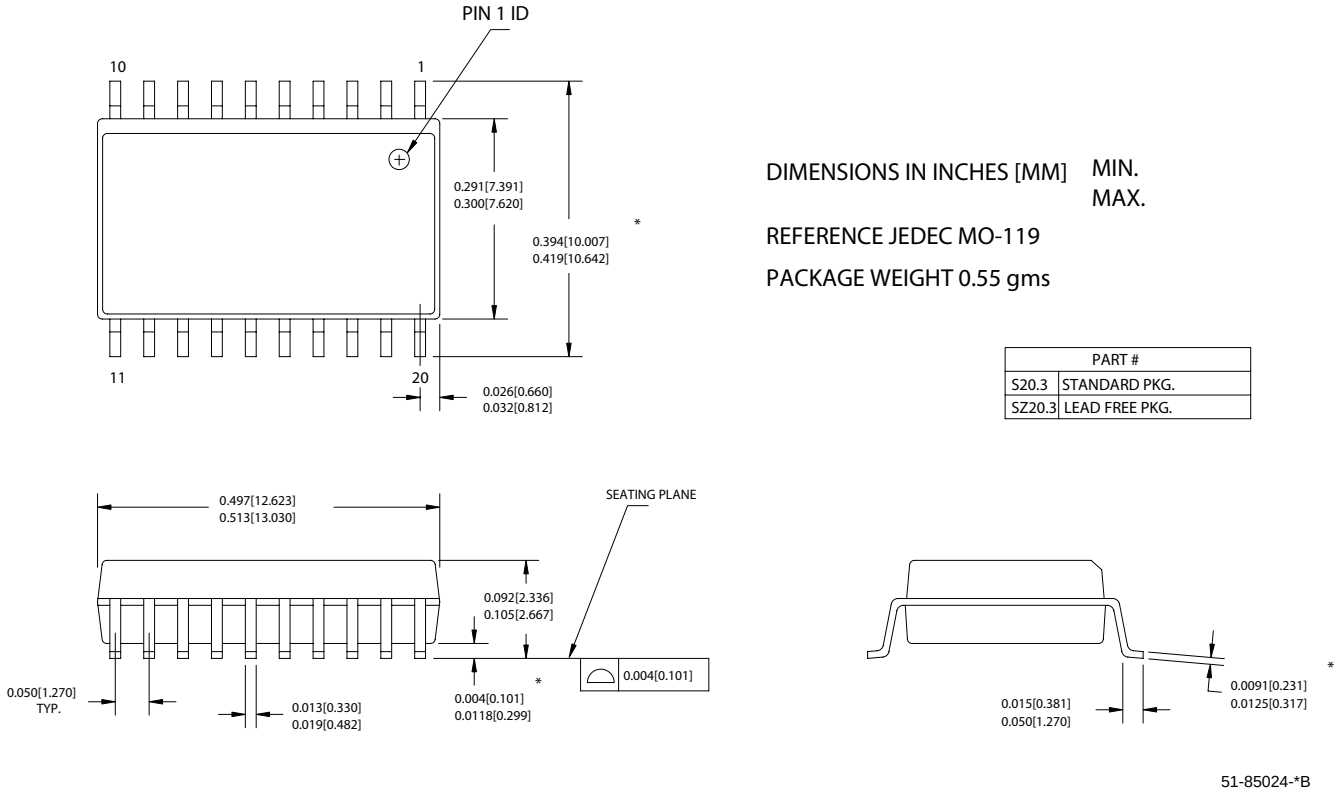
Ordering Code	EPROM Size	Number of GPIO	Package Name	Package Type	Operating Range
CY7C63001C-PXC	4KB	12	P5	20-Pin (300-Mil) PDIP Lead-free	Commercial
CY7C63001C-SXC	4KB	12	S5	20-Pin (300-Mil) SOIC Lead-free	Commercial
CY7C63001C-SXCT	4KB	12	S5	20-Pin (300-Mil) SOIC Lead-free Tape reel	Commercial
CY7C63101C-QXC	4KB	16	Q13	24-Pin (150-Mil) QSOP Lead-free	Commercial
CY7C63001C-XC	4KB	16	-	DIE Form Lead-free	Commercial

11.0 Package Diagrams



11.0 Package Diagrams (continued)

20-Lead (300-Mil) SOIC S5



DIMENSIONS IN INCHES [MM] MIN.
MAX.

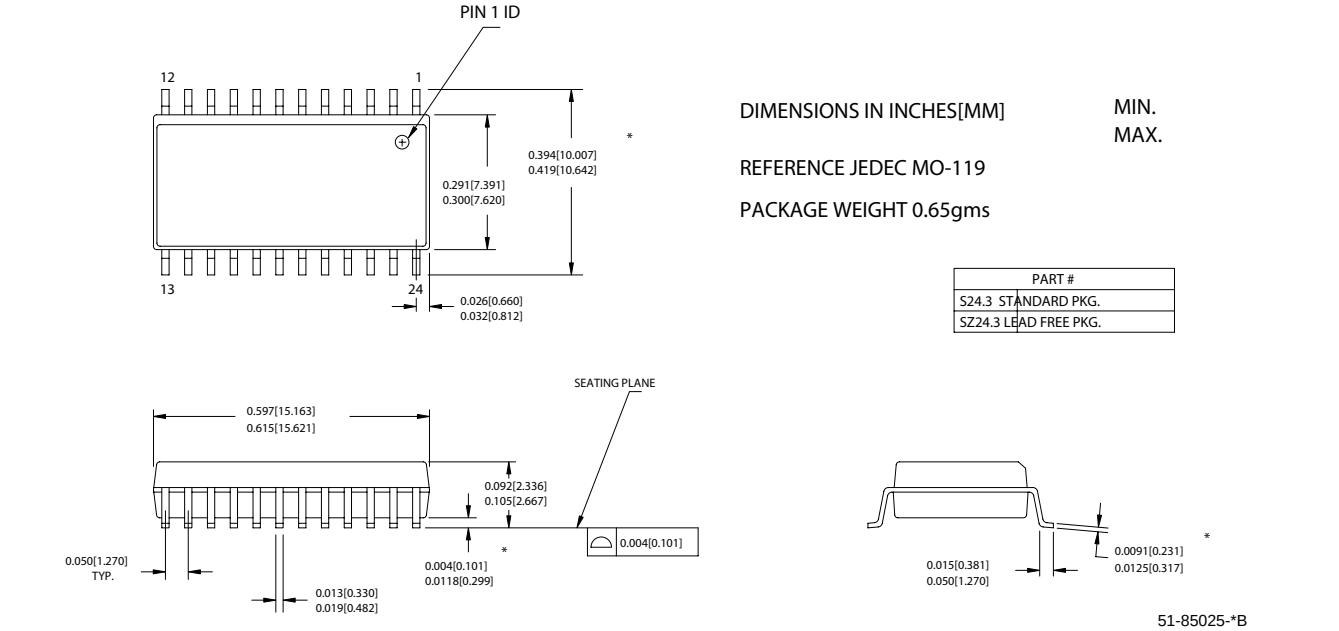
REFERENCE JEDEC MO-119

PACKAGE WEIGHT 0.55 gms

PART #	
S20.3	STANDARD PKG.
SZ20.3	LEAD FREE PKG.

51-85024-*B

24-Lead (300-Mil) SOIC S13



DIMENSIONS IN INCHES[MM] MIN.
MAX.

REFERENCE JEDEC MO-119

PACKAGE WEIGHT 0.65gms

PART #	
S24.3	STANDARD PKG.
SZ24.3	LEAD FREE PKG.

51-85025-*B

11.0 Package Diagrams (continued)

DIE FORM

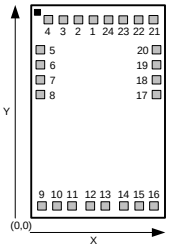


Table 11-1 below shows the die pad coordinates for the CY7C63001C-XC. The center location of each bond pad is relative to the bottom left corner of the die which has coordinate (0,0).

Table 11-1. CY7C63001C-XC Probe Pad Coordinates in microns ((0,0) to bond pad centers)

Pad #	Pin Name	X (microns)	Y (microns)	Pad #	Pin Name	X (microns)	Y (microns)
1	Port00	676.00	2325.40	13	Xtlout	794.85	121.80
2	Port01	507.35	2325.40	14	Vcc	1033.55	121.80
3	Port02	338.70	2325.40	15	D-	1129.75	121.80
4	Port03	170.05	2325.40	16	D+	1451.70	121.80
5	Port10	120.10	2132.30	17	Port17	1446.10	1595.80
6	Port12	120.10	1962.90	18	Port15	1446.10	1765.20
7	Port14	120.10	1765.20	19	Port13	1446.10	1962.90
8	Port16	120.10	1595.80	20	Port11	1446.10	2132.30
9	Vss	148.50	121.80	21	Port07	1395.65	2325.40
10	Vpp	278.30	121.80	22	Port06	1227.00	2325.40
11	Cext	414.25	121.80	23	Port05	1058.35	2325.40
12	Xtalin	653.45	121.80	24	Port04	889.7	2325.40

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Document History Page

Document Title: CY7C63001C, CY7C63101C Universal Serial Bus Microcontroller Document Number: 38-08026				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	116223	06/12/02	DSG	Change from Spec number: 38-00662 to 38-08026
*A	276070	See ECN	BON	Added die form and bond pad information. Added lead free packages. Removed obsolete packages and their references
*B	408068	See ECN	TYJ	128-ms timer interrupts corrected to 128- Rs interrupts Part Ordering information updated - Table 10.0. Type A updated with type C Data-sheet header changed to CY7C63001C, CY7C63101C