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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	M8A
Program Memory Type	OTP (4kB)
Controller Series	CY7C630xx
RAM Size	128 x 8
Interface	USB
Number of I/O	12
Voltage - Supply	4V ~ 5.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c63001c-sxct

4.0 Pin Definitions (continued)

Name	I/O	20-Pin	24-pin	Die Pad #	Description
CEXT	I/O	9	11	11	Connects to external R/C timing circuit for optional 'suspend' wakeup
D+	I/O	14	16	16	USB data+
D–	I/O	13	15	15	USB data–
V_{PP}	–	8	10	10	Programming voltage supply, tie to ground during normal operation
V_{CC}	–	12	14	14	Voltage supply
V_{SS}	–	7	9	9	Ground

5.0 Pin Description

Name	Description
V_{CC}	1 pin. Connects to the USB power source or to a nominal 5V power supply. Actual V_{CC} range can vary between 4.0V and 5.25V.
V_{SS}	1 pin. Connects to ground.
V_{PP}	1 pin. Used in programming the on-chip EPROM. This pin should be tied to ground during normal operations.
XTALIN	1 pin. Input from an external ceramic resonator.
XTALOUT	1 pin. Return path for the ceramic resonator (leave unconnected if driving XTALIN from an external oscillator).
P0.0–P0.7, P1.0–P1.7	16 pins. P0.0–P0.7 are the 8 I/O lines in Port 0. P1.0–P1.7 are the 8 I/O lines in Port 1. P1.0–P1.3 are supported in the CY7C63001C. All I/O pins include bit-programmable pull-up resistors. However, the sink current of each pin can be programmed to one of sixteen levels. Besides functioning as GPIO lines, each pin can be programmed as an interrupt input. The interrupt is edge-triggered, with programmable polarity.
D+, D–	2 pins. Bidirectional USB data lines. An external pull-up resistor must be connected between the D pin and V_{CC} to select low-speed USB operation.
CEXT	1 pin. Open-drain output with Schmitt trigger input. The input is connected to a rising edge-triggered interrupt. CEXT may be connected to an external RC to generate a wake-up from Suspend mode. See Section 6.4.

6.0 Functional Description

The Cypress CY7C630/101C USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, joystick, and gamepad. These USB microcontrollers conform to the low-speed (1.5 Mbps) requirements of the USB specification version 1.1. Each microcontroller is a self-contained unit with: a USB interface engine, USB transceivers, an 8-bit RISC microcontroller, a clock oscillator, timers, and program memory. Each microcontroller supports one USB device address and two endpoints.

The 6-MHz clock is doubled to 12 MHz to drive the microcontroller. A RISC architecture with 35 instructions provides the best balance between performance and product cost.

6.1 Memory Organization

The memory in the USB Controller is organized into user program memory in EPROM space and data memory in SRAM space.
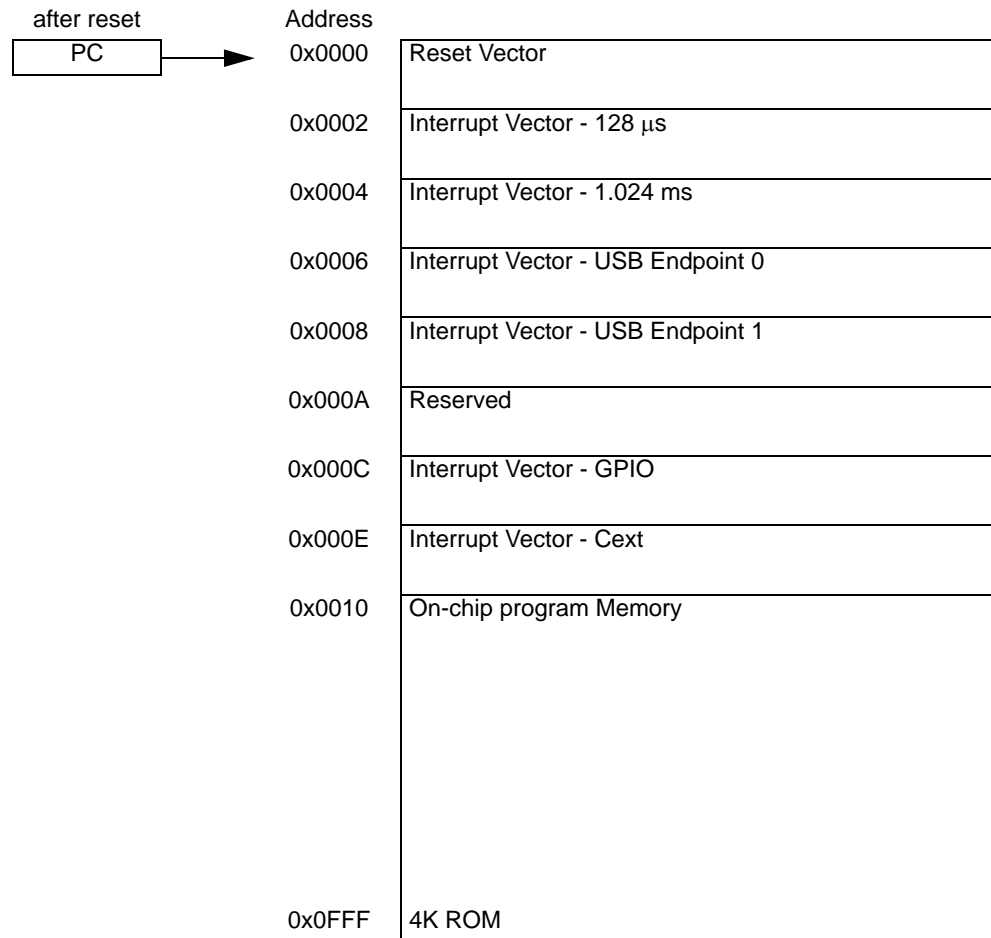
6.1.1 Program Memory Organization

The CY7C63001C and CY7C63101C each offer 4 Kbytes of EPROM. The program memory space is divided into two functional groups: interrupt vectors and program code.

The interrupt vectors occupy the first 16 bytes of the program space. Each vector is 2 bytes long. After a reset, the Program Counter points to location zero of the program space. *Figure 6-1* shows the organization of the Program Memory Space.

6.1.2 Security Fuse Bit

The Cypress USB microcontroller includes a security fuse bit. When the security fuse is programmed, the EPROM program memory outputs 0xFF to the EPROM programmer, thus protecting the user's code.

Figure 6-1. Program Memory Space

6.1.3 Data Memory Organization

The USB Controller includes 128 bytes of data RAM. The upper 16 bytes of the data memory are used as USB FIFOs for Endpoint 0 and Endpoint 1. Each endpoint is associated with an 8-byte FIFO.

The USB controller includes two pointers into data RAM, the Program Stack Pointer (PSP) and the Data Stack Pointer (DSP). The value of PSP after reset is 0x00. The PSP increments by 2 whenever a CALL instruction is executed and it decrements by 2 whenever a RET instruction is used.

The DSP pre-decrements by 1 whenever a PUSH instruction is executed and it increments by 1 after a POP instruction is used. The default value of the DSP after reset is 0x00, which would cause the first PUSH to write into USB FIFO space for Endpoint 1. Therefore, the DSP should be mapped to a location such as 0x70 before initiating any data stack operations. Refer to the Reset section for more information about DSP remapping after reset. *Figure 6-2* illustrates the Data Memory Space.
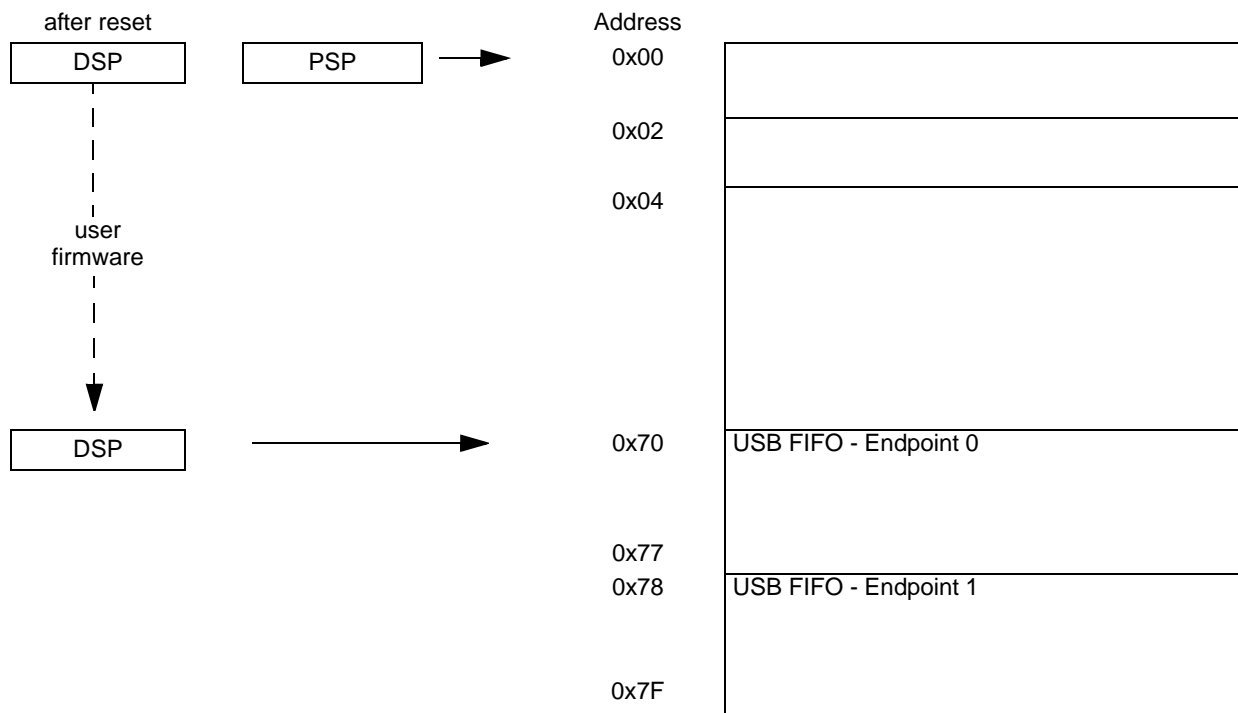
Figure 6-2. Data Memory Space

6.2 I/O Register Summary

I/O registers are accessed via the I/O Read (IORD) and I/O Write (IOWR, IOWX) instructions.

Table 6-1. I/O Register Summary

Register Name	I/O Address	Read/Write	Function	Page
P0 Data	0x00	R/W	General purpose I/O Port (low current)	9
P1 Data	0x01	R/W	General purpose I/O Port (high current)	9
P0 IE	0x04	W	Interrupt enable for Port 0 pins	12
P1 IE	0x05	W	Interrupt enable for Port 1 pins	12
P0 Pull-up	0x08	W	Pull-up resistor control for Port 0 pins	10
P1 Pull-up	0x09	W	Pull-up resistor control for Port 1 pins	10
EP0 TX Config.	0x10	R/W	USB Endpoint 0 transmit configuration	15
EP1 TX Config.	0x11	R/W	USB Endpoint 1 transmit configuration	15
USB DA	0x12	R/W	USB device address	14
USB SCR	0x13	R/W	USB status and control	16
EP0 RX Status	0x14	R/W	USB Endpoint 0 receive status	14
GIE	0x20	R/W	Global Interrupt Enable	11
WDT	0x21	W	Watch Dog Timer clear	7
Cext	0x22	R/W	External R-C Timing circuit control	8
Timer	0x23	R	Free-running timer	8
P0 Isink	0x30-0x37	W	Input sink current control for Port 0 pins. There is one Isink register for each pin. Address of the Isink register for pin 0 is located at 0x30 and the register address for pin 7 is located at 0x37.	10
P1 Isink	0x38-0x3F	W	Input sink current control for Port 1 pins. There is one Isink register for each pin. Address of the Isink register for pin 0 is located at 0x38 and the register address for pin 7 is located at 0x3F. The number of Port 1 pins depends on package type.	10
SCR	0xFF	R/W	Processor status and control register	7

6.3 Reset

The USB Controller supports three types of resets. All registers are restored to their default states during a reset. The USB Device Address is set to 0 and all interrupts are disabled. In addition, the Program Stack Pointer (PSP) is set to 0x00 and the Data Stack Pointer (DSP) is set to 0x00. The user should set the DSP to a location such as 0x70 to reserve 16 bytes of USB FIFO space. The assembly instructions to do so are:

    MOV A, 70h   ; Move 70 hex into Accumulator, use 70
    instead of 6F because the dsp is
                    ; always decremented by 1 before the
    data transfer of the PUSH instruction occurs
    SWAP A, DSP   ; Move Accumulator value into dsp

The three reset types are:

1. Power-On Reset (POR)

2. Watch Dog Reset (WDR)

3. USB Reset

The occurrence of a reset is recorded in the Status and Control Register located at I/O address 0xFF (*Figure 6-3*). Reading

and writing this register are supported by the IORD and IOWR instructions. Bits 1, 2, and 7 are reserved and must be written as zeros during a write. During a read, reserved bit positions should be ignored. Bits 4, 5, and 6 are used to record the occurrence of POR, USB, and WDR Reset respectively. The firmware can interrogate these bits to determine the cause of a reset. If a Watch Dog Reset occurs, firmware must clear the WDR bit (bit 6) in the Status and Control Register to re-enable the USB transmitter (please refer to the Watch Dog Reset section for further details). Bit 0, the "Run" control, is set to 1 at POR. Clearing this bit stops the microcontroller (firmware normally should not clear this bit). Once this bit is set to LOW, only a reset can set this bit HIGH.

The microcontroller resumes execution from ROM address 0x00 after a reset unless the Suspend bit (bit 3) of the Status and Control Register is set. Setting the Suspend bit stops the clock oscillator and the interrupt timers and powers down the microcontroller. The detection of any USB activity, the occurrence of a GPIO Interrupt, or the occurrence of the Cext Interrupt terminates the suspend condition.

b7	b6	b5	b4	b3	b2	b1	b0
Reserved	WDR	USBR	POR	SUSPEND	Reserved	Reserved	RUN
	R/W	R/W	R/W	R/W			R/W
0	0	0	1	0	0	0	1

Figure 6-3. Status and Control Register (SCR - Address 0xFF)

6.3.1 Power-On Reset (POR)

Power-On Reset (POR) occurs every time the power to the device is switched on. Bit 4 of the Status and Control Register is set to record this event (the register contents are set to 00011001 by the POR). The USB Controller is placed in suspended mode at the end of POR to conserve power (the clock oscillator, the timers, and the interrupt logic are turned off in suspend mode). After POR, only a non-idle USB Bus state terminates the suspend mode. The microcontroller then begins execution from ROM address 0x00.

6.3.2 Watch Dog Reset (WDR)

The Watch Dog Timer Reset (WDR) occurs when the Most Significant Bit of the 4-bit Watch Dog Timer Register transitions from LOW to HIGH. Writing any value to the write-only Watch Dog Restart Register at 0x21 clears the timer (firmware should periodically write to the Watch Dog Restart Register in the 'main loop' of firmware). The Watch Dog timer is clocked by a 1.024-ms clock from the free-running timer. If 8 clocks occur between writes to the timer, a WDR occurs and bit 6 of the Status and Control Register is set to record the event. A Watch Dog Timer Reset lasts for 8.192 ms, at which time the microcontroller begins execution at ROM address 0x00. The USB transmitter is disabled by a Watch Dog Reset because the USB Device Address Register is cleared (otherwise, the USB Controller would respond to all address 0 transactions). The transmitter remains disabled until the WDR bit (bit 6) in the Status and Control Register is reset to 0 by firmware.

6.3.3 USB Bus Reset

The USB Controller recognizes a USB Reset when a Single Ended Zero (SE0) condition persists for at least 8–16 μs (the Reset may be recognized for an SE0 as short as 8 μs, but it is always recognized for an SE0 longer than 16 μs). SE0 is the condition in which both the D+ line and the D– line are LOW. Bit 5 of the Status and Control Register is set to record this event. If the USB reset happens while the device is suspended, the suspend condition is cleared and the clock oscillator is restarted. However, the microcontroller is not released until the USB reset is removed.

6.4 Instant-on Feature (Suspend Mode)

The USB Controller can be placed in a low-power state by setting the Suspend bit (bit 3) of the Status and Control register. All logic blocks in the device are turned off except the USB receiver, the GPIO interrupt logic, and the Cext interrupt logic. The clock oscillator and the free-running and watch dog timers are shut down.

The suspend mode is terminated when one of the following three conditions occur:

1. USB activity

2. A GPIO interrupt

3. Cext interrupt

The clock oscillator, GPIO, and timers restart immediately upon exiting suspend mode. The USB engine and microcontroller return to a fully functional state no more than 256 μs later. Before servicing any interrupt requests, the microcontroller executes the instruction following the I/O write that placed the device into suspend mode.

Both the GPIO interrupt and the Cext interrupt allow the USB Controller to wake-up periodically and poll potentiometers, optics, and other system components while maintaining a very low average power consumption. The Cext Interrupt is preferred for lowest power consumption.

For Cext to generate an "Instant-on" interrupt, the pin must be connected to ground with an external capacitor and connected to V_{CC} with an external resistor. A "0" is written to the Cext register located at I/O address 0x22 to discharge the capacitor. Then, a "1" is written to disable the open-drain output driver. A Schmitt trigger input circuit monitors the input and generates a wake-up interrupt when the input voltage rises above the input threshold. By changing the values of the external resistor and capacitor, the user can fine tune the charge rate of the R-C timing circuit. The format of the Cext register is shown in
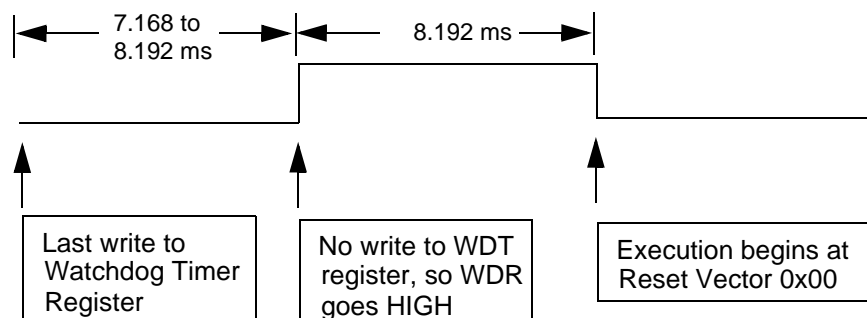
Figure 1. Watch Dog Reset (WDR)

6.6 General Purpose I/O Ports

Interface with peripherals is conducted via as many as 16 GPIO signals. These signals are divided into two ports: Port 0 and Port 1. Port 0 contains eight lines (P0.0–P0.7) and Port 1 contains up to eight lines (P1.0–P1.7). The number of external I/O pins depends on the package type. Both ports can be accessed by the IORD, IOWR, and IOWX instructions. The Port 0 data register is located at I/O address 0x00 while the Port 1 data register is located at I/O address 0x01. The contents of both registers are set HIGH during a reset. Refer to *Figures 6-7* and *6-8* for the formats of the data registers. In addition to supporting general input/output functions, each I/O line can trigger an interrupt to the microcontroller. Please refer to the interrupt section for more details.

Each GPIO line includes an internal R_{up} resistor. This resistor provides both the pull-up function and slew control. Two factors govern the enabling and disabling of each resistor: the state of its associated Port Pull-up register bit and the state of the Data Register bit. NOTE: The control bits in the Port Pull-up register are active LOW.

A GPIO line is HIGH when a "1" is written to the Data Register and a "0" is written to the respective Port Pull-up register. Writing a "0" to the port Data Register disables the port's Pull-up resistor and outputs a LOW on the GPIO line regardless of the setting in the Port Pull-up Register. The output goes to a high-Z state if the Data Register bit and the Port Pull-up Register bit are both "1". *Figure 6-9* illustrates the block diagram of one I/O line. The Port Isink Register is used to control the output current level and it is described later in this section. NOTE: The Isink logic block is turned off during suspend mode (please refer to the Instant-on Feature section for more details). Therefore, to prevent higher I_{CC} currents during USB suspend mode, firmware must set ALL Port 0 and Port 1 Data Register bits (which are not externally driven to a known state), **including those that are not bonded out on a particular package**, to "1" and all Port 0 and Port 1 Pull-Up Register data bits to "0" to enable port pull-ups before setting the Suspend bit (bit 3 of the Status and Control Register). *Table 6-2* is the Output Control truth table.

b7	b6	b5	b4	b3	b2	b1	b0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

Figure 6-7. Port 0 Data Register (Address 0x00)

b7	b6	b5	b4	b3	b2	b1	b0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

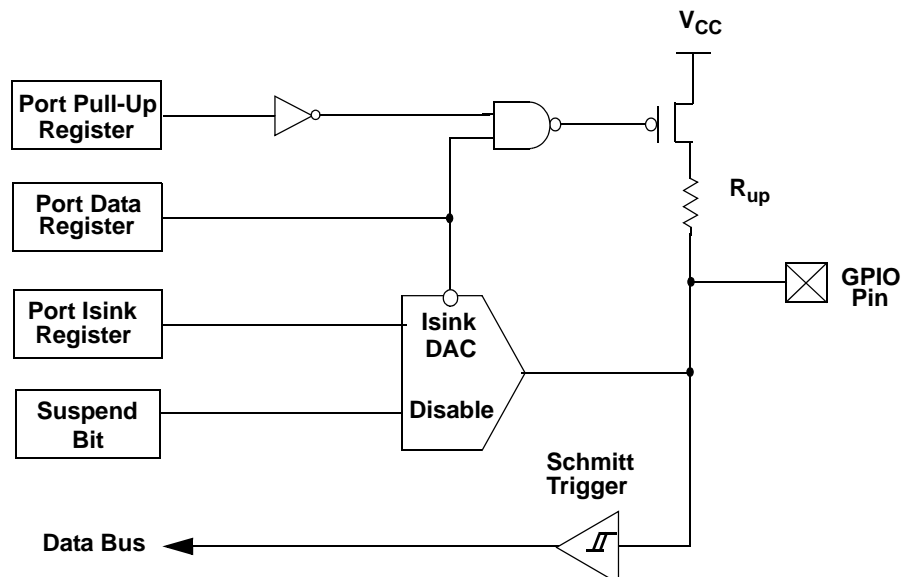**Figure 6-8. Port 1 Data Register (Address 0x01)**

Figure 6-9. Block Diagram of an I/O Line

Table 6-2. Output Control Truth Table

Data Register	Port Pull-up Register	Output at I/O Pin	Interrupt Polarity
0	0	Sink Current ('0')	High to Low
0	1	Sink Current ('0')	Low to High
1	0	Pull-up Resistor ('1')	High to Low
1	1	Hi-Z	Low to High

To configure a GPIO pin as an input, a "1" should be written to the Port Data Register bit associated with that pin to disable the pull-down function of the Isink DAC (see *Figure 6-9*).When the Port Data Register is read, the bit value is a "1" if the voltage on the pin is greater than the Schmitt trigger threshold, or "0" if it is below the threshold. In applications where an internal pull-up is required, the R_{up} pull-up resistor can be engaged by writing a "0" to the appropriate bit in the Port Pull-up Register.

Both Port 0 and Port 1 Pull-up Registers are write only (see *Figures 6-10* and *6-11*). The Port 0 Pull-up Register is located at I/O address 0x08 and Port 1 Pull-up Register is mapped to address 0x09. The contents of the Port Pull-up Registers are cleared during reset, allowing the outputs to be controlled by the state of the Data Registers. The Port Pull-up Registers also select the polarity of transition that generates a GPIO interrupt. A "0" selects a HIGH to LOW transition while a "1" selects a LOW to HIGH transition.

Writing a "0" to the Data Register drives the output LOW. Instead of providing a fixed output drive, the USB Controller allows the user to select an output sink current level for each I/O pin. The sink current of each output is controlled by a dedicated Port Isink Register. The lower four bits of this register contain a code selecting one of sixteen sink current levels. The upper four bits of the register are ignored. The format of the Port Isink Register is shown in *Figure 6-12*.

Port 0 is a low-current port suitable for connecting photo transistors. Port 1 is a high current port capable of driving LEDs. See section 8.0 for current ranges. 0000 is the lowest drive strength. 1111 is the highest.

The write-only sink current control registers for Port 0 outputs are assigned from I/O address 0x30 to 0x37 with the control bits for P00 starting at 0x30. Port 1 sink current control registers are assigned from I/O address 0x38 to 0x3F with the control bits for P10 starting at 0x38. All sink current control registers are cleared during a reset, resulting in the minimum current sink setting.

b7	b6	b5	b4	b3	b2	b1	b0
PULL0.7	PULL0.6	PULL0.5	PULL0.4	PULL0.3	PULL0.2	PULL0.1	PULL0.0
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0

Figure 6-10. Port 0 Pull-up Register (Address 0x08)

b7	b6	b5	b4	b3	b2	b1	b0
PULL1.7	PULL1.6	PULL1.5	PULL1.4	PULL1.3	PULL1.2	PULL1.1	PULL1.0
W	W	W	W	W	W	W	W
0x	0	0	0	0	0	0	0

Figure 6-11. Port 1 Pull-up Register (Address 0x09)

b7	b6	b5	b4	b3	b2	b1	b0
Reserved	Reserved	Reserved	UNUSED	ISINK3	ISINK2	ISINK1	ISINK0
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 6-12. Port Isink Register for One GPIO Line
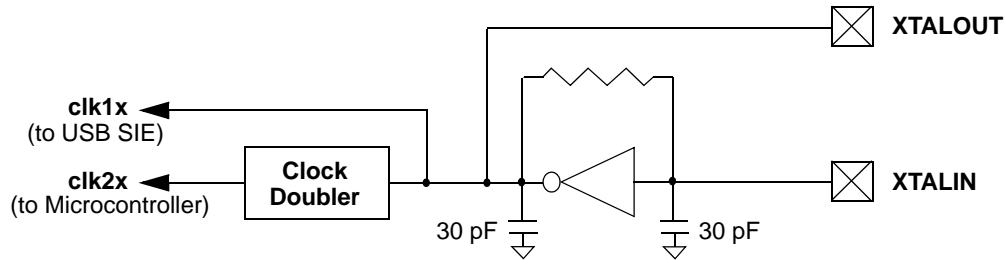
Figure 2. Clock Oscillator On-chip Circuit

6.7 XTALIN/XTALOUT

The XTALIN and XTALOUT pins support connection of a 6-MHz ceramic resonator. The feedback capacitors and bias resistor are internal to the IC, as shown in *Figure 2* Leave XTALOUT unconnected when driving XTALIN from an external oscillator.
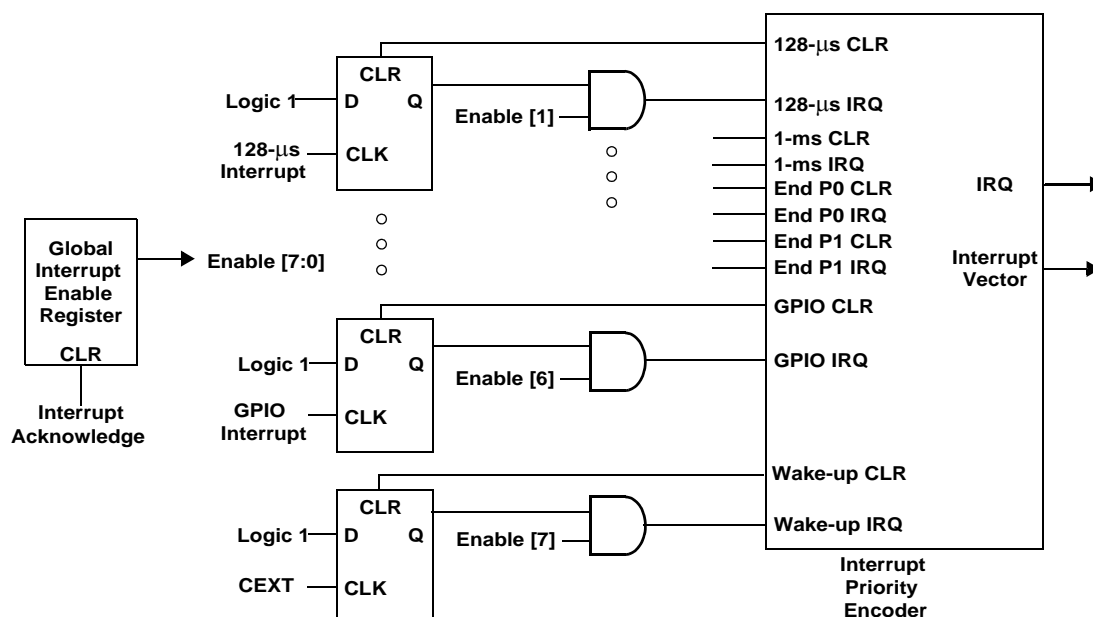
6.8 Interrupts

Interrupts are generated by the General Purpose I/O lines, the Cext pin, the internal timer, and the USB engine. All interrupts are maskable by the Global Interrupt Enable Register. Access to this register is accomplished via IORD, IOWR, and IOWX instructions to address 0x20. Writing a "1" to a bit position enables the interrupt associated with that position. During a reset, the contents of the Interrupt Enable Register are cleared, disabling all interrupts. *Figure 6-13* illustrates the format of the Global Interrupt Enable Register.

The interrupt controller contains a separate latch for each interrupt. See *Figure 3* for the logic block diagram for the interrupt controller. When an interrupt is generated, it is latched as a pending interrupt. It stays as a pending interrupt until it is serviced or a reset occurs. A pending interrupt only generates an interrupt request if it is enabled in the Global Interrupt Enable Register. The highest priority interrupt request is serviced following the execution of the current instruction.

When servicing an interrupt, the hardware first disables all interrupts by clearing the Global Interrupt Enable Register. Next, the interrupt latch of the current interrupt is cleared. This is followed by a CALL instruction to the ROM address associated with the interrupt being serviced (i.e., the interrupt vector). The instruction in the interrupt table is typically a JMP instruction to the address of the Interrupt Service Routine (ISR). The user can re-enable interrupts in the interrupt service routine by writing to the appropriate bits in the Global Interrupt Enable Register. Interrupts can be nested to a level limited only by the available stack space.

b7	b6	b5	b4	b3	b2	b1	b0
CEXTIE	GPIOIE	Reserved	EP1IE	EP0IE	1024IE	128IE	Reserved
R/W	R/W		R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0

Figure 6-13. Global Interrupt Enable Register (GIER - Address 0x20)

Figure 3. Interrupt Controller Logic Block Diagram
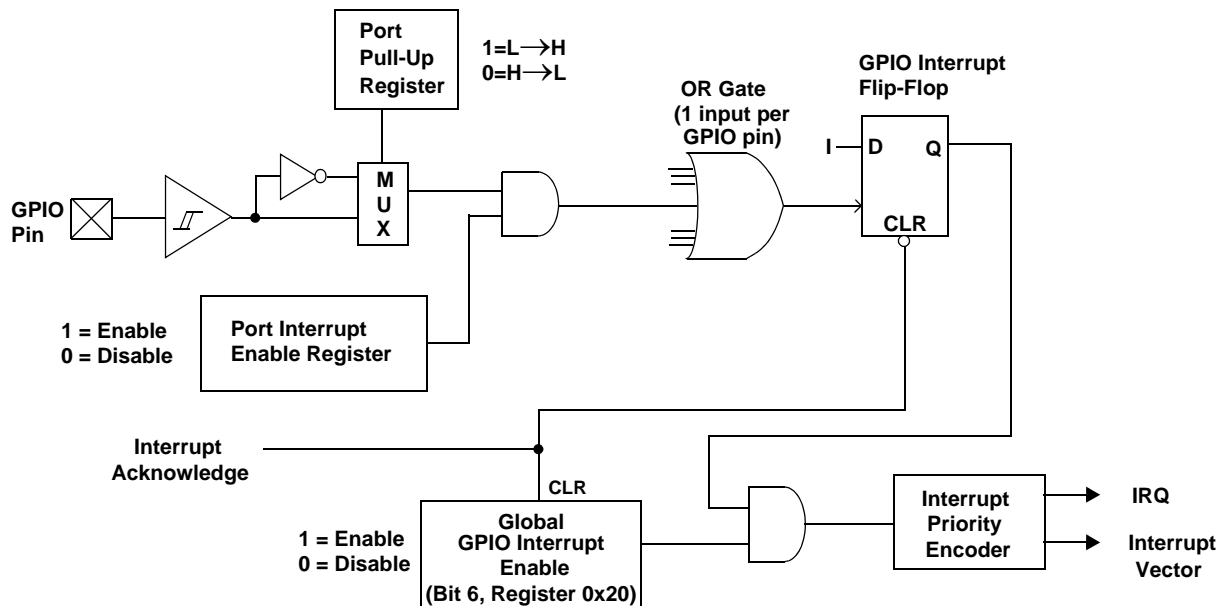
Figure 6-16. GPIO Interrupt Logic Block Diagram

Note: If one port pin triggers an interrupt, no other port pin can cause a GPIO interrupt until the port pin that triggered the interrupt has returned to its inactive (non-trigger) state or until its corresponding port interrupt enable bit is cleared (these events 'reset' the clock of the GPIO Interrupt flip-flop, which must be 'reset' to '0' before another GPIO interrupt event can 'clock' the GPIO Interrupt flip-flop and produce an IRQ).

Note: If the port pin that triggered an interrupt is held in its active (trigger) state while its corresponding port interrupt enable bit is cleared and then set, a GPIO interrupt event occurs as the GPIO Interrupt flip-flop clock transitions from '1' to '0' and then back to '1' (please refer to *Figure 6-16*). The USB Controller does not assign interrupt priority to different port pins and the Port Interrupt Enable Registers are not cleared during the interrupt acknowledge process. When a GPIO interrupt is serviced, the ISR must poll the ports to determine which pin caused the interrupt.

6.8.3   USB Interrupt

A USB Endpoint 0 interrupt is generated after the host has written data to Endpoint 0 or after the USB Controller has transmitted a packet from Endpoint 0 and receives an ACK from the host. An OUT packet from the host which is NAKed by the USB Controller does not generate an interrupt. This interrupt is masked by the USB EP0 Interrupt Enable bit (bit 3) of the Global Interrupt Enable Register.

A USB Endpoint 1 interrupt is generated after the USB Controller has transmitted a packet from Endpoint 1 and has received an ACK from the host. This interrupt is masked by the USB EP1 Interrupt Enable bit (bit 4) of the Global Interrupt Enable Register.

6.8.4   Timer Interrupt

There are two timer interrupts: the 128-μs interrupt and the 1.024-ms interrupt. They are masked by bits 1 and 2 of the Global Interrupt Enable Register respectively. The user should disable both timer interrupts before going into the suspend

mode to avoid possible conflicts from timer interrupts occurring just as suspend mode is entered.

6.8.5   Wake-Up Interrupt

A wake-up interrupt is generated when the Cext pin goes HIGH. This interrupt is latched in the interrupt controller. It can be masked by the Wake-up Interrupt Enable bit (bit 7) of the Global Interrupt Enable Register. This interrupt can be used to perform periodic checks on attached peripherals when the USB Controller is placed in the low-power suspend mode. See the Instant-On Feature section for more details.

6.9   USB Engine

The USB engine includes the Serial Interface Engine (SIE) and the low-speed USB I/O transceivers. The SIE block performs most of the USB interface functions with only minimal support from the microcontroller core. Two endpoints are supported. Endpoint 0 is used to receive and transmit control (including setup) packets while Endpoint 1 is only used to transmit data packets.

The USB SIE processes USB bus activity at the transaction level independently. It does all the NRZI encoding/decoding and bit stuffing/unstuffing. It also determines token type, checks address and endpoint values, generates and checks CRC values, and controls the flow of data bytes between the bus and the Endpoint FIFOs. NOTE: the SIE stalls the CPU for 3 cycles per byte when writing data to the endpoint FIFOs (or 3 * 1/12 MHz * 8 bytes = 2 μs per 8-byte transfer).

The firmware handles higher level and function-specific tasks. During control transfers the firmware must interpret device requests and respond correctly. It also must coordinate Suspend/Resume, verify and select DATA toggle values, and perform function specific tasks.

The USB engine and the firmware communicate though the Endpoint FIFOs, USB Endpoint interrupts, and the USB registers described in the sections below.

b7	b6	b5	b4	b3	b2	b1	b0
Reserved	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 6-17. USB Device Address Register (USB DA - Address 0x12)

6.9.1   USB Enumeration Process

The USB Controller provides a USB Device Address Register at I/O location 0x12. Reading and writing this register is achieved via the IORD and IOWR instructions. The register contents are cleared during a reset, setting the USB address of the USB Controller to 0. *Figure 6-17* shows the format of the USB Address Register.

Typical enumeration steps:

1. The host computer sends a SETUP packet followed by a DATA packet to USB address 0 requesting the Device descriptor.
2. The USB Controller decodes the request and retrieves its Device descriptor from the program memory space.
3. The host computer performs a control read sequence and the USB Controller responds by sending the Device descriptor over the USB bus.
4. After receiving the descriptor, the host computer sends a SETUP packet followed by a DATA packet to address 0 assigning a new USB address to the device.
5. The USB Controller stores the new address in its USB Device Address Register after the no-data control sequence completes.
6. The host sends a request for the Device descriptor using the new USB address.
7. The USB Controller decodes the request and retrieves the Device descriptor from the program memory.
8. The host performs a control read sequence and the USB Controller responds by sending its Device descriptor over the USB bus.
9. The host generates control reads to the USB Controller to request the Configuration and Report descriptors.
10. The USB Controller retrieves the descriptors from its program space and returns the data to the host over the USB.
11. Enumeration is complete after the host has received all the descriptors.

6.9.2   Endpoint 0

All USB devices are required to have an endpoint number 0 that is used to initialize and manipulate the device. Endpoint 0

provides access to the device's configuration information and allows generic USB status and control accesses.

Endpoint 0 can receive and transmit data. Both receive and transmit data share the same 8-byte Endpoint 0 FIFO located at data memory space 0x70 to 0x77. Received data may overwrite the data previously in the FIFO.

6.9.2.1   Endpoint 0 Receive

After receiving a packet and placing the data into the Endpoint 0 FIFO, the USB Controller updates the USB Endpoint 0 RX register to record the receive status and then generates a USB Endpoint 0 interrupt. The format of the Endpoint 0 RX Register is shown in *Figure 6-18*.

This is a read/write register located at I/O address 0x14. Any write to this register clears all bits except bit 3 which remains unchanged. All bits are cleared during reset.

Bit 0 is set to 1 when a SETUP token for Endpoint 0 is received. Once set to a 1, this bit remains HIGH until it is cleared by an I/O write or a reset. While the data following a SETUP is being received by the USB engine, this bit is not cleared by an I/O write. User firmware writes to the USB FIFOs are disabled when bit 0 is set. This prevents SETUP data from being overwritten.

Bits 1 and 2 are updated whenever a valid token is received on Endpoint 0. Bit 1 is set to 1 if an OUT token is received and cleared to 0 if any other token is received. Bit 2 is set to 1 if an IN token is received and cleared to 0 if any other token is received.

Bit 3 shows the Data Toggle status of DATA packets received on Endpoint 0. This bit is updated for DATA following SETUP tokens and for DATA following OUT tokens if Stall (bit 5 of 0x10) is not set and either EnableOuts or StatusOuts (bits 3 and 4 of 0x13) are set.

Bits 4 to 7 are the count of the number of bytes received in a DATA packet. The two CRC bytes are included in the count, so the count value is two greater than the number of data bytes received. The count is always updated and the data is always stored in the FIFO for DATA packets following a SETUP token. The count for DATA following an OUT token is updated if Stall (bit 5 of 0x10) is 0 and either EnableOuts or StatusOuts (bits 3 and 4 of 0x13) are 1. The DATA following an OUT is written into the FIFO if EnableOuts is set to 1 and Stall and StatusOuts are 0.

b7	b6	b5	b4	b3	b2	b1	b0
COUNT3	COUNT2	COUNT1	COUNT0	TOGGLE	IN	OUT	SETUP
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 6-18. USB Endpoint 0 RX Register (Address 0x14)

6.10 USB Physical Layer Characteristics

The following section describes the CY7C630/101C compliance to the Chapter 7 Electrical section of the USB Specification, Revision 1.1. The section contains all signaling, power distribution, and physical layer specifications necessary to describe a low- speed USB function.

6.10.1 Low-Speed Driver Characteristics

The CY7C630/101C devices use a differential output driver to drive the Low-speed USB data signal onto the USB cable, as shown in *Figure 6-22*. The output swings between the differential HIGH and LOW state are well balanced to minimize signal skew. Slew rate control on the driver minimizes the radiated noise and cross talk on the USB cable. The driver's outputs support three-state operation to achieve bidirectional half duplex operation. The CY7C630/101C driver tolerates a voltage on the signal pins of –0.5V to 3.8V with respect to local ground reference without damage. The driver tolerates this voltage for 10.0 μs while the driver is active and driving, and tolerates this condition indefinitely when the driver is in its high-impedance state.

A low-speed USB connection is made through an unshielded, untwisted wire cable a maximum of 3 meters in length. The rise and fall time of the signals on this cable are well controlled to reduce RFI emissions while limiting delays, signaling skews and distortions. The CY7C630/101C driver reaches the specified static signal levels with smooth rise and fall times, resulting in minimal reflections and ringing when driving the USB cable. This cable and driver are intended to be used only on network segments between low-speed devices and the ports to which they are connected.

6.10.2 Receiver Characteristics

The CY7C630/101C has a differential input receiver which is able to accept the USB data signal. The receiver features an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8V to 2.5V with respect to its local ground reference. This is the common mode input voltage range. Proper data reception is also guaranteed when the differential data lines are outside the common mode range, as shown in *Figure 6-23*. The receiver tolerates static input voltages between –0.5V and 3.8V with respect to its local ground reference without damage. In addition to the differential receiver, there is a single-ended receiver for each of the two data lines. The single-ended receivers have a switching threshold between 0.8V and 2.0V (TTL inputs).
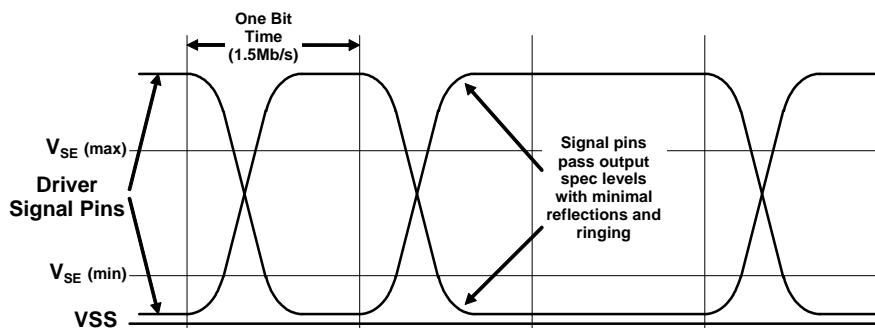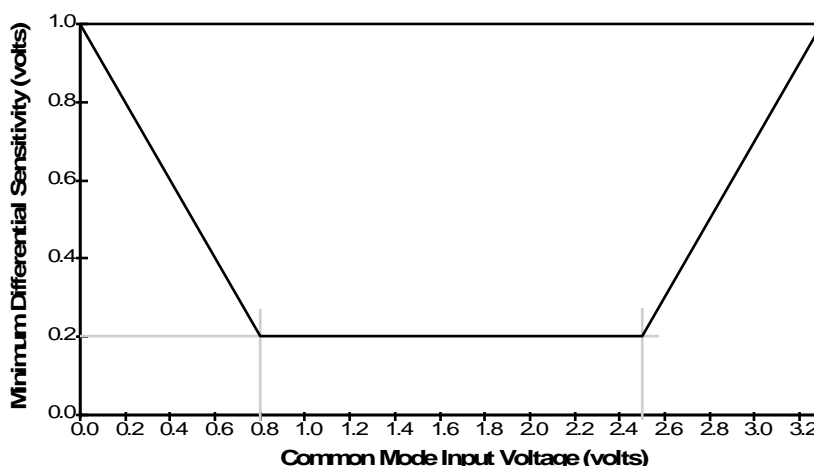

Figure 6-22. Low-speed Driver Signal Waveforms

Figure 6-23. Differential Input Sensitivity Over Entire Common Mode Range

6.12 Instruction Set Summary

Table 6-5. Instruction Set Map

MNEMONIC	operand	opcode	cycles		MNEMONIC	operand	opcode	cycles
HALT		00	7		NOP		20	4
ADD A,expr	data	01	4		INC A	acc	21	4
ADD A,[expr]	direct	02	6		INC X	x	22	4
ADD A,[X+expr]	index	03	7		INC [expr]	direct	23	7
ADC A,expr	data	04	4		INC [X+expr]	index	24	8
ADC A,[expr]	direct	05	6		DEC A	acc	25	4
ADC A,[X+expr]	index	06	7		DEC X	x	26	4
SUB A,expr	data	07	4		DEC [expr]	direct	27	7
SUB A,[expr]	direct	08	6		DEC [X+expr]	index	28	8
SUB A,[X+expr]	index	09	7		IORD expr	address	29	5
SBB A,expr	data	0A	4		IOWR expr	address	2A	5
SBB A,[expr]	direct	0B	6		POP A		2B	4
SBB A,[X+expr]	index	0C	7		POP X		2C	4
OR A,expr	data	0D	4		PUSH A		2D	5
OR A,[expr]	direct	OE	6		PUSH X		2E	5
OR A,[X+expr]	index	0F	7		SWAP A,X		2F	5
AND A,expr	data	10	4		SWAP A,DSP		30	5
AND A,[expr]	direct	11	6		MOV [expr],A	direct	31	5
AND A,[X+expr]	index	12	7		MOV [X+expr],A	index	32	6
XOR A,expr	data	13	4		OR [expr],A	direct	33	7
XOR A,[expr]	direct	14	6		OR [X+expr],A	index	34	8
XOR A,[X+expr]	index	15	7		AND [expr],A	direct	35	7
CMP A,expr	data	16	5		AND [X+expr],A	index	36	8
CMP A,[expr]	direct	17	7		XOR [expr],A	direct	37	7
CMP A,[X+expr]	index	18	8		XOR [X+expr],A	index	38	8
MOV A,expr	data	19	4		IOWX [X+expr]	index	39	6
MOV A,[expr]	direct	1A	5		CPL		3A	4
MOV A,[X+expr]	index	1B	6		ASL		3B	4
MOV X,expr	data	1C	4		ASR		3C	4
MOV X,[expr]	direct	1D	5		RLC		3D	4
IPRET	addr	1E	13		RRC		3E	4
XPAGE		1F	4		RET		3F	8
JMP	addr	8x	5		JC	addr	Cx	5
CALL	addr	9x	10		JNC	addr	Dx	5
JZ	addr	Ax	5		JACC	addr	Ex	7
JNZ	addr	Bx	5		INDEX	addr	Fx	14

7.0 Absolute Maximum Ratings

Storage Temperature ....−65°C to +150°C

Ambient Temperature with Power Applied ......−0°C to +70°C

Supply Voltage on V_{CC} Relative to V_{SS} .... −0.5V to +7.0V

DC Input Voltage..................................... −0.5V to +V_{CC}+0.5V

DC Voltage Applied to Outputs in High-Z state −0.5V to +V_{CC}+0.5V

Max. Output Current into Port 1 Pins ....60 mA

Max. Output Current into Non-Port 1 Pins .... 10 mA

Power Dissipation ....300 mW

Static Discharge Voltage ....>2000V

Latch-up Current[1]... >200 mA

8.0 Electrical Characteristics f_{OSC} = 6 MHz; Operating Temperature = 0 to 70°C, V_{CC} = 4.0 to 5.25 volts

	Parameter	Min	Max	Units	Conditions
	General				
I_{CC}	V_{CC} Operating Supply Current		25	mA	
I_{SB1}	Supply Current—Suspend Mode		20	μA	Resonator off, D− > Voh min[2]
I_{SB2}	Supply Current—Start-up Mode		4	mA	
V_{PP}	Programming Voltage (disabled)	−0.4	0.4	V	
t_{start}	Resonator Start-up Interval		256	μs	Ceramic resonator
t_{watch}	Watch Dog Timer Period	7.168	8.192	ms	
	Power On Reset				
t_{VCCS}	V_{CC} Slew	0.010	1000	ms	Linear ramp on V_{CC} pin to V_{CC}[3, 4]
	USB Interface				
V_{oh}	Static Output High	2.8	3.6	V	15kΩ ± 5% to Gnd[5,6]
V_{ol}	Static Output Low		0.3	V	See Notes 5 and 6
V_{di}	Differential Input Sensitivity	0.2		V	|(D+)−(D−)|, and *Figure 6-23*
V_{cm}	Differential Input Common Mode Range	0.8	2.5	V	*Figure 6-23*
V_{se}	Single Ended Receiver Threshold	0.8	2.0	V	
C_{in}	Transceiver Input Capacitance		20	pF	D+ to Vss; D- to Vss
I_{lo}	Data Line (D+, D−) Leakage	−10	10	μA	0 V <(D+, D−)<3.3 V, Hi-Z State
R_{pu1}	External Bus Pull-up Resistance, D− pin	1.425	1.575	kΩ	1.5 kΩ ± 5% to 3.3V supply
R_{pu2}	External Bus Pull-up Resistance, D− pin	7.425	7.575	kΩ	7.5 kΩ ± 1% to Vcc[7]
R_{pd}	External Bus Pull-down Resistance	14.25	15.75	kΩ	15 kΩ ± 5%

Notes:
1. All pins specified for >200 mA positive and negative injection, except P1.0 is specified for >50 mA negative injection.
2. Cext at V_{CC} or Gnd, Port 0 and Port1 at V_{CC}.
3. Part powers up in suspend mode, able to be reset by USB Bus Reset.
4. POR may re-occur whenever V_{CC} drops to approximately 2.5V.
5. Level guaranteed for range of V_{CC} = 4.35V to 5.25V.
6. With R_{pu1} of 1.5 KW±5% on D− to 3.3V regulator.
7. Maximum matched capacitive loading allowed on D+ and D− (including USB cable and host/hub) is approximately 230 pF.

8.0 Electrical Characteristics (continued) f_{OSC} = 6 MHz; Operating Temperature = 0 to 70°C, V_{CC} = 4.0 to 5.25 volts

Parameter		Min	Max	Units	Conditions
	General Purpose I/O Interface				
R_{up}	Pull-up Resistance	8	24	kΩ	
$I_{sink0(0)}$	Port 0 Sink Current (0), lowest current	0.1	0.3	mA	Vout = 2.0V DC, Port 0 only[5]
$I_{sink0(F)}$	Port 0 Sink Current (F), highest current	0.5	1.5	mA	Vout = 2.0V DC, Port 0 only[5]
$I_{sink1(0)}$	Port 1 Sink Current (0), lowest current	1.6	4.8	mA	Vout = 2.0V DC, Port 1 only[5]
$I_{sink1(F)}$	Port 1 Sink Current (F), highest current	8	24	mA	Vout = 2.0V DC, Port 1 only[5]
		5		mA	Vout = 0.4V DC, Port 1 only[5]
I_{range}	Sink Current max./min.	4.5	5.5		Vout = 2.0V DC, Port 0 or 1[5, 8]
I_{lin}	Differential Nonlinearity		0.5	I_{SB}	Port 0 or Port 1[9]
T_{ratio}	Tracking Ratio Port1 to Port0	14.4	19.6		Vout = 2.0V[10]
t_{sink}	Current Sink Response Time		0.8	μs	Full scale transition
I_{max}	Port 1 Max Sink Current		60	mA	Summed over all Port 1 bits
P_{max}	Port 1 & Cext Sink Mode Dissipation		25	mW	Per pin
V_{ith}	Input Threshold Voltage	45%	65%	V_{CC}	All ports and Cext[11]
V_H	Input Hysteresis Voltage	6%	12%	V_{CC}	Port 0 and Port 1[12]
V_{HCext}	Input Hysteresis Voltage, Cext	12%	30%	V_{CC}	Cext Pin Only[12]
Iin	Input Leakage Current, GPIO Pins	−1	1	μA	Port 0 and Port 1, Vout = 0 or V_{CC}[13]
I_{inCx}	Input Leakage Current, Cext Pin		50	nA	V_{Cext} = 0 or V_{CC}
I_{Cext}	Sink Current, Cext Pin	6	18	mA	V_{Cext} = V_{CC}
V_{ol1}	Output LOW Voltage, Cext Pin		0.4	V	V_{CC} = Min., I_{ol} = 2 mA
V_{ol2}	Output LOW Voltage, Cext Pin		2.0	V	V_{CC} = Min., I_{ol} = 5 mA

Notes:
8. I_{range} = $I_{sink(F)}$/$I_{sink(0)}$ for each port 0 or 1 output.
9. Measured as largest step size vs. nominal according to measured full scale and zero programmed values.
10. T_{ratio} = $I_{sink1(n)}$/$I_{sink0(n)}$ for the same n.
11. Low to High transition.
12. This parameter is guaranteed, but not tested.
13. With Ports configured in Hi-Z mode.

9.0 Switching Characteristics

| Parameter	Description	Min.	Max.	Unit	Conditions
	Clock				
t_{CYC}	Input Clock Cycle Time	166.67	166.67	ns	
t_{CH}	Clock HIGH Time	0.45 t_{CYC}		ns	
t_{CL}	Clock LOW Time	0.45 t_{CYC}		ns	
	USB Driver Characteristics				
t_r	USB Data Transition Rise Time	75	300	ns	See Notes 5, 6, and 14
t_f	USB Data Transition Fall Time	75	300	ns	See Notes 5, 6, and 14
t_{rfm}	Rise/Fall Time Matching	80	125	%	t_r/t_f
V_{crs}	Output Signal Crossover Voltage	1.3	2.0	V	See Note 5
	USB Data Timing				
t_{drate}	Low Speed Data Rate	1.4775	1.5225	Mb/s	Ave. Bit Rate (1.5 Mb/s ± 1.5%)
t_{djr1}	Receiver Data Jitter Tolerance	−75	75	ns	To Next Transition, *Figure 9-3*[15]
t_{djr2}	Receiver Data Jitter Tolerance	−45	45	ns	For Paired Transitions, *Figure 9-3*[15]
t_{deop}	Differential to EOP Transition Skew	−40	100	ns	*Figure 9-4*[15]
t_{eopr}	EOP Width at Receiver	670		ns	Accepts as EOP[15]
t_{lst}	Width of SE0 Interval During Differential Transition		210	ns	
t_{eopt}	Source EOP Width	1.25	1.50	µs	
t_{udj1}	Differential Driver Jitter	−95	95	ns	To next transition, *Figure 9-5*
t_{udj2}	Differential Driver Jitter	−150	150	ns	To paired transition, *Figure 9-5*

Notes:
14. C_{load} of 200 (75 ns) to 600 pF (300 ns).
15. Measured at crossover point of differential data signals.
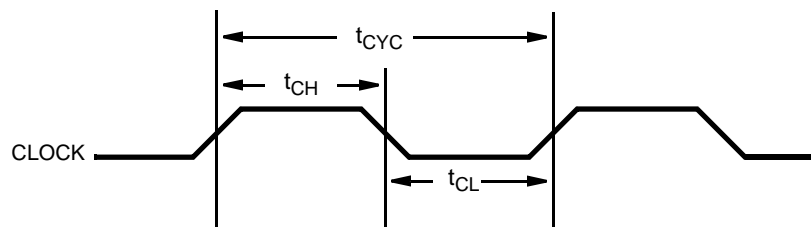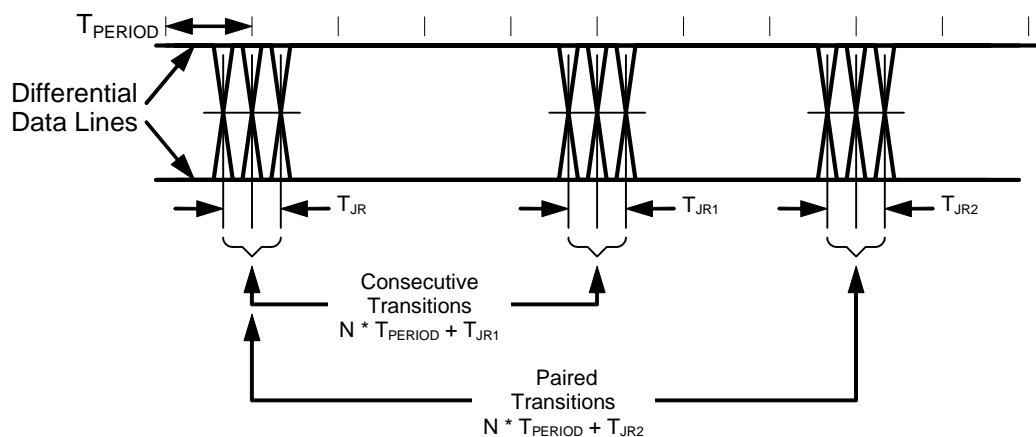
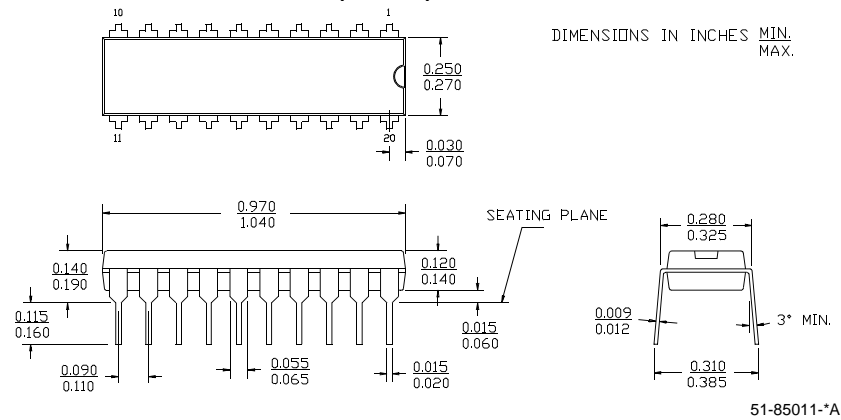**Figure 9-1. Clock Timing**
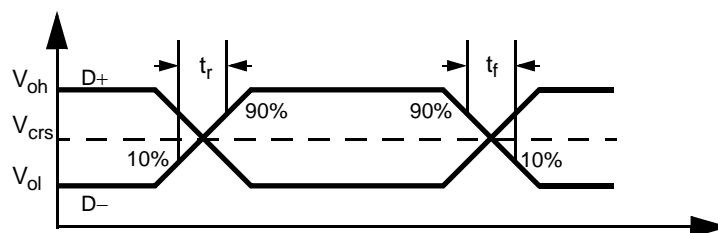
Figure 9-2. USB Data Signal Timing and Voltage Levels

Figure 9-3. Receiver Jitter Tolerance

11.0   Package Diagrams

20-Lead (300-Mil) Molded DIP P5

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

0.250 / 0.270

0.030 / 0.070

0.970 / 1.040

SEATING PLANE

0.140 / 0.190

0.120 / 0.140

0.115 / 0.160

0.015 / 0.060

0.090 / 0.110

0.055 / 0.065

0.015 / 0.020

0.280 / 0.325

0.009 / 0.012

3° MIN.

0.310 / 0.385

51-85011-*A

24-Lead Quarter Size Outline Q13

0.033 REF.

PIN 1 ID

0.150 / 0.157

0.228 / 0.244

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

0.337 / 0.344

SEATING PLANE

0.053 / 0.069

0.004

0.004 / 0.010

0.025 BSC.

0.008 / 0.012

0.007 / 0.010

0.016 / 0.034

0°-8°

51-85055-*B
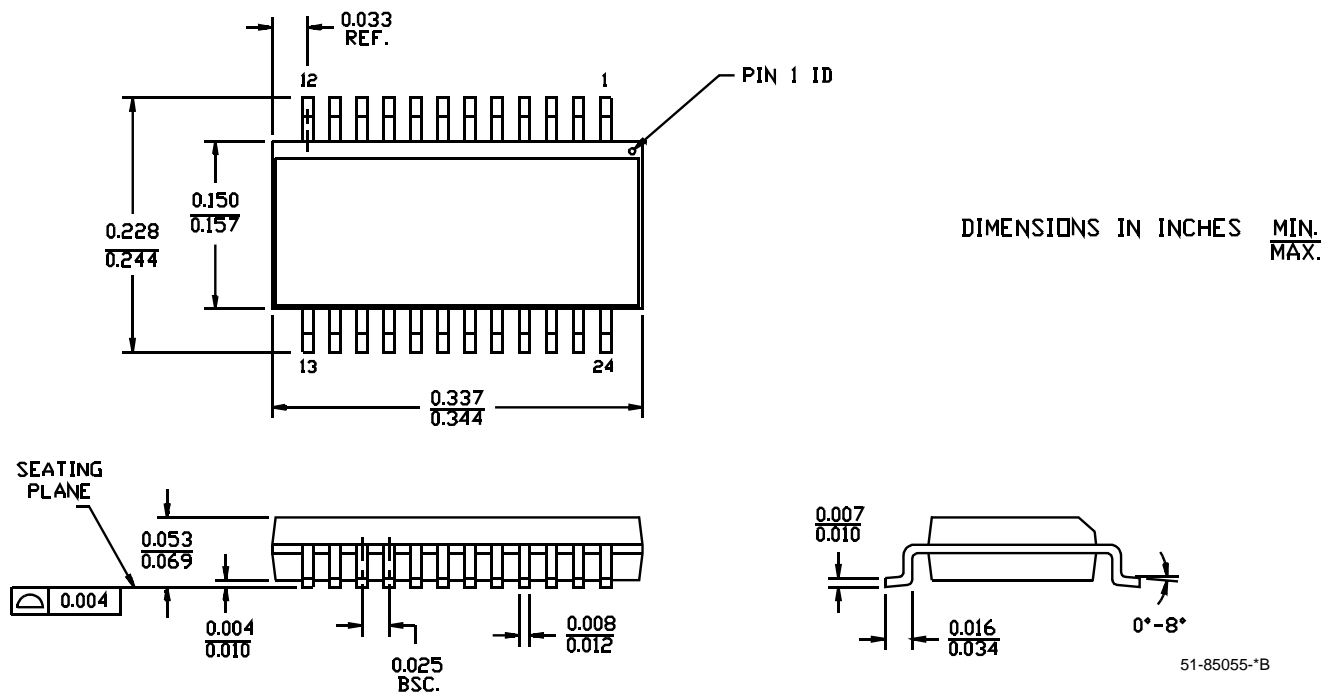
11.0   Package Diagrams (continued)

20-Lead (300-Mil) SOIC S5

PIN 1 ID

10   1

0.291[7.391]
0.300[7.620]

0.394[10.007]
0.419[10.642]   *

11   20

0.026[0.660]
0.032[0.812]
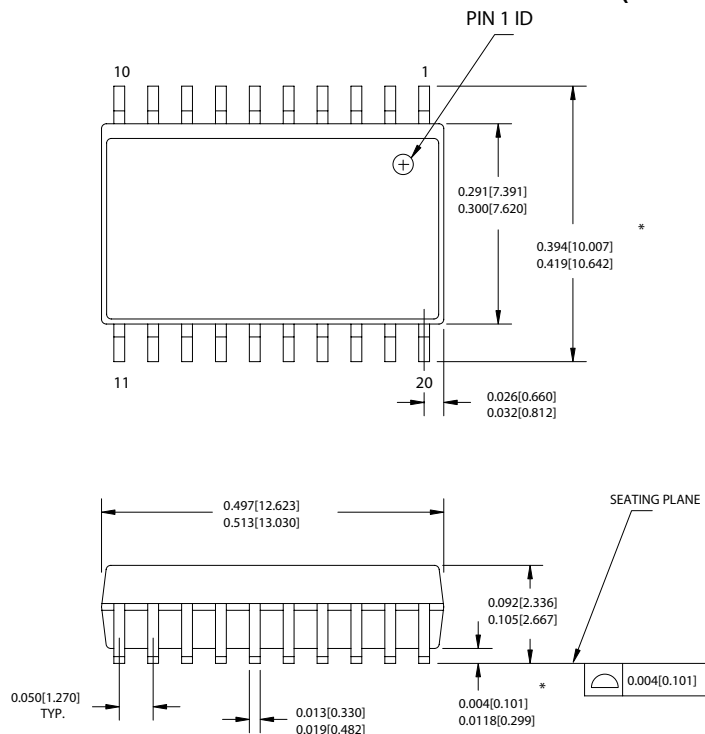
DIMENSIONS IN INCHES [MM]   MIN.
                              MAX.

REFERENCE JEDEC MO-119

PACKAGE WEIGHT 0.55 gms

	PART #
S20.3	STANDARD PKG.
SZ20.3	LEAD FREE PKG.

SEATING PLANE

0.497[12.623]
0.513[13.030]

0.092[2.336]
0.105[2.667]

0.050[1.270]
TYP.

0.013[0.330]
0.019[0.482]

0.004[0.101]
0.0118[0.299]   *

0.004[0.101]

0.015[0.381]
0.050[1.270]

0.0091[0.231]
0.0125[0.317]   *
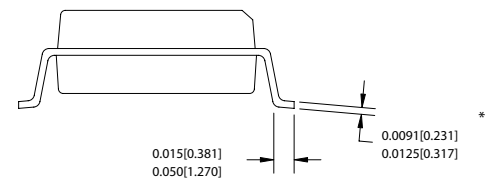
51-85024-*B

24-Lead (300-Mil) SOIC S13

PIN 1 ID

12   1

0.394[10.007]
0.419[10.642]   *

0.291[7.391]
0.300[7.620]

13   24

0.026[0.660]
0.032[0.812]
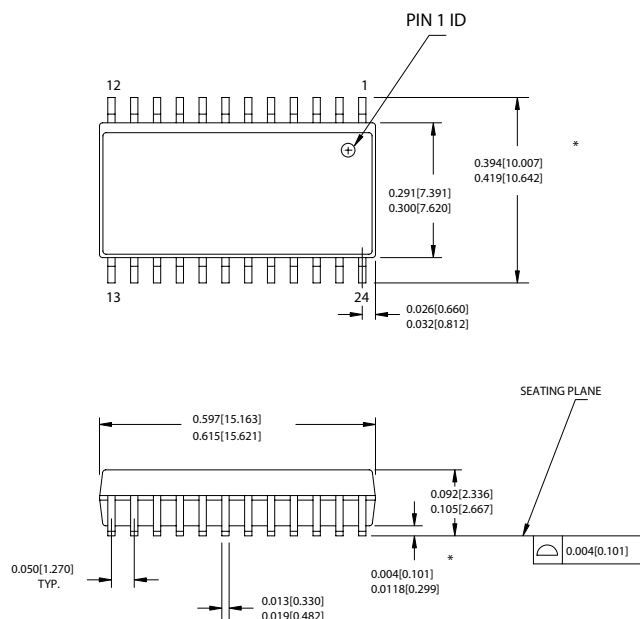
DIMENSIONS IN INCHES[MM]   MIN.
                             MAX.

REFERENCE JEDEC MO-119

PACKAGE WEIGHT 0.65gms

	PART #
S24.3	STANDARD PKG.
SZ24.3	LEAD FREE PKG.

SEATING PLANE

0.597[15.163]
0.615[15.621]

0.092[2.336]
0.105[2.667]

0.050[1.270]
TYP.

0.013[0.330]
0.019[0.482]

0.004[0.101]
0.0118[0.299]   *

0.004[0.101]

0.015[0.381]
0.050[1.270]

0.0091[0.231]
0.0125[0.317]   *
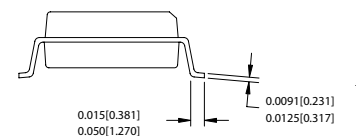
51-85025-*B

11.0   Package Diagrams (continued)
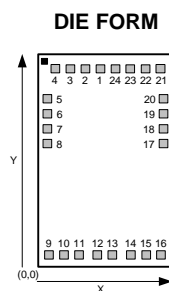
DIE FORM

Table 11-1 below shows the die pad coordinates for the CY7C63001C-XC. The center location of each bond pad is relative to the bottom left corner of the die which has coordinate (0,0).

Table 11-1. CY7C63001C-XC Probe Pad Coordinates in microns ((0,0) to bond pad centers)

Pad #	Pin Name	X (microns)	Y (microns)	Pad #	Pin Name	X (microns)	Y (microns)
1	Port00	676.00	2325.40	13	Xtlout	794.85	121.80
2	Port01	507.35	2325.40	14	Vcc	1033.55	121.80
3	Port02	338.70	2325.40	15	D-	1129.75	121.80
4	Port03	170.05	2325.40	16	D+	1451.70	121.80
5	Port10	120.10	2132.30	17	Port17	1446.10	1595.80
6	Port12	120.10	1962.90	18	Port15	1446.10	1765.20
7	Port14	120.10	1765.20	19	Port13	1446.10	1962.90
8	Port16	120.10	1595.80	20	Port11	1446.10	2132.30
9	Vss	148.50	121.80	21	Port07	1395.65	2325.40
10	Vpp	278.30	121.80	22	Port06	1227.00	2325.40
11	Cext	414.25	121.80	23	Port05	1058.35	2325.40
12	Xtalin	653.45	121.80	24	Port04	889.7	2325.40

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Document History Page

				Document Title: CY7C63001C, CY7C63101C Universal Serial Bus Microcontroller Document Number: 38-08026
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116223	06/12/02	DSG	Change from Spec number: 38-00662 to 38-08026
*A	276070	See ECN	BON	Added die form and bond pad information. Added lead free packages. Removed obsolete packages and their references
*B	408068	See ECN	TYJ	128-ms timer interrupts corrected to 128-μs interrupts Part Ordering information updated - Table 10.0. Type A updated with type C Data-sheet header changed to CY7C63001C, CY7C63101C