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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08gw32clkr

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1 Devices in the MC9S08GW64 Series

Table 1 summarizes the feature set available in the MC9S08GW64 series of MCUs.

Table 1. MC9S08GW64 Series Features by MCU and Package

Feature	MC9S08GW64		MC9S08GW32	
Package	80-pin LQFP	64-pin LQFP	80-pin LQFP	64-pin LQFP
FLASH	65,536 Bytes		32,768 Bytes	
RAM	4,032 Bytes		2,048 Bytes	
ADC0[1] Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC0 Differential Channels[2]	1	0	1	0
ADC1 Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC1 Differential Channels	1	1	1	1
BKPT	yes		yes	
ICS	yes		yes	
IIC	yes		yes	
IRQ	yes		yes	
IRTC	yes		yes	
KBI	8-ch		8-ch	
MTIM8	2		2	
MTIM16	yes		yes	
PCNT	yes		yes	
PCRC	yes		yes	
PDB	yes		yes	
PRACMP	3		3	
SCI	4		4	
SPI	3		3	
FTM	2-ch		2-ch	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO	yes	yes	yes	yes
XOSC	2		2	
I/O pins[3]	57	45	57	45

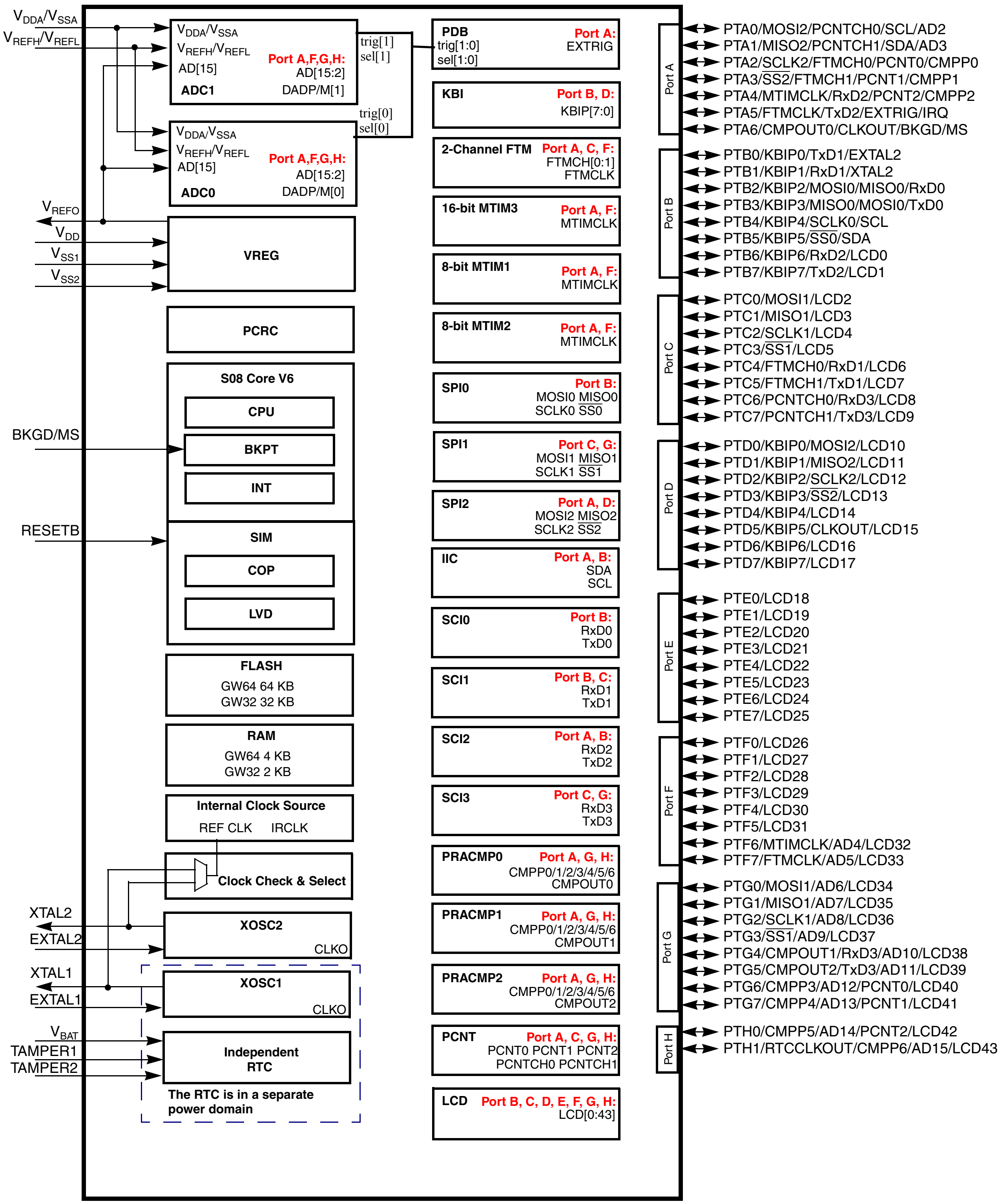


Figure 1. MC9S08GW64 Series Block Diagram

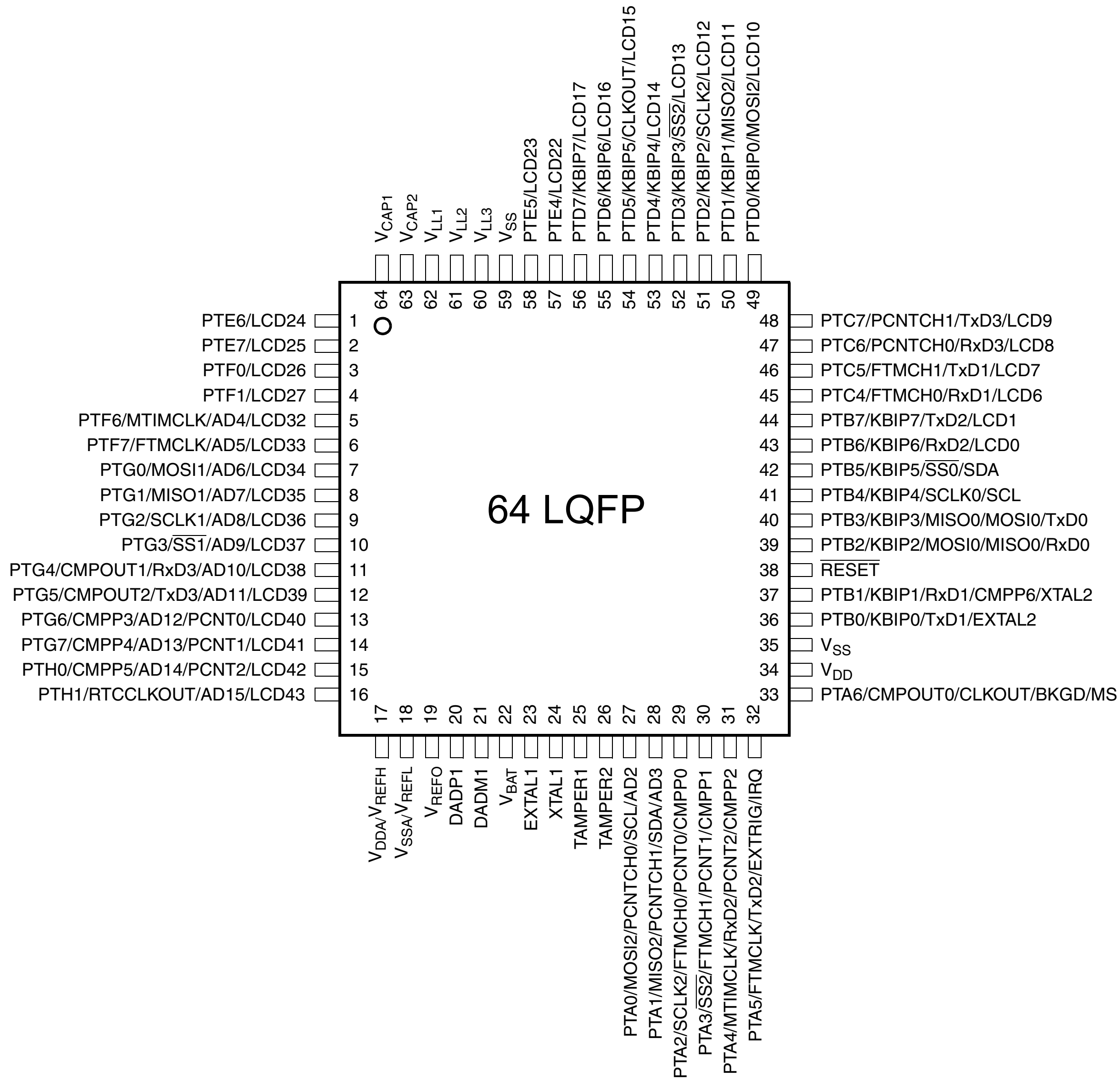


Figure 3. MC9S08GW64 Series in 64-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
1	1	PTE6	PTE6		LCD24		
2	2	PTE7	PTE7		LCD25		
3	3	PTF0	PTF0	LCD26			
4	4	PTF1	PTF1	LCD27			
5		PTF2	PTF2	LCD28			
6		PTF3	PTF3	LCD29			

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
42	34	V_{DD}	V_{DD}				
43	35	V_{SS}	V_{SS}				
44	36	PTB0	PTB0	KBIP0	TxD1	EXTAL2	
45	37	PTB1[1]	PTB1	KBIP1	RxD1	CMPP6	XTAL2
46	38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$				
47	39	PTB2	PTB2	KBIP2	MOSI0	MISO0	RxD0
48	40	PTB3[4]	PTB3	KBIP3	MISO0	MOSI0	TxD0
49	41	PTB4[3]	PTB4	KBIP4	SCLK0	SCL	
50	42	PTB5[3]	PTB5	KBIP5	$\overline{\text{SS0}}$	SDA	
51	43	PTB6	PTB6	KBIP6	RxD2	LCD0	
52	44	PTB7	PTB7	KBIP7	TxD2	LCD1	
53		PTC0	PTC0	MOSI1	LCD2		
54		PTC1	PTC1	MISO1	LCD3		
55		PTC2	PTC2	SCLK1	LCD4		
56		PTC3	PTC3	$\overline{\text{SS1}}$	LCD5		
57	45	PTC4	PTC4	FTMCH0	RxD1	LCD6	
58	46	PTC5	PTC5	FTMCH1	TxD1	LCD7	
59	47	PTC6	PTC6	PCNTCH0	RxD3	LCD8	
60	48	PTC7	PTC7	PCNTCH1	TxD3	LCD9	
61	49	PTD0	PTD0	KBIP0	MOSI2	LCD10	
62	50	PTD1	PTD1	KBIP1	MISO2	LCD11	
63	51	PTD2	PTD2	KBIP2	SCLK2	LCD12	
64	52	PTD3	PTD3	KBIP3	$\overline{\text{SS2}}$	LCD13	
65	53	PTD4	PTD4	KBIP4	LCD14		
66	54	PTD5	PTD5	KBIP5	CLKOUT	LCD15	
67	55	PTD6	PTD6	KBIP6	LCD16		
68	56	PTD7	PTD7	KBIP7	LCD17		
69		PTE0	PTE0	LCD18			
70		PTE1	PTE1	LCD19			
71		PTE2	PTE2	LCD20			
72		PTE3	PTE3	LCD21			
73	57	PTE4	PTE4		LCD22		
74	58	PTE5	PTE5		LCD23		
75	59	V_{SS}	V_{SS}				
76	60	V_{LL3}	V_{LL3}				

high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins except PTA5 and PTB1)[1, 2, 3]	I_D	± 25	mA
Instantaneous maximum current Single pin limit (applies to PTA5 and PTB1)[1,2,3]	I_D	± 50	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature		T_J	95	°C
Thermal resistance Single-layer board				
	80-pin LQFP	θ_{JA}	61	°C/W
	64-pin LQFP		70	
Thermal resistance Four-layer board				
	80-pin LQFP	θ_{JA}	48	°C/W
	64-pin LQFP		52	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
5	C	Output low voltage	All non-LCD pins low-drive strength	V_{OL}	$V_{DD} > 1.8$ V $I_{Load} = 0.6$ mA	—	—	0.5	V
	P		All non-LCD pins high-drive strength		$V_{DD} > 2.7$ V $I_{Load} = 10$ mA	—	—	0.5	
	C				$V_{DD} > 1.8$ V $I_{Load} = 3$ mA	—	—	0.5	
6	C	Output low voltage	All LCD/GPIO pins low-drive strength	V_{OL}	$V_{DD} > 1.8$ V $I_{Load} = 0.5$ mA	—	—	0.5	V
	P		All LCD/GPIO pins high-drive strength		$V_{DD} > 2.7$ V $I_{Load} = 3$ mA	—	—	0.5	
	C				$V_{DD} > 1.8$ V $I_{Load} = 1$ mA	—	—	0.5	
7	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage	all digital inputs	V_{IH}	$V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V
	C				$V_{DD} > 1.8$ V	0.85 x V_{DD}	—	—	
9	P	Input low voltage	all digital inputs	V_{IL}	$V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	
	C				$V_{DD} > 1.8$ V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis	all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current	all input only pins (per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	0.025	1	μA
12	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	0.025	1	μA
13	C	Total leakage current[2]	Total leakage current for all pins	$\|I_{InT}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
14	P	Pullup, Pulldown resistors	all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors	all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
16	D	DC injection current[3, 4, 5]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
18	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
19	C	iRTC RAM retention voltage		V_{iRAM}		—	1.05	—	V
20	C	POR re-arm voltage[6]		V_{POR}		0.9	1.4	2.0	V
21	D	POR re-arm time		t_{POR}		10	—	—	μs

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
22	C	Low-voltage detection threshold	High range — V_{DD} falling	V_{LVDH}		2.11	2.16	2.22	V
			High range — V_{DD} rising			2.16	2.23	2.27	
23	C	Low-voltage detection threshold	Low range — V_{DD} falling	V_{LVDL}		1.80	1.85	1.91	V
			Low range — V_{DD} rising			1.86	1.92	1.99	
24	C	Low-voltage warning threshold	V_{DD} falling, LVWV = 1	V_{LVWH}		2.36	2.46	2.56	V
			V_{DD} rising, LVWV = 1			2.52	2.49	2.71	
25	C	Low-voltage warning	V_{DD} falling, LVWV = 0	V_{LVWL}		2.10	2.16	2.23	V
			V_{DD} rising, LVWV = 0			2.15	2.23	2.26	
26	C	Low-voltage inhibit reset/recover hysteresis		V_{hys}		—	80	—	mV
27	P	Bandgap Voltage Reference[7]		V_{BG}		1.15	1.17	1.19	V

1 Typical values are measured at 25°C. Characterized, not tested

2 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250nA.

3 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 POR will occur below the minimum voltage.

7 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

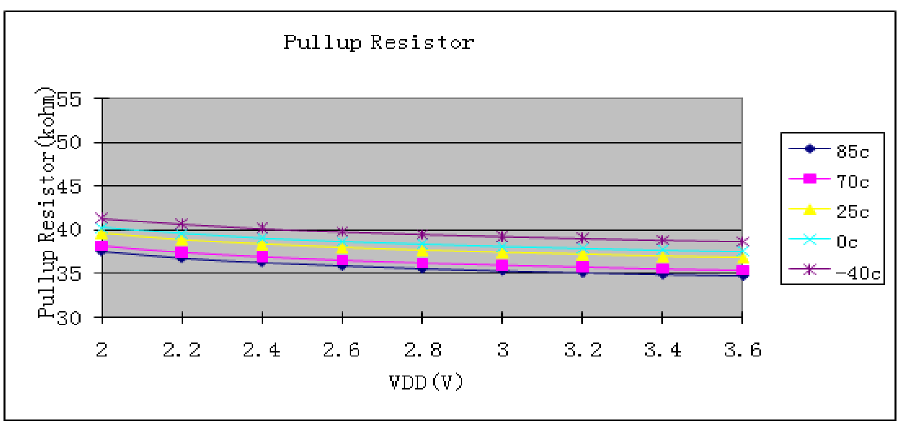
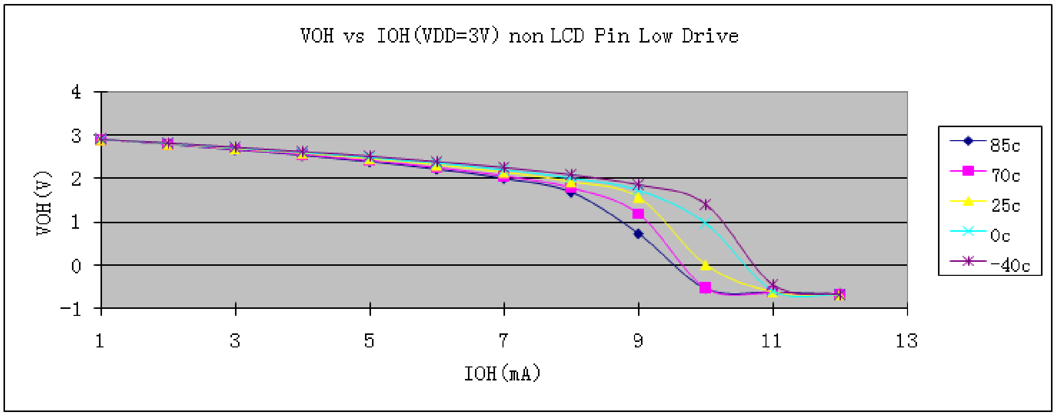


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values



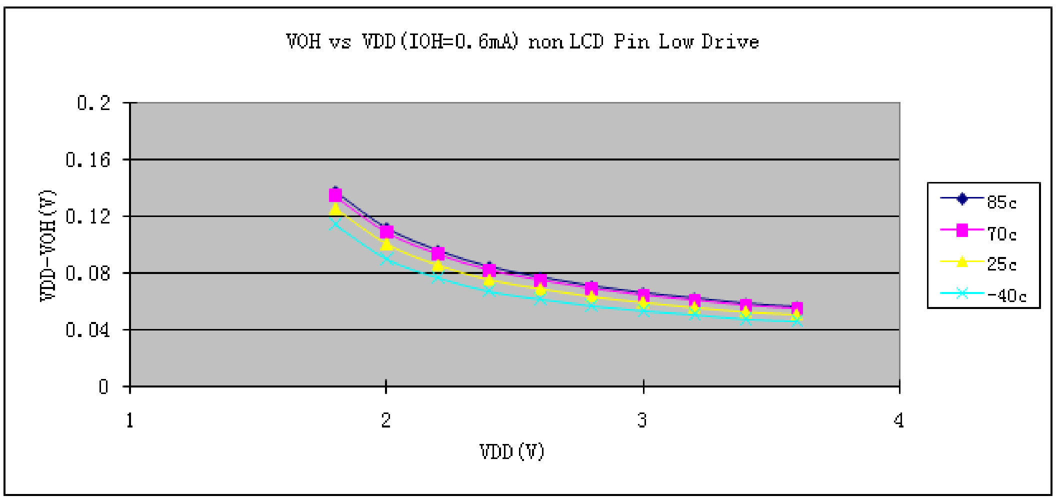
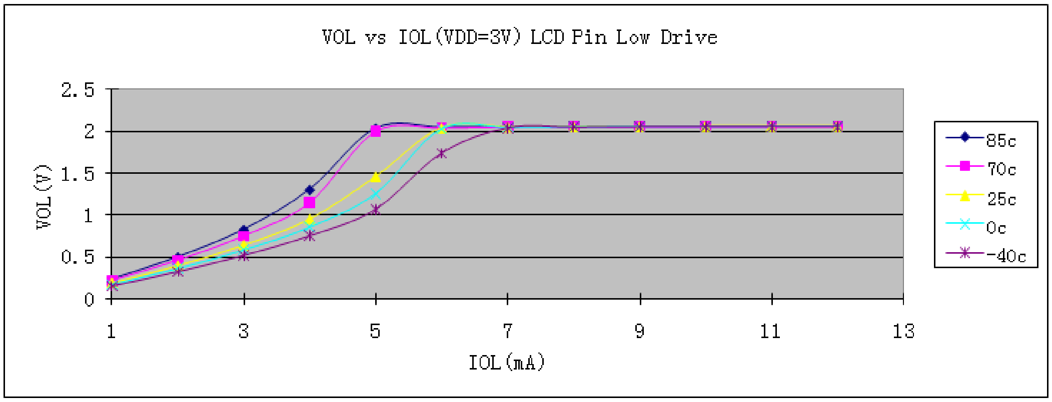


Figure 8. Typical High-Side (Source) Characteristics (Non LCD pins)— Low Drive (PTxDSn = 0)



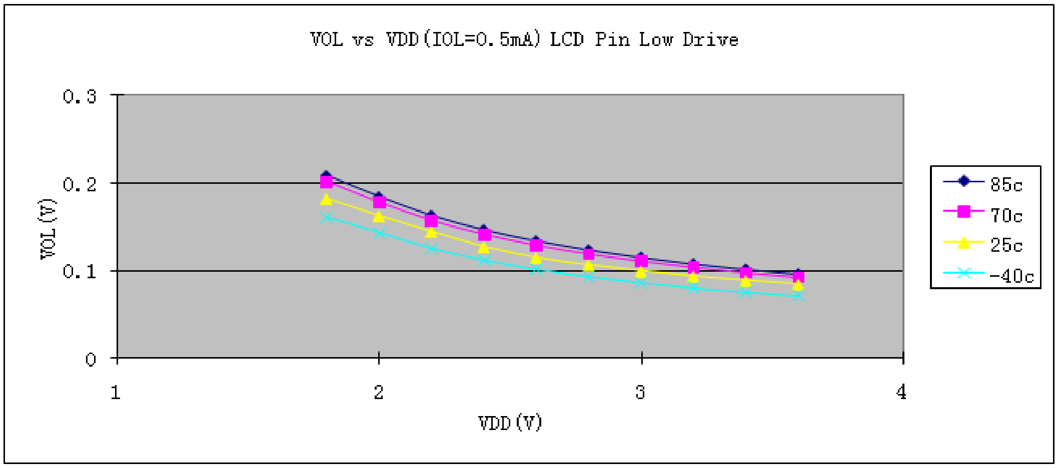
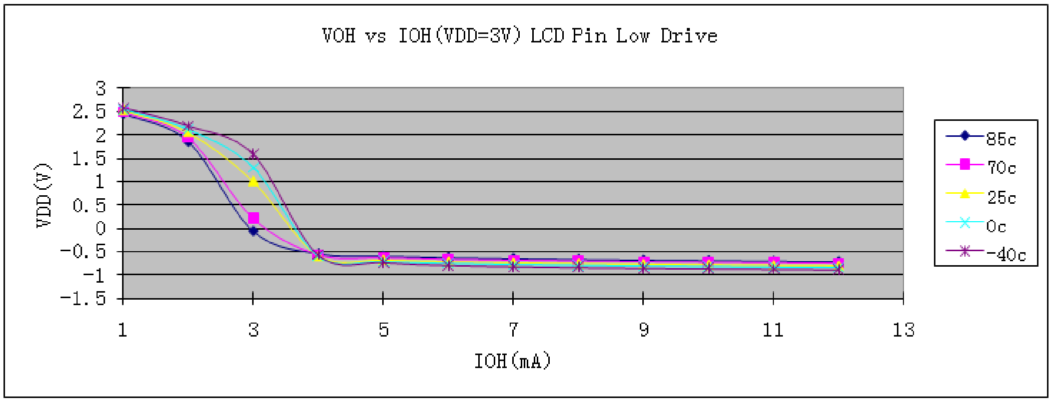


Figure 10. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — Low Drive (PTxDSn = 0)



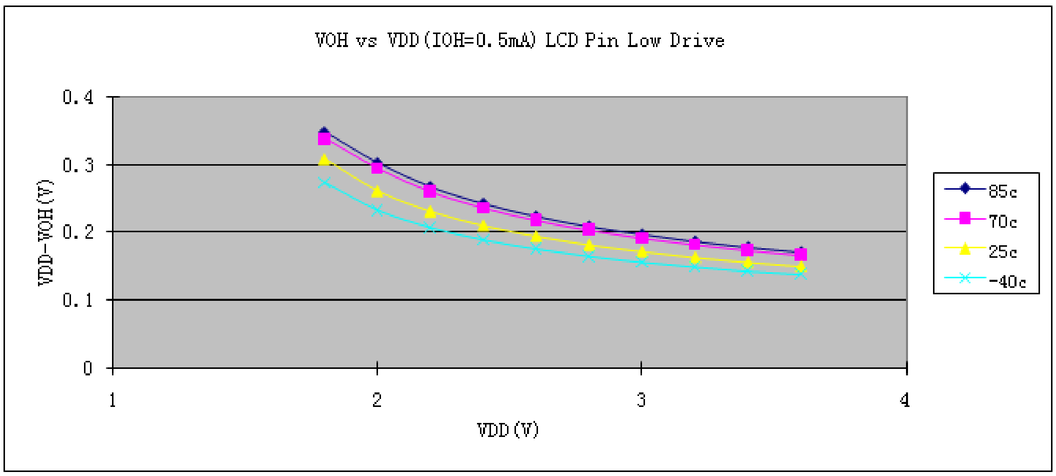


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO pins)— Low Drive (PTxDSn = 0)

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	137	—	µA	–40 to 85°C
	T			16 kHz FBELP		8	—		
6	C	Wait mode supply current, all modules off	WI_{DD}	20 MHz	3	5.4	7.5	mA	–40 to 85°C
	C			2 MHz		1.1	—		
7	T	Wait mode supply current LPRS = 0, all modules off	WI_{DD}	16 kHz FBILP	3	131	—	µA	–40 to 85°C
	T			16 kHz FBELP	3	123	—	µA	–40 to 85°C
8	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBILP	3	159	—	µA	–40 to 85°C
	T			16 kHz FBELP	3	5.6	—	µA	–40 to 85°C
9	C	Stop2 mode supply current	$S2I_{DD}$	N/A	3	330	1000	nA	–40 to 25°C
						1622	—		70°C
						6000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C
10	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	N/A	3	474	1100	nA	–40 to 25°C
						2608	—		70°C
						9000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C

[1] Typical values are measured at 25°C. Characterized, not tested.

Table 10. Stop Mode Adders (V_{DD}=3V, V_{DDA}=V_{DD})

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	C	LPO		100	100	150	175	nA
2	C	ERREFSTEN	RANGE = HGO = 0	600	737	830	863	nA
3	C	IREFSTEN[1]		—	73	80	92	µA
4	C	LVD[1]	LVDSE = 1	110	112	112	113	µA
5	C	PRACMP[1]	Not using the bandgap (BGBE = 0), PRG enabled	30	35	40	55	µA

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

[2] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[3] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

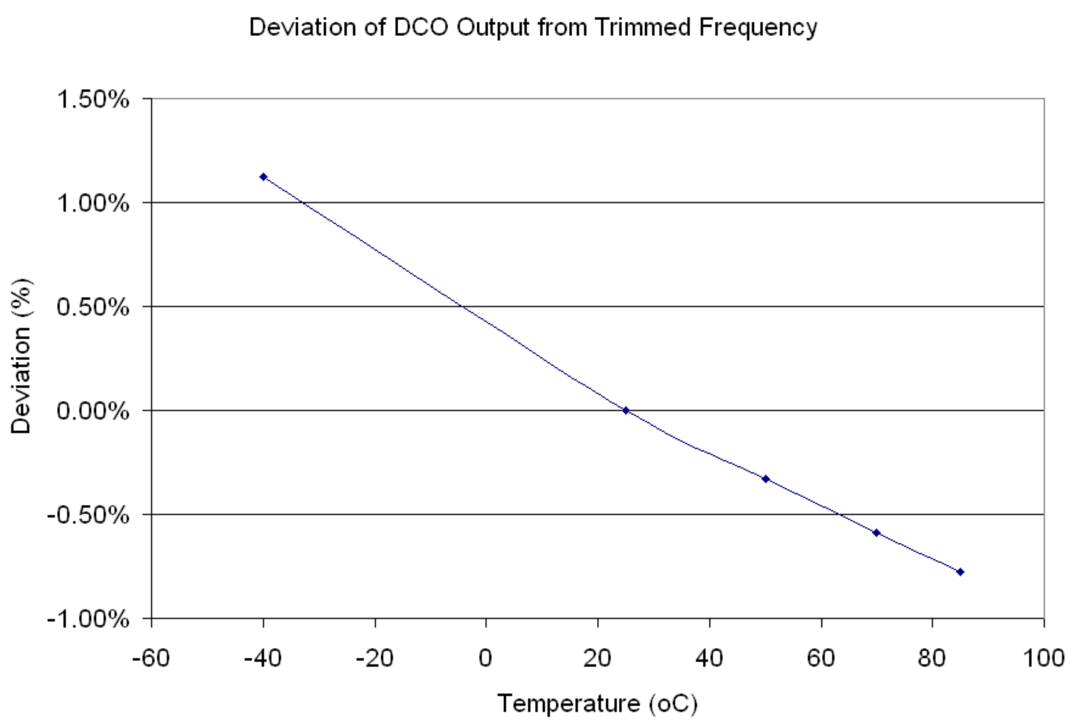


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

6 Except for LCD pins in Open Drain mode.

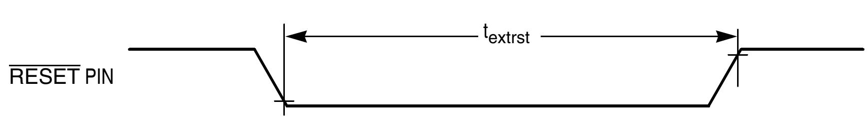


Figure 17. Reset Timing

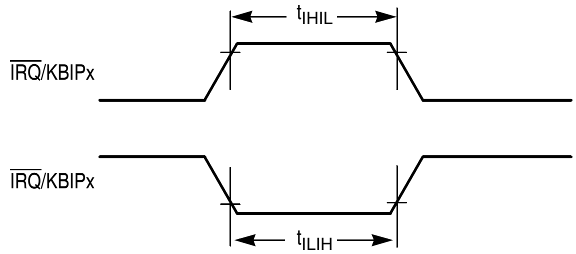


Figure 18. IRQ/KBIPx Timing

3.10.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

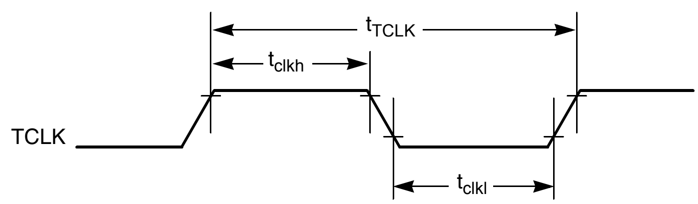
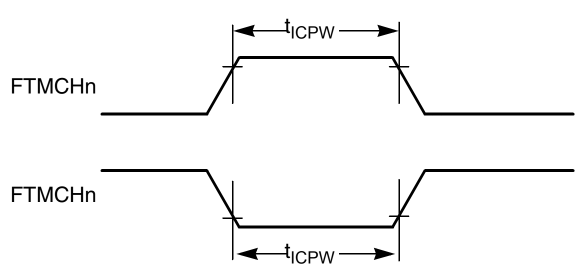


Figure 19. Timer External Clock



3.11 Analog Comparator (PRACMP) Electricals

Table 16. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA
4	C	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	D	Analog input voltage	VAIN	$V_{SS} - 0.3$	—	V_{DD}	V
6	C	Analog input offset voltage	VAIO	—	5	40	mV
7	C	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	P	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	C	Analog comparator initialization delay	tAINIT	—	—	1.0	µs
10	C	Programmable reference generator inputs	$V_{In1}(V_{DD})$	1.8	—	V_{DD}	V
11	C	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	C	Programmable reference generator setup delay	t_{PRGST}	—	—	—	ns
13	C	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB
14	C	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V

3.12 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs.. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} $(V_{DD}–V_{DDA})^2$	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} $(V_{SS}–V_{SSA})^2$	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

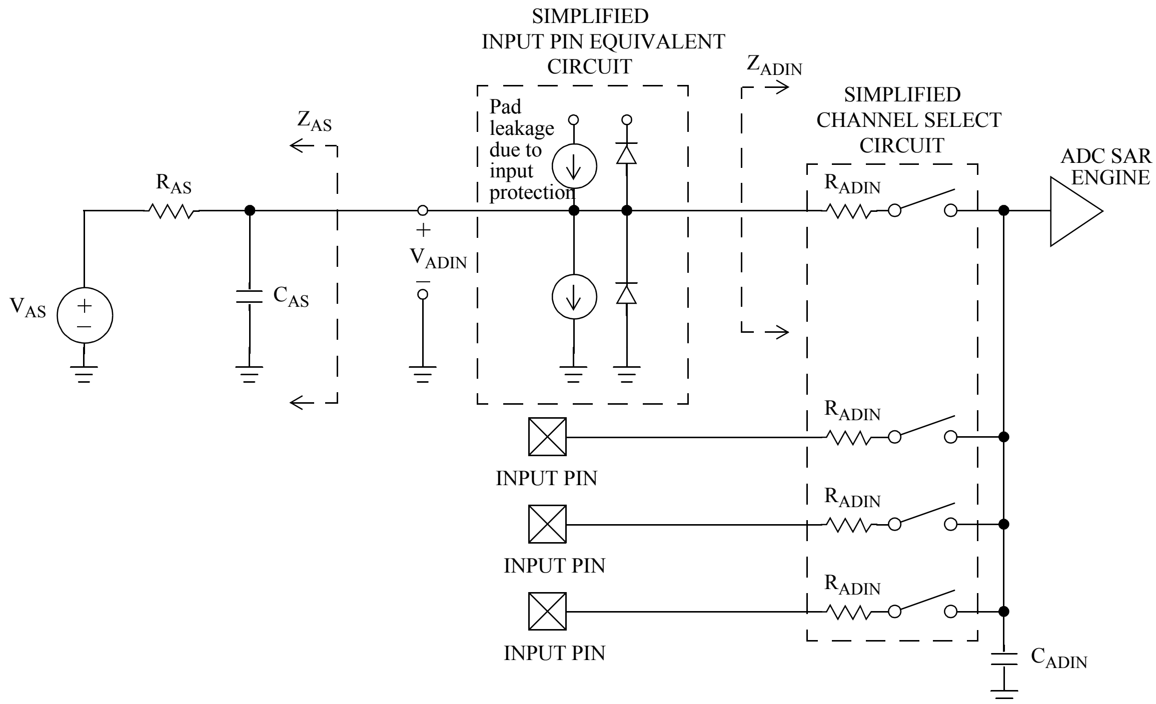


Figure 24. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 10MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	µA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	540	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.072	—	µA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

2 Typical values assume $V_{DDAD} = 3.0V$, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 19. 16-bit ADC Characteristics(V_{REFH} = V_{DDAD} ≥ 2.7V, V_{REFL} = V_{SSAD}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-38	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}
2 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3 1 LSB = $(V_{REFH}–V_{REFL})/2^N$

3.13 VREF Characteristics

Table 20. Electrical specifications

Num	C	Characteristic	Symbol	Min	Max	Unit
1	P	Supply voltage	V_{DD}	1.80	3.60	V
2	P	Operating temperature range	T_{op}	–40	85	C
3	C	Maximum Load			10	mA
		Operation across Temperature				
4	P	Voltage output room temperature	Untrimmed	1.070–1.3		V
5	P	Voltage output room temperature	Factory trimmed[1]	1.180–1.22		V
6	C	–40 °C	Factory trimmed	1.19–1.200		V
7	C	85 °C	Factory trimmed	1.185–1.200		V
		Load Bandwidth				
8	C	Load Regulation Mode = 10 at 1mA load	Mode = 10	20	100	µV/mA
9	C	Line Regulation (Power Supply Rejection)	DC	±0.1 from room temp voltage		mV
			AC	–60		dB
		Power Consumption				
10	C	Powered down Current (Stop Mode, VREFEN = 0, VRSTEN = 0)	I		100	µA
11	C	Bandgap only (Mode[1:0] 00)	I		75	µA
12	C	Low Power buffer (Mode[1:0] 01)	I		125	µA
13	C	Tight Regulation buffer (Mode[1:0] 10)	I		1.1	mA
14	C	Low Power and Tight Regulation (Mode[1:0] 11)	I		1.15	mA

1 Factory trim is performed at the room temperature.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

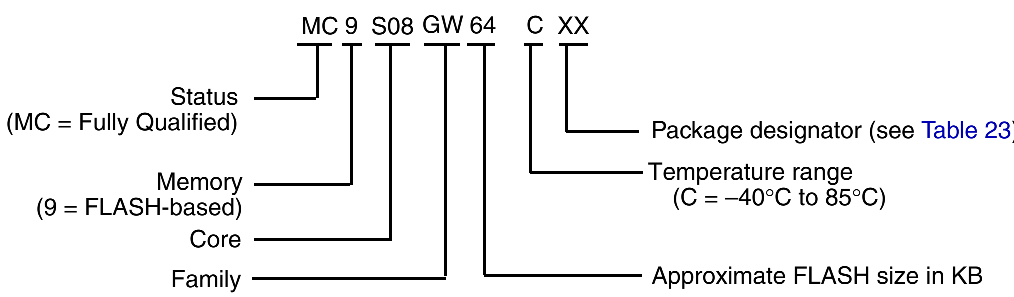
5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08GW64 Series.

4.1 Device Numbering System

Example of the device numbering system:



5 Package Information and Mechanical Drawings

Table 23 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08GW64 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 23, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 23) in the “Enter Keyword” search box at the top of the page.

Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W