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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HC08 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SCI, SPI |
| Peripherals | LVD, POR, PWM |
| Number of I/O | 33 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 42-SDIP (0.600", 15.24mm) |
| Supplier Device Package | 42-PDIP |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908gp32cb |

# MC68HC908GP32

**Data Sheet**

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $FE08 | FLASH Control Register (FLCR) | Read: | 0 | 0 | 0 | 0 | HVEN | MASS | ERASE | PGM |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FE09 | Break Address Register High (BRKH) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FE0A | Break Address Register Low (BRKL) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FE0B | Break Status and Control Register (BRKSCR) | Read: | BRKE | BRKA | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FE0C | LVI Status Register (LVISR) | Read: | LVIOUT | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $FF7E | FLASH Block Protect Register (FLBPR)† | Read: | BPR7 | BPR6 | BPR5 | BPR4 | BPR3 | BPR2 | BPR1 | BPR0 |
| | | Write: | | | | | | | | |
| | | Reset: | U | U | U | U | U | U | U | U |
| $FFFF | COP Control Register (COPCTL) | Read: | Low byte of reset vector | | | | | | | |
| | | Write: | Writing clears COP counter (any value) | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |

† Non-volatile FLASH register

= Unimplemented R = Reserved U = Unaffected

**Figure 2-2. Control, Status, and Data Registers (Sheet 6 of 6)**

## 3.10 Serial Communications Interface Module (SCI)

### 3.10.1 Wait Mode

The SCI module remains active in wait mode. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

### 3.10.2 Stop Mode

The SCI module is inactive in stop mode. The STOP instruction does not affect SCI register states. SCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

## 3.11 Serial Peripheral Interface Module (SPI)

### 3.11.1 Wait Mode

The SPI module remains active in wait mode. Any enabled CPU interrupt request from the SPI module can bring the MCU out of wait mode.

If SPI module functions are not required during wait mode, reduce power consumption by disabling the SPI module before executing the WAIT instruction.

### 3.11.2 Stop Mode

The SPI module is inactive in stop mode. The STOP instruction does not affect SPI register states. SPI operation resumes after an external interrupt. If stop mode is exited by reset, any transfer in progress is aborted, and the SPI is reset.

## 3.12 Timer Interface Module (TIM1 and TIM2)

### 3.12.1 Wait Mode

The TIM remains active in wait mode. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

### 3.12.2 Stop Mode

The TIM is inactive in stop mode. The STOP instruction does not affect register states or the state of the TIM counter. TIM operation resumes when the MCU exits stop mode after an external interrupt.

# Chapter 7
# Computer Operating Properly (COP)

## 7.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the CONFIG register.

## 7.2 Functional Description

Figure 7-1 shows the structure of the COP module.

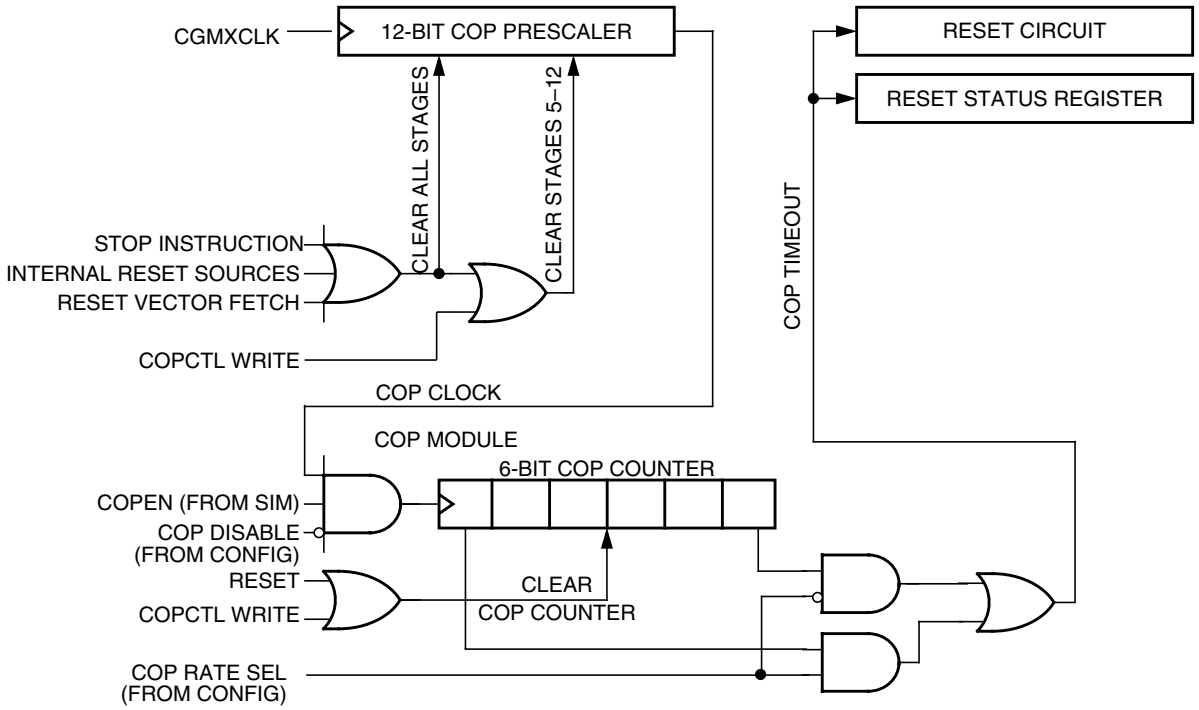


**Figure 7-1. COP Block Diagram**

### 7.3.7 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register. (See Chapter 6 Configuration Register (CONFIG).)

### 7.3.8 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register. (See Chapter 6 Configuration Register (CONFIG).)

## 7.4 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: | Low byte of reset vector | | | | | | | |
| Write: | Clear COP counter | | | | | | | |
| Reset: | Unaffected by reset | | | | | | | |

**Figure 7-2. COP Control Register (COPCTL)**

## 7.5 Interrupts

The COP does not generate CPU interrupt requests.

## 7.6 Monitor Mode

When monitor mode is entered with $V_{TST}$ on the $\overline{IRQ}$ pin, the COP is disabled as long as $V_{TST}$ remains on the $\overline{IRQ}$ pin or the $\overline{RST}$ pin. When monitor mode is entered by having blank reset vectors and not having $V_{TST}$ on the $\overline{IRQ}$ pin, the COP is automatically disabled until a POR occurs.

## 7.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

### 7.7.1 Wait Mode

The COP remains active during wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter in a CPU interrupt routine.

### 7.7.2 Stop Mode

Stop mode turns off the CGMXCLK input to the COP and clears the COP prescaler. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

# Chapter 11
# Low-Voltage Inhibit (LVI)

## 11.1 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the $V_{DD}$ pin and can force a reset when the $V_{DD}$ voltage falls below the LVI trip falling voltage, $V_{TRIPF}$.

## 11.2 Features

Features of the LVI module include:

- Programmable LVI reset
- Selectable LVI trip voltage
- Programmable stop mode operation

## 11.3 Functional Description

Figure 11-1 shows the structure of the LVI module. The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit, LVIPWRD, enables the LVI to monitor $V_{DD}$ voltage. Clearing the LVI reset disable bit, LVIRSTD, enables the LVI module to generate a reset when $V_{DD}$ falls below a voltage, $V_{TRIPF}$. Setting the LVI enable in stop mode bit, LVISTOP, enables the LVI to operate in stop mode. Setting the LVI 5-V or 3-V trip point bit, LVI5OR3, enables the trip point voltage, $V_{TRIPF}$, to be configured for 5-V operation. Clearing the LVI5OR3 bit enables the trip point voltage, $V_{TRIPF}$, to be configured for 3-V operation. The actual trip points are shown in Chapter 19 Electrical Specifications.

***NOTE***

*After a power-on reset (POR) the LVI's default mode of operation is 3 V. If a 5-V system is used, the user must set the LVI5OR3 bit to raise the trip point to 5-V operation. Note that this must be done after every power-on reset since the default will revert back to 3-V mode after each power-on reset. If the $V_{DD}$ supply is below the 5-V mode trip voltage but above the 3-V mode trip voltage when POR is released, the part will operate because $V_{TRIPF}$ defaults to 3-V mode after a POR. So, in a 5-V system care must be taken to ensure that $V_{DD}$ is above the 5-V mode trip voltage after POR is released.*

***NOTE***

*If the user requires 5-V mode and sets the LVI5OR3 bit after a power-on reset while the $V_{DD}$ supply is not above the $V_{TRIPR}$ for 5-V mode, the MCU will immediately go into reset. The LVI in this case will hold the part in reset until either $V_{DD}$ goes above the rising 5-V trip point, $V_{TRIPR}$, which will release reset or $V_{DD}$ decreases to approximately 0 V which will re-trigger the power-on reset and reset the trip point to 3-V operation.*

### 13.4.2 Transmitter

Figure 13-4 shows the structure of the SCI transmitter.

The baud rate clock source for the SCI can be selected via the configuration bit, SCIBDSRC. Source selection values are shown in Figure 13-4.

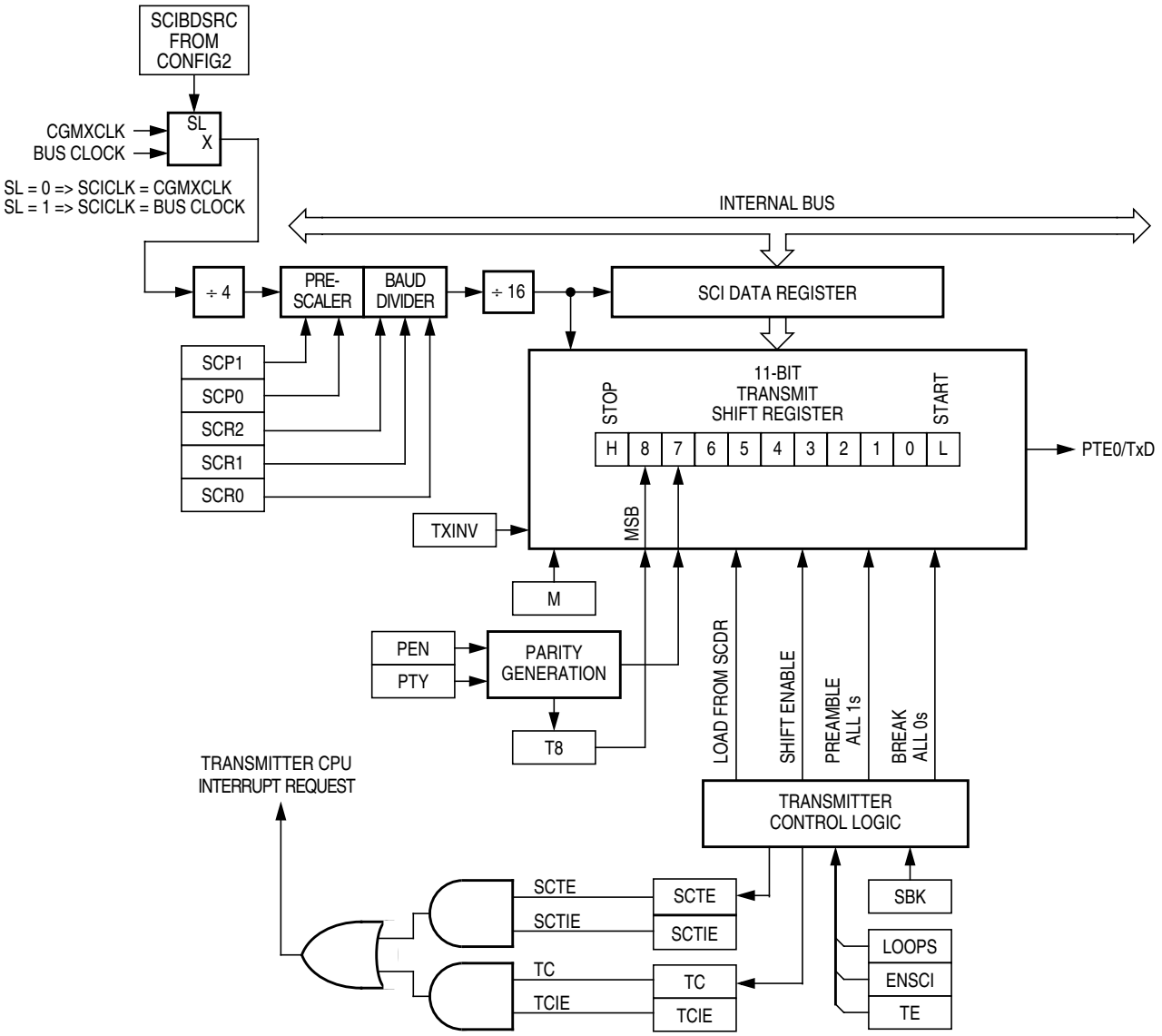


**Figure 13-4. SCI Transmitter Block Diagram**

#### *13.4.2.1 Character Length*

The transmitter can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCC1) determines character length. When transmitting 9-bit data, bit T8 in SCI control register 3 (SCC3) is the ninth bit (bit 8).

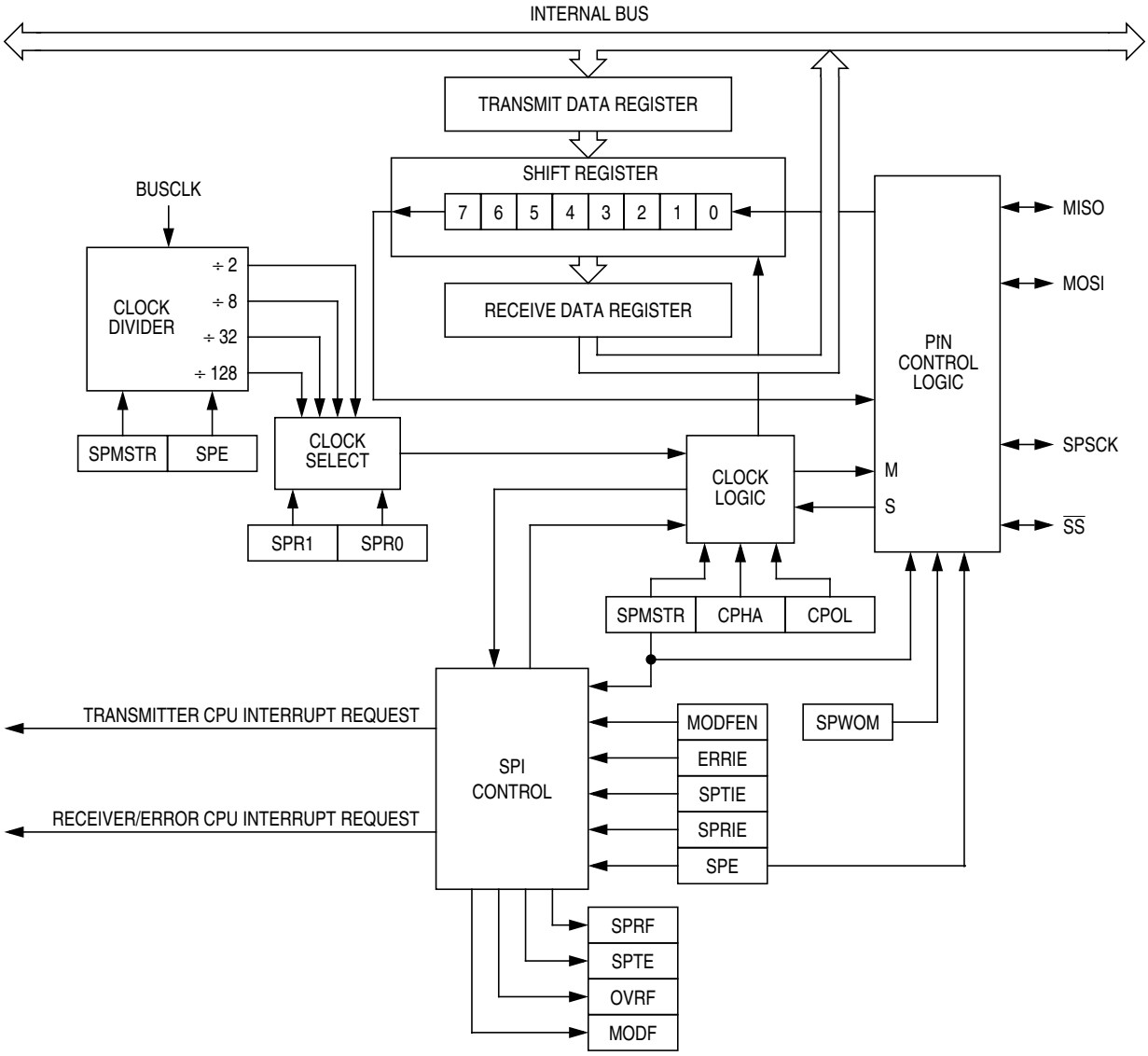


**Figure 15-2. SPI Module Block Diagram**

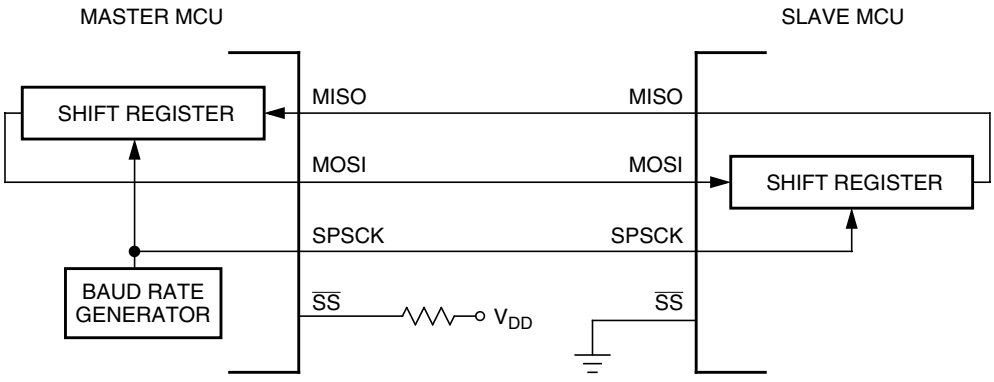


**Figure 15-3. Full-Duplex Master-Slave Connections**

# Chapter 16
# Timebase Module (TBM)

## 16.1 Introduction

This section describes the timebase module (TBM). The TBM will generate periodic interrupts at user selectable rates using a counter clocked by the external crystal clock. This TBM version uses 15 divider stages, eight of which are user selectable.

## 16.2 Features

Features of the TBM module include:

- Software programmable 1-Hz, 4-Hz, 16-Hz, 256-Hz, 512-Hz, 1024-Hz, 2048-Hz, and 4096-Hz periodic interrupt using external 32.768-kHz crystal
- Configurable for operation during stop mode to allow periodic wakeup from stop

## 16.3 Functional Description

***NOTE***

*This module is designed for a 32.768-kHz oscillator.*

This module can generate a periodic interrupt by dividing the crystal frequency, CGMXCLK. The counter is initialized to all 0s when TBON bit is cleared. The counter, shown in Figure 16-1, starts counting when the TBON bit is set. When the counter overflows at the tap selected by TBR2:TBR0, the TBIF bit gets set. If the TBIE bit is set, an interrupt request is sent to the CPU. The TBIF flag is cleared by writing a 1 to the TACK bit. The first time the TBIF flag is set after enabling the timebase module, the interrupt is generated at approximately half of the overflow period. Subsequent events occur at the exact period.

## 16.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes.

### 16.6.1 Wait Mode

The timebase module remains active after execution of the WAIT instruction. In wait mode, the timebase register is not accessible by the CPU.

If the timebase functions are not required during wait mode, reduce the power consumption by stopping the timebase before enabling the WAIT instruction.

### 16.6.2 Stop Mode

The timebase module may remain active after execution of the STOP instruction if the oscillator has been enabled to operate during stop mode through the OSCSTOPEN bit in the CONFIG register. The timebase module can be used in this mode to generate a periodic wakeup from stop mode.

If the oscillator has not been enabled to operate in stop mode, the timebase module will not be active during STOP mode. In stop mode the timebase register is not accessible by the CPU.

If the timebase functions are not required during stop mode, reduce the power consumption by stopping the timebase before enabling the STOP instruction.

## 17.8 I/O Signals

Port D shares four of its pins with the TIM. The four TIM channel I/O pins are T1CH0, T1CH1, T2CH0, and T2CH1 as described in 17.3 Pin Name Conventions.

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. T1CH0 and T2CH0 can be configured as buffered output compare or buffered PWM pins.

## 17.9 I/O Registers

***NOTE***

*References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TSC may generically refer to both T1SC AND T2SC.*

These I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0, TSC1)
- TIM channel registers (TCH0H:TCH0L, TCH1H:TCH1L)

### 17.9.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: T1SC, $0020 and T2SC, $002B

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: | TOF | TOIE | TSTOP | 0 | 0 | PS2 | PS1 | PS0 |
| Write: | 0 | | | TRST | | | | |
| Reset: | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented

**Figure 17-4. TIM Status and Control Register (TSC)**

**TOF — TIM Overflow Flag Bit**

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a logic 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing logic 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a logic 1 to TOF has no effect.

1 = TIM counter has reached modulo value

0 = TIM counter has not reached modulo value

**TOIE — TIM Overflow Interrupt Enable Bit**

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

**TSTOP — TIM Stop Bit**

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

***NOTE***

*Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

**TRST — TIM Reset Bit**

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM counter is reset and always reads as logic 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared
0 = No effect

***NOTE***

*Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of $0000.*

**PS[2:0] — Prescaler Select Bits**

These read/write bits select one of the seven prescaler outputs as the input to the TIM counter as Table 17-2 shows. Reset clears the PS[2:0] bits.

**Table 17-2. Prescaler Selection**

| PS2 | PS1 | PS0 | TIM Clock Source |
|---|---|---|---|
| 0 | 0 | 0 | Internal bus clock ÷ 1 |
| 0 | 0 | 1 | Internal bus clock ÷ 2 |
| 0 | 1 | 0 | Internal bus clock ÷ 4 |
| 0 | 1 | 1 | Internal bus clock ÷ 8 |
| 1 | 0 | 0 | Internal bus clock ÷ 16 |
| 1 | 0 | 1 | Internal bus clock ÷ 32 |
| 1 | 1 | 0 | Internal bus clock ÷ 64 |
| 1 | 1 | 1 | Not available |

## 17.9.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

Address: T1CH0H, $0026 and T2CH0H, $0031

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| Reset: | Indeterminate after reset | | | | | | | |

**Figure 17-12. TIM Channel 0 Register High (TCH0H)**

Address: T1CH0L, $0027 and T2CH0L $0032

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Reset: | Indeterminate after reset | | | | | | | |

**Figure 17-13. TIM Channel 0 Register Low (TCH0L)**

Address: T1CH1H, $0029 and T2CH1H, $0034

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| Reset: | Indeterminate after reset | | | | | | | |

**Figure 17-14. TIM Channel 1 Register High (TCH1H)**

Address: T1CH1L, $002A and T2CH1L, $0035

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| Reset: | Indeterminate after reset | | | | | | | |

**Figure 17-15. TIM Channel 1 Register Low (TCH1L)**

### 18.3.2 Security

A security feature discourages unauthorized reading of Flash locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

**NOTE**

*Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.*

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTA0. If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all Flash locations and execute code from Flash. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. See Figure 18-17.

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a Flash location returns an invalid value and trying to execute code from Flash causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

**NOTE**

*The MCU does not transmit a break character until after the host sends the eight security bytes.*

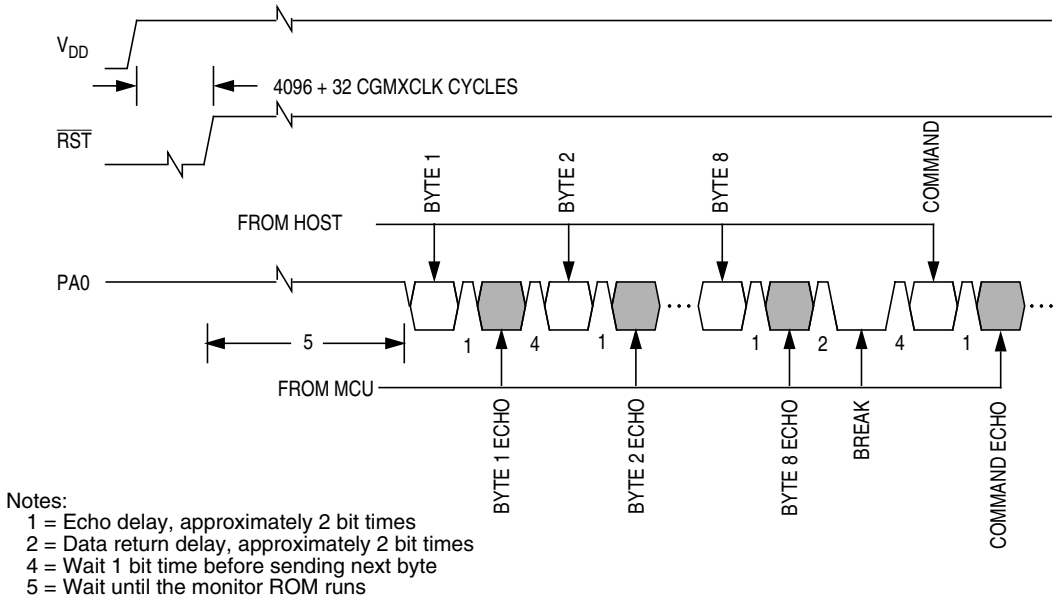


**Figure 18-17. Monitor Mode Entry Timing**

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $40 is set. If it is, then the correct security code has been entered and Flash can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the Flash module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

## 19.6 3.0-V DC Electrical Characteristics

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | | | | | |
| ($I_{Load}$ = –0.6 mA) all I/O pins | $V_{OH}$ | $V_{DD}$ – 0.3 | — | — | V |
| ($I_{Load}$ = –4.0 mA) all I/O pins | $V_{OH}$ | $V_{DD}$ – 1.0 | — | — | V |
| ($I_{Load}$ = –4.0 mA) pins PTC0–PTC4 only | $V_{OH}$ | $V_{DD}$ – 0.5 | — | — | V |
| Maximum combined $I_{OH}$ for port C, port E, port PTD0–PTD3 | $I_{OH1}$ | — | — | 30 | mA |
| Maximum combined $I_{OH}$ for port PTD4–PTD7, port A, port B | $I_{OH2}$ | — | — | 30 | mA |
| Maximum total $I_{OH}$ for all port pins | $I_{OHT}$ | — | — | 60 | mA |
| Output low voltage | | | | | |
| ($I_{Load}$ = 0.5 mA) all I/O pins | $V_{OL}$ | — | — | 0.3 | V |
| ($I_{Load}$ = 6.0 mA) all I/O pins | $V_{OL}$ | — | — | 1.0 | V |
| ($I_{Load}$ = 10.0 mA) pins PTC0–PTC4 only | $V_{OL}$ | — | — | 0.8 | V |
| Maximum combined $I_{OL}$ for port C, port E, port PTD0–PTD3 | $I_{OL1}$ | — | — | 30 | mA |
| Maximum combined $I_{OL}$ for port PTD4–PTD7, port A, port B | $I_{OL2}$ | — | — | 30 | mA |
| Maximum total $I_{OL}$ for all port pins | $I_{OLT}$ | — | — | 60 | mA |
| Input high voltage<br>All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1 | $V_{IH}$ | 0.7 × $V_{DD}$ | — | $V_{DD}$ | V |
| Input low voltage<br>All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1 | $V_{IL}$ | $V_{SS}$ | — | 0.3 × $V_{DD}$ | V |
| $V_{DD}$ supply current | | | | | |
| Run[3] | $I_{DD}$ | — | 4.5 | 8 | mA |
| Wait[4] | | — | 1.65 | 4 | mA |
| Stop[5] | | | | | |
| 25 °C | | — | 2 | — | µA |
| 25 °C with TBM enabled[6] | | — | 12 | — | µA |
| 25 °C with LVI and TBM enabled[6] | | — | 200 | — | µA |
| –40 °C to 85 °C with TBM enabled[6] | | — | 30 | — | µA |
| –40 °C to 85 °C with LVI and TBM enabled[6] | | — | 300 | — | µA |
| DC injection current[7] [8] [9] [10] | | | | | |
| Single pin limit | | | | | |
| $V_{in}$ > $V_{DD}$ | $I_{IC}$ | 0 | — | 2 | mA |
| $V_{in}$ < $V_{SS}$ | | 0 | — | –0.2 | |
| Total MCU limit, includes sum of all stressed pins | | | | | |
| $V_{in}$ > $V_{DD}$ | | 0 | — | 25 | |
| $V_{in}$ < $V_{SS}$ | | 0 | — | –5 | |
| I/O ports Hi-Z leakage current[11] | $I_{IL}$ | — | — | ±10 | µA |
| Input current | $I_{In}$ | — | — | ±1 | µA |

Contined on next page

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUMPLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.

5. THIS DIMENSION TO BE DETERMINED AT SEATING PLANE -C-.

6. THIS DIMENSION DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE PROTRUSION IS 0.25 PER SIDE, DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSTION, ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: | DOCUMENT NO: 98ASB42839B | REV: B |
|---|---|---|
| 44LD QFP,<br>10X10X2.0 PKG, 0.8 PITCH | CASE NUMBER: 824A-01 | 06 APR 2005 |
| | STANDARD: NON-JEDEC | |