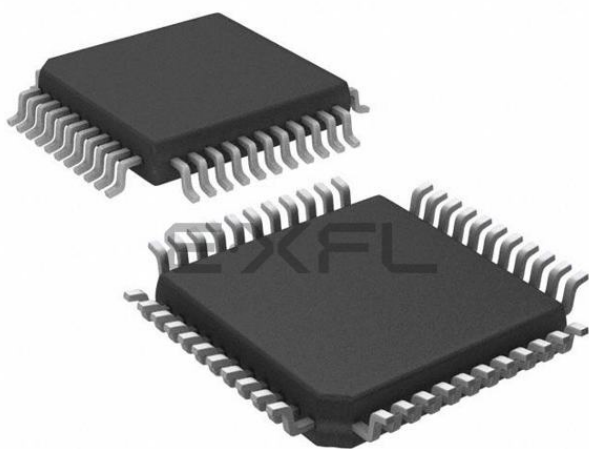




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	33
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gp32cfbr2

Table of Contents

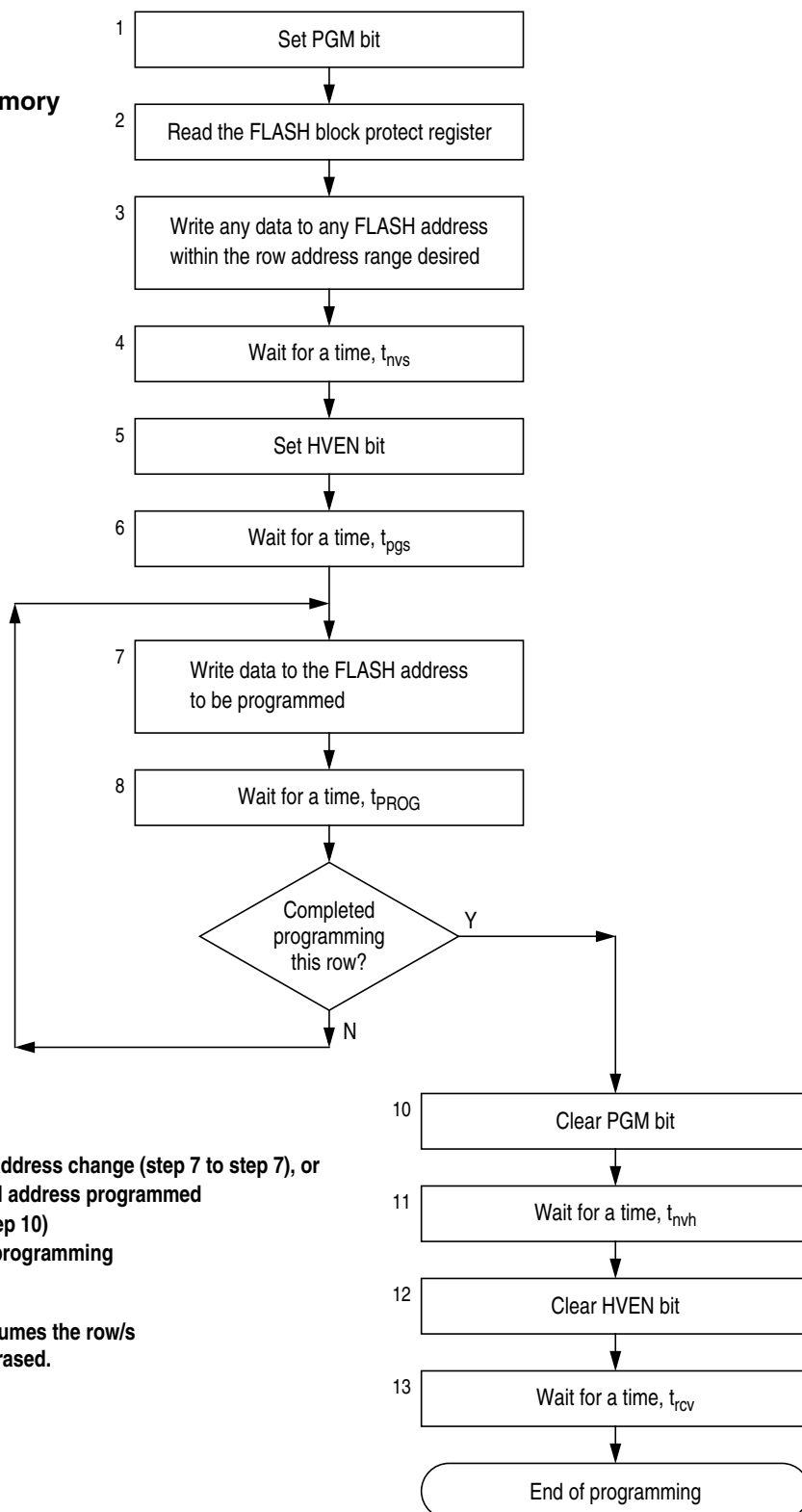
17.8	I/O Signals	208
17.9	I/O Registers	208
17.9.1	TIM Status and Control Register	208
17.9.2	TIM Counter Registers	209
17.9.3	TIM Counter Modulo Registers	210
17.9.4	TIM Channel Status and Control Registers	211
17.9.5	TIM Channel Registers	213

Chapter 18 Development Support

18.1	Introduction	215
18.2	Break Module (BRK)	215
18.2.1	Functional Description	215
18.2.1.1	Flag Protection During Break Interrupts	217
18.2.1.2	TIM During Break Interrupts	217
18.2.1.3	COP During Break Interrupts	217
18.2.2	Break Module Registers	217
18.2.2.1	Break Status and Control Register	218
18.2.2.2	Break Address Registers	218
18.2.2.3	SIM Break Status Register	219
18.2.2.4	SIM Break Flag Control Register	219
18.2.3	Low-Power Modes	219
18.3	Monitor Module (MON)	220
18.3.1	Functional Description	220
18.3.1.1	Normal Monitor Mode	225
18.3.1.2	Forced Monitor Mode	226
18.3.1.3	Monitor Vectors	226
18.3.1.4	Data Format	227
18.3.1.5	Break Signal	227
18.3.1.6	Baud Rate	227
18.3.1.7	Commands	227
18.3.2	Security	231

Chapter 19 Electrical Specifications

19.1	Introduction	233
19.2	Absolute Maximum Ratings	233
19.3	Functional Operating Range	234
19.4	Thermal Characteristics	234
19.5	5.0-V DC Electrical Characteristics	235
19.6	3.0-V DC Electrical Characteristics	237
19.7	5.0-V Control Timing	239
19.8	3.0-V Control Timing	240
19.9	Output High-Voltage Characteristics	241
19.10	Output Low-Voltage Characteristics	243
19.11	Typical Supply Currents	245

**Algorithm for programming
a row (64 bytes) of FLASH memory**

NOTE:

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time, $t_{\text{PROG max}}$.

This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 2-4. FLASH Programming Flowchart



4.6.2 ADC Analog Ground Pin (V_{SSAD})/ADC Voltage Reference Low Pin (V_{REFL})

The ADC analog portion uses V_{SSAD} as its ground pin. Connect the V_{SSAD} pin to the same voltage potential as V_{SS} .

NOTE

Route V_{SSAD} cleanly to avoid any offset errors.

4.6.3 ADC Voltage In (V_{ADIN})

V_{ADIN} is the input voltage signal from one of the eight ADC channels to the ADC module.

4.7 I/O Registers

These I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR)
- ADC data register (ADR)
- ADC clock register (ADCLK)

4.7.1 ADC Status and Control Register

Function of the ADC status and control register (ADSCR) is described here.

Address:	\$003C							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:	R							
Reset:	0	0	0	1	1	1	1	1
	R = Reserved							

Figure 4-2. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

In non-interrupt mode ($AIEN = 0$), COCO is a read-only bit that is set at the end of each conversion. COCO will stay set until cleared by a read of the ADC data register. Reset clears this bit.

In interrupt mode ($AIEN = 1$), COCO is a read-only bit that is not set at the end of a conversion. It always reads as a 0.

- 1 = Conversion completed ($AIEN = 0$)
- 0 = Conversion not completed ($AIEN = 0$) or CPU interrupt enabled ($AIEN = 1$)

NOTE

The write function of the COCO bit is reserved. When writing to the ADSCR register, always have a 0 in the COCO bit position.

AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when the data register is read or the status/control register is written. Reset clears the AIEN bit.

- 1 = ADC interrupt enabled
- 0 = ADC interrupt disabled

Temperature and processing also can affect acquisition time because the electrical characteristics of the PLL change. The part operates as specified as long as these influences stay within the specified limits. External factors, however, can cause drastic changes in the operation of the PLL. These factors include noise injected into the PLL through the filter capacitor, filter capacitor leakage, stray impedances on the circuit board, and even humidity or circuit board contamination.

5.8.3 Choosing a Filter

As described in 5.8.2 Parametric Influences on Reaction Time, the external filter network is critical to the stability and reaction time of the PLL. The PLL is also dependent on reference frequency and supply voltage.

Either of the filter networks in Figure 5-10 is recommended when using a 32.768kHz reference crystal. Figure 5-10 **(a)** is used for applications requiring better stability. Figure 5-10 **(b)** is used in low-cost applications where stability is not critical.

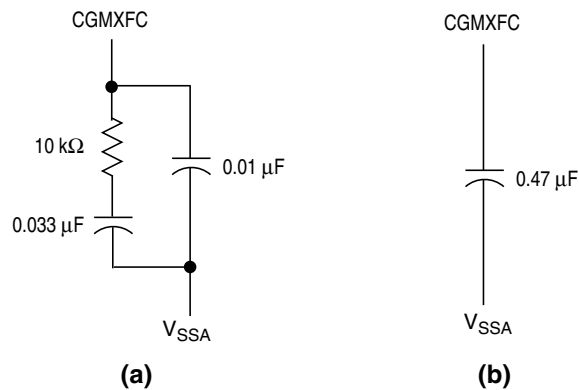


Figure 5-10. PLL Filter

LVI5OR3 — LVI 5-V or 3-V Operating Mode Bit

LVI5OR3 selects the voltage operating mode of the LVI module. (See Chapter 11 Low-Voltage Inhibit (LVI).) The voltage mode selected for the LVI should match the operating V_{DD} . See Chapter 19

Electrical Specifications for the LVI's voltage trip points for each of the modes.

1 = LVI operates in 5-V mode.

0 = LVI operates in 3-V mode.

SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of a 4096-CGMXCLK cycle delay.

1 = Stop mode recovery after 32 CGMXCLK cycles

0 = Stop mode recovery after 4096 CGMXCLK cycles

NOTE

Exiting stop mode by pulling reset will result in the long stop recovery.

If using an external crystal oscillator, do not set the SSREC bit.

NOTE

When the LVISTOP is enabled, the system stabilization time for power on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the enable time for the LVI. There is no period where the MCU is not protected from a low power condition. However, when using the short stop recovery configuration option, the 32-CGMXCLK delay is less than the LVI's turn-on time and there exists a period in startup where the LVI is not protecting the MCU.

STOP — STOP Instruction Enable Bit

STOP enables the STOP instruction.

1 = STOP instruction enabled

0 = STOP instruction treated as illegal opcode

COPD — COP Disable Bit

COPD disables the COP module. (See Chapter 7 Computer Operating Properly (COP).)

1 = COP module disabled

0 = COP module enabled

Table 8-1. Instruction Set Summary (Sheet 5 of 6)

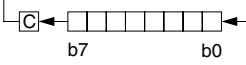
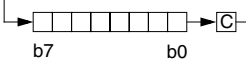
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z				
PULA	Pull A from Stack	$SP \leftarrow (SP + 1); \text{Pull (A)}$	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	$SP \leftarrow (SP + 1); \text{Pull (H)}$	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	$SP \leftarrow (SP + 1); \text{Pull (X)}$	–	–	–	–	–	INH	88		2
ROL <i>opr</i> ROLA ROLX ROL <i>opr</i> ,X ROL ,X ROL <i>opr</i> ,SP	Rotate Left through Carry		↑	–	–	–	↑	DIR INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR <i>opr</i> RORA RORX ROR <i>opr</i> ,X ROR ,X ROR <i>opr</i> ,SP	Rotate Right through Carry		↑	–	–	–	↑	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	$SP \leftarrow \$FF$	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	$SP \leftarrow (SP + 1); \text{Pull (CCR)}$ $SP \leftarrow (SP + 1); \text{Pull (A)}$ $SP \leftarrow (SP + 1); \text{Pull (X)}$ $SP \leftarrow (SP + 1); \text{Pull (PCH)}$ $SP \leftarrow (SP + 1); \text{Pull (PCL)}$	↑	↑	↑	↑	↑	INH	80		7
RTS	Return from Subroutine	$SP \leftarrow SP + 1; \text{Pull (PCH)}$ $SP \leftarrow SP + 1; \text{Pull (PCL)}$	–	–	–	–	–	INH	81		4
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> ,X SBC <i>opr</i> ,X SBC ,X SBC <i>opr</i> ,SP SBC <i>opr</i> ,SP	Subtract with Carry	$A \leftarrow (A) - (M) - (C)$	↑	–	–	–	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	$C \leftarrow 1$	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	$I \leftarrow 1$	–	–	1	–	–	INH	9B		2
STA <i>opr</i> STA <i>opr</i> STA <i>opr</i> ,X STA <i>opr</i> ,X STA ,X STA <i>opr</i> ,SP STA <i>opr</i> ,SP	Store A in M	$M \leftarrow (A)$	0	–	–	–	↑	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ff ff ee ff	3 4 4 3 2 4 5
STHX <i>opr</i>	Store H:X in M	$(M:M + 1) \leftarrow (H:X)$	0	–	–	–	↑	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	$I \leftarrow 0$; Stop Processing	–	–	0	–	–	INH	8E		1
STX <i>opr</i> STX <i>opr</i> STX <i>opr</i> ,X STX <i>opr</i> ,X STX ,X STX <i>opr</i> ,SP STX <i>opr</i> ,SP	Store X in M	$M \leftarrow (X)$	0	–	–	–	↑	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ff ff ee ff	3 4 4 3 2 4 5
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> ,X SUB <i>opr</i> ,X SUB ,X SUB <i>opr</i> ,SP SUB <i>opr</i> ,SP	Subtract	$A \leftarrow (A) - (M)$	↑	–	–	–	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5

Table 8-2. Opcode Map

MSB LSB	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	BRSET0 3 DIR	BSET0 2 DIR	BRA 2 REL	NEG 2 DIR	NEGA 1 INH	NEGX 1 INH	NEG 2 IX1	NEG 3 SP1	NEG 1 IX	RTI 1 INH	BGE 2 REL	SUB 2 IMM	SUB 2 DIR	SUB 3 EXT	SUB 3 IX2	SUB 4 SP2	SUB 2 IX1	SUB 3 SP1	SUB 1 IX
1	BRCLR0 3 DIR	BCLR0 2 DIR	BRN 2 REL	CBEQ 3 DIR	CBEQA 3 IMM	CBEQX 3 IMM	CBEQ 3 IX1+	CBEQ 4 SP1	CBEQ 2 IX+	RTS 1 INH	BLT 2 REL	CMP 2 IMM	CMP 2 DIR	CMP 3 EXT	CMP 3 IX2	CMP 4 SP2	CMP 2 IX1	CMP 3 SP1	CMP 1 IX
2	BRSET1 3 DIR	BSET1 2 DIR	BHI 2 REL		MUL 1 INH	DIV 1 INH	NSA 1 INH		DAA 1 INH		BGT 2 REL	SBC 2 IMM	SBC 2 DIR	SBC 3 EXT	SBC 3 IX2	SBC 4 SP2	SBC 2 IX1	SBC 3 SP1	SBC 1 IX
3	BRCLR1 3 DIR	BCLR1 2 DIR	BLS 2 REL	COM 2 DIR	COMA 1 INH	COMX 1 INH	COM 2 IX1	COM 3 SP1	COM 1 IX	SWI 1 INH	BLE 2 REL	CPX 2 IMM	CPX 2 DIR	CPX 3 EXT	CPX 3 IX2	CPX 4 SP2	CPX 2 IX1	CPX 3 SP1	CPX 1 IX
4	BRSET2 3 DIR	BSET2 2 DIR	BCC 2 REL	LSR 2 DIR	LSRA 1 INH	LSRX 1 INH	LSR 2 IX1	LSR 3 SP1	LSR 1 IX	TAP 1 INH	TXS 1 INH	AND 2 IMM	AND 2 DIR	AND 3 EXT	AND 3 IX2	AND 4 SP2	AND 2 IX1	AND 3 SP1	AND 1 IX
5	BRCLR2 3 DIR	BCLR2 2 DIR	BCS 2 REL	STHX 2 DIR	LDHX 3 IMM	LDHX 2 DIR	CPHX 3 IMM		CPHX 2 DIR	TPA 1 INH	TSX 1 INH	BIT 2 IMM	BIT 2 DIR	BIT 3 EXT	BIT 3 IX2	BIT 4 SP2	BIT 2 IX1	BIT 3 SP1	BIT 1 IX
6	BRSET3 3 DIR	BSET3 2 DIR	BNE 2 REL	ROR 2 DIR	RORA 1 INH	RORX 1 INH	ROR 2 IX1	ROR 3 SP1	ROR 1 IX	PULA 1 INH		LDA 2 IMM	LDA 2 DIR	LDA 3 EXT	LDA 3 IX2	LDA 4 SP2	LDA 2 IX1	LDA 3 SP1	LDA 1 IX
7	BRCLR3 3 DIR	BCLR3 2 DIR	BEQ 2 REL	ASR 2 DIR	ASRA 1 INH	ASRX 1 INH	ASR 2 IX1	ASR 3 SP1	ASR 1 IX	PSHA 1 INH	TAX 1 INH	AIS 2 IMM	STA 2 DIR	STA 3 EXT	STA 3 IX2	STA 4 SP2	STA 2 IX1	STA 3 SP1	STA 1 IX
8	BRSET4 3 DIR	BSET4 2 DIR	BHCC 2 REL	LSL 2 DIR	LSLA 1 INH	LSLX 1 INH	LSL 2 IX1	LSL 3 SP1	LSL 1 IX	PULX 1 INH	CLC 1 INH	EOR 2 IMM	EOR 2 DIR	EOR 3 EXT	EOR 3 IX2	EOR 4 SP2	EOR 2 IX1	EOR 3 SP1	EOR 1 IX
9	BRCLR4 3 DIR	BCLR4 2 DIR	BHCS 2 REL	ROL 2 DIR	ROLA 1 INH	ROLX 1 INH	ROL 2 IX1	ROL 3 SP1	ROL 1 IX	PSHX 1 INH	SEC 1 INH	ADC 2 IMM	ADC 2 DIR	ADC 3 EXT	ADC 3 IX2	ADC 4 SP2	ADC 2 IX1	ADC 3 SP1	ADC 1 IX
A	BRSET5 3 DIR	BSET5 2 DIR	BPL 2 REL	DEC 2 DIR	DECA 1 INH	DECX 1 INH	DEC 2 IX1	DEC 3 SP1	DEC 1 IX	PULH 1 INH	CLI 1 INH	ORA 2 IMM	ORA 2 DIR	ORA 3 EXT	ORA 3 IX2	ORA 4 SP2	ORA 2 IX1	ORA 3 SP1	ORA 1 IX
B	BRCLR5 3 DIR	BCLR5 2 DIR	BMI 2 REL	DBNZ 3 DIR	DBNZA 2 INH	DBNZX 2 INH	DBNZ 3 IX1	DBNZ 4 SP1	DBNZ 2 IX	PSHH 1 INH	SEI 1 INH	ADD 2 IMM	ADD 2 DIR	ADD 3 EXT	ADD 3 IX2	ADD 4 SP2	ADD 2 IX1	ADD 3 SP1	ADD 1 IX
C	BRSET6 3 DIR	BSET6 2 DIR	BMC 2 REL	INC 2 DIR	INCA 1 INH	INCX 1 INH	INC 2 IX1	INC 3 SP1	INC 1 IX	CLRH 1 INH	RSP 1 INH		JMP 2 DIR	JMP 3 EXT	JMP 3 IX2		JMP 2 IX1		JMP 1 IX
D	BRCLR6 3 DIR	BCLR6 2 DIR	BMS 2 REL	TST 2 DIR	TSTA 1 INH	TSTX 1 INH	TST 2 IX1	TST 3 SP1	TST 1 IX		NOP 1 INH	BSR 2 REL	JSR 2 DIR	JSR 3 EXT	JSR 3 IX2		JSR 2 IX1		JSR 1 IX
E	BRSET7 3 DIR	BSET7 2 DIR	BIL 2 REL		MOV 3 DD	MOV 2 DIX+	MOV 3 IMD		MOV 2 IX+D	STOP 1 INH	*	LDX 2 IMM	LDX 2 DIR	LDX 3 EXT	LDX 3 IX2	LDX 4 SP2	LDX 2 IX1	LDX 3 SP1	LDX 1 IX
F	BRCLR7 3 DIR	BCLR7 2 DIR	BIH 2 REL	CLR 2 DIR	CLRA 1 INH	CLRAX 1 INH	CLR 2 IX1	CLR 3 SP1	CLR 1 IX	WAIT 1 INH	TXA 1 INH	AIX 2 IMM	STX 2 DIR	STX 3 EXT	STX 3 IX2	STX 4 SP2	STX 2 IX1	STX 3 SP1	STX 1 IX

INH Inherent

REL Relative

SP1 Stack Pointer, 8-Bit Offset

IMM Immediate

IX Indexed, No Offset

SP2 Stack Pointer, 16-Bit Offset

DIR Direct

IX1 Indexed, 8-Bit Offset

IX+ Indexed, No Offset with

EXT Extended

IX2 Indexed, 16-Bit Offset

Post Increment

DD Direct-Direct

IMD Immediate-Direct

IX1+ Indexed, 1-Byte Offset with

IX+D Indexed-Direct

DIX+ Direct-Indexed

Post Increment

*Pre-byte for stack pointer indexed instructions

Low Byte of Opcode in Hexadecimal

MSB LSB	0
0	5 BRSET0 3 DIR

High Byte of Opcode in Hexadecimal

Cycles
Opcode Mnemonic
Number of Bytes / Addressing Mode

Chapter 9

External Interrupt (IRQ)

9.1 Introduction

The IRQ (external interrupt) module provides a maskable interrupt input.

9.2 Features

Features of the IRQ module include:

- A dedicated external interrupt pin $\overline{\text{IRQ}}$
- IRQ interrupt control bits
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Internal pullup device

9.3 Functional Description

A low level applied to the external interrupt request ($\overline{\text{IRQ}}$) pin can latch a CPU interrupt request. Figure 9-1 shows the structure of the IRQ module.

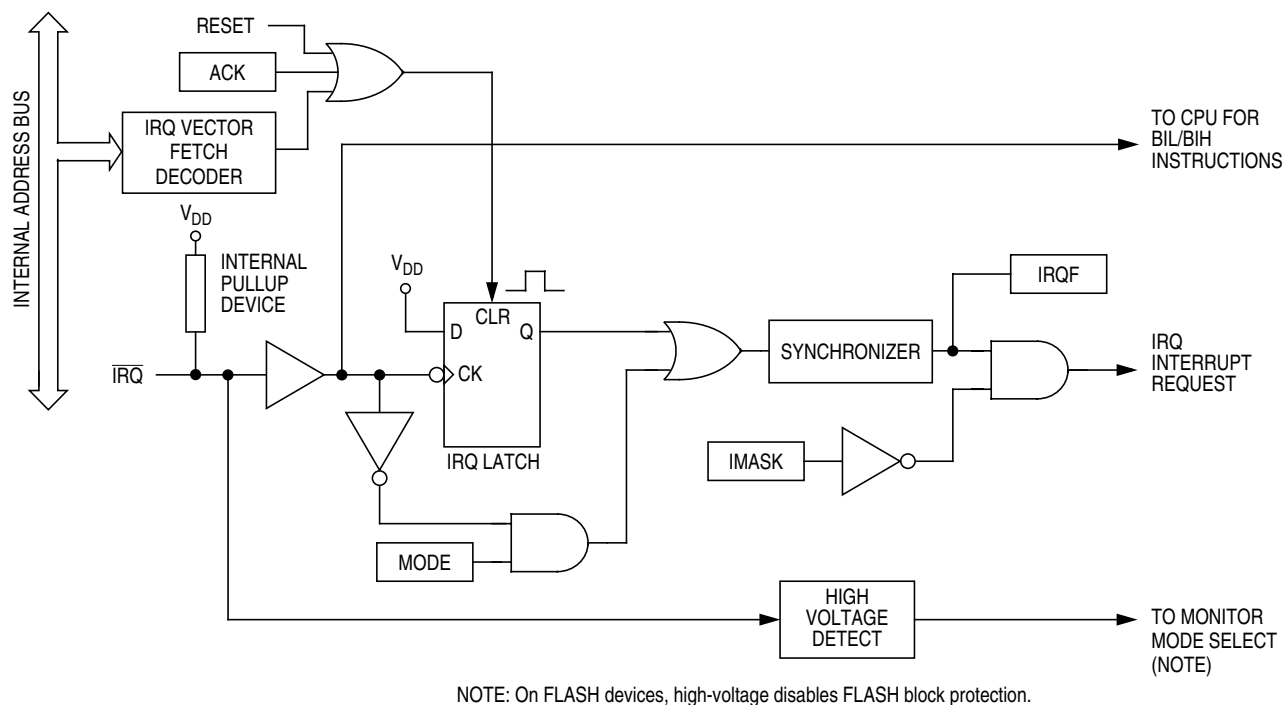


Figure 9-1. IRQ Module Block Diagram

Low-Voltage Inhibit (LVI)

LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are in the configuration register (CONFIG1). See 6.2 Functional Description for details of the LVI's configuration bits. Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR} , which causes the MCU to exit reset. See 14.3.2.5 Low-Voltage Inhibit (LVI) Reset for details of the interaction between the SIM and the LVI. The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR).

An LVI reset also drives the $\overline{RST}$ pin low to provide low-voltage protection to external peripheral devices.

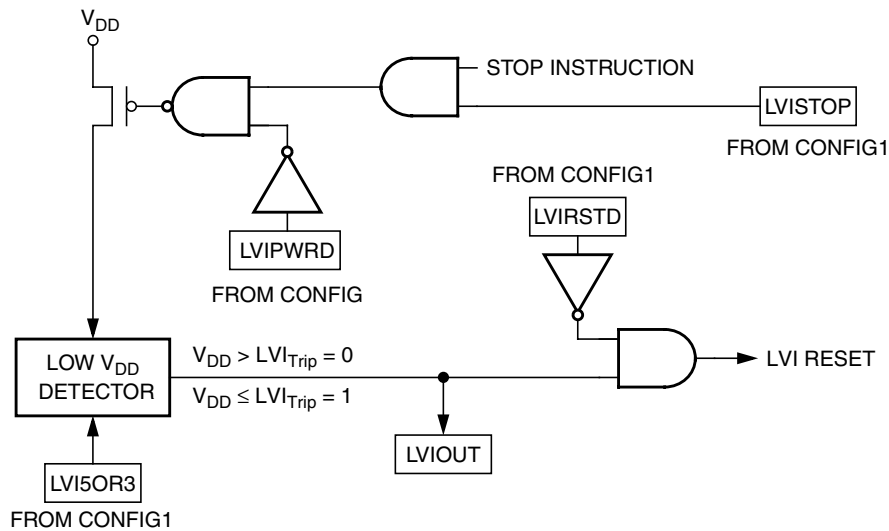


Figure 11-1. LVI Module Block Diagram

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$FE0C	LVI Status Register (LVISR)	Read: LVIOUT	0	0	0	0	0	0	0
		Write:							
		Reset:	0	0	0	0	0	0	0

= Unimplemented

Figure 11-2. LVI I/O Register Summary

11.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be at logic 0 to enable the LVI module, and the LVIRSTD bit must be at logic 1 to disable LVI resets.

11.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be at logic 0 to enable the LVI module and to enable LVI resets.

13.4.2.2 Character Transmission

During an SCI transmission, the transmit shift register shifts a character out to the PTE0/TxD pin. The SCI data register (SCDR) is the write-only buffer between the internal data bus and the transmit shift register. To initiate an SCI transmission:

1. Enable the SCI by writing a logic 1 to the enable SCI bit (ENSCI) in SCI control register 1 (SCC1).
2. Enable the transmitter by writing a logic 1 to the transmitter enable bit (TE) in SCI control register 2 (SCC2).
3. Clear the SCI transmitter empty bit by first reading SCI status register 1 (SCS1) and then writing to the SCDR.
4. Repeat step 3 for each subsequent transmission.

At the start of a transmission, transmitter control logic automatically loads the transmit shift register with a preamble of logic 1s. After the preamble shifts out, control logic transfers the SCDR data into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

The SCI transmitter empty bit, SCTE, in SCS1 becomes set when the SCDR transfers a byte to the transmit shift register. The SCTE bit indicates that the SCDR can accept new data from the internal data bus. If the SCI transmit interrupt enable bit, SCTIE, in SCC2 is also set, the SCTE bit generates a transmitter CPU interrupt request.

When the transmit shift register is not transmitting a character, the PTE0/TxD pin goes to the idle condition, logic 1. If at any time software clears the ENSCI bit in SCI control register 1 (SCC1), the transmitter and receiver relinquish control of the port E pins.

13.4.2.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCC2 loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCC1. As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next character.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be.

Receiving a break character has these effects on SCI registers:

- Sets the framing error bit (FE) in SCS1
- Sets the SCI receiver full bit (SCRF) in SCS1
- Clears the SCI data register (SCDR)
- Clears the R8 bit in SCC3
- Sets the break flag bit (BKF) in SCS2
- May set the overrun (OR), noise flag (NF), parity error (PE), or reception in progress flag (RPF) bits

13.4.2.4 Idle Characters

An idle character contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCC1. The preamble is a synchronizing idle character that begins every transmission.

13.4.3.3 Data Sampling

The receiver samples the PTE1/RxD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock is resynchronized at the following times (see Figure 13-6):

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

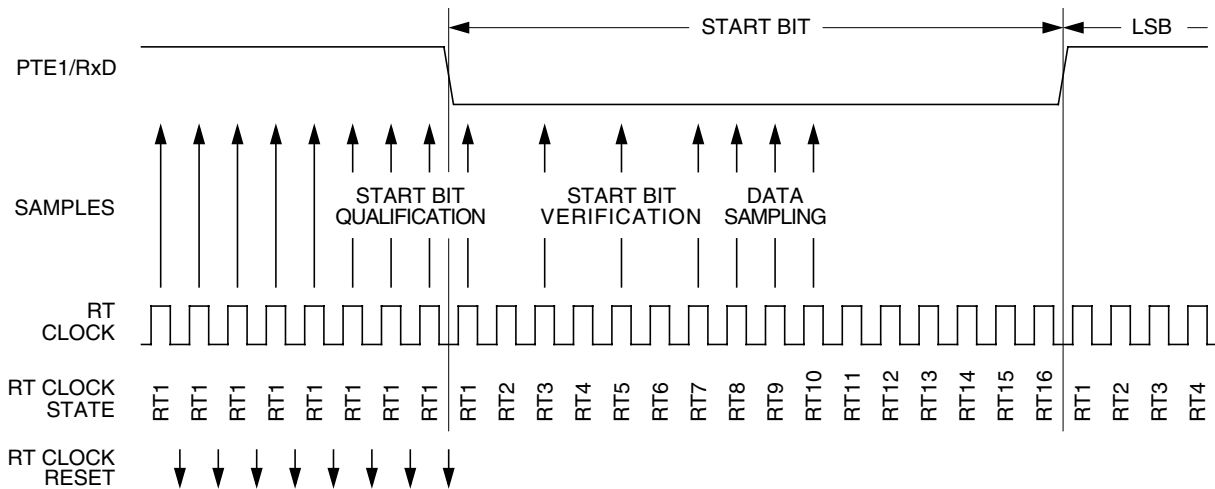


Figure 13-6. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-2 summarizes the results of the start bit verification samples.

Table 13-2. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

Start bit verification is not successful if any two of the three verification samples are logic 1s. If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

Fast Data Tolerance

Figure 13-8 shows how much a fast received character can be misaligned without causing a noise error or a framing error. The fast stop bit ends at RT10 instead of RT16 but is still there for the stop bit data samples at RT8, RT9, and RT10.

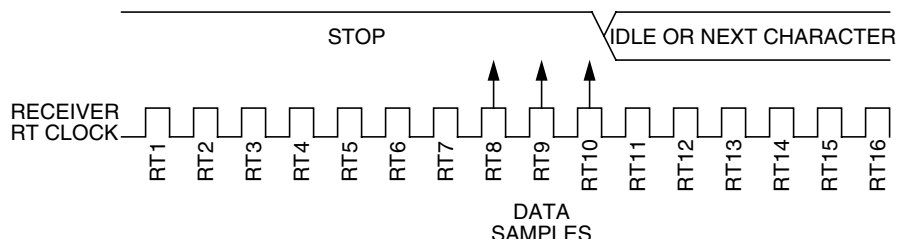


Figure 13-8. Fast Data

For an 8-bit character, data sampling of the stop bit takes the receiver
 $9 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 154 \text{ RT cycles}$.

With the misaligned character shown in Figure 13-8, the receiver counts 154 RT cycles at the point when the count of the transmitting device is
 $10 \text{ bit times} \times 16 \text{ RT cycles} = 160 \text{ RT cycles}$.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is

$$\left| \frac{154 - 160}{154} \right| \times 100 = 3.90\%$$

For a 9-bit character, data sampling of the stop bit takes the receiver
 $10 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 170 \text{ RT cycles}$.

With the misaligned character shown in Figure 13-8, the receiver counts 170 RT cycles at the point when the count of the transmitting device is
 $11 \text{ bit times} \times 16 \text{ RT cycles} = 176 \text{ RT cycles}$.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is

$$\left| \frac{170 - 176}{170} \right| \times 100 = 3.53\%$$

13.4.3.6 Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCC2 puts the receiver into a standby state during which receiver interrupts are disabled.



14.5.1.3 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. Table 14-3 summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

Table 14-3. Interrupt Sources

Priority	Interrupt Source	Interrupt Status Register Flag
Highest	Reset	—
	SWI instruction	—
	$\overline{\text{IRQ}}$ pin	IF1
	PLL	IF2
	TIM1 channel 0	IF3
	TIM1 channel 1	IF4
	TIM1 overflow	IF5
	TIM2 channel 0	IF6
	TIM2 channel 1	IF7
	TIM2 overflow	IF8
	SPI receiver full	IF9
	SPI transmitter empty	IF10
	SCI receive error	IF11
	SCI receive	IF12
	SCI transmit	IF13
	Keyboard	IF14
	ADC conversion complete	IF15
Lowest	Timebase module	IF16

Interrupt Status Register 1

Address:	\$FE04							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF6	IF5	IF4	IF3	IF2	IF1	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0
	R	= Reserved						

Figure 14-12. Interrupt Status Register 1 (INT1)

IF6–IF1 — Interrupt Flags 1–6

These flags indicate the presence of interrupt requests from the sources shown in Table 14-3.

1 = Interrupt request present

0 = No interrupt request present

Chapter 16

Timebase Module (TBM)

16.1 Introduction

This section describes the timebase module (TBM). The TBM will generate periodic interrupts at user selectable rates using a counter clocked by the external crystal clock. This TBM version uses 15 divider stages, eight of which are user selectable.

16.2 Features

Features of the TBM module include:

- Software programmable 1-Hz, 4-Hz, 16-Hz, 256-Hz, 512-Hz, 1024-Hz, 2048-Hz, and 4096-Hz periodic interrupt using external 32.768-kHz crystal
- Configurable for operation during stop mode to allow periodic wakeup from stop

16.3 Functional Description

NOTE

This module is designed for a 32.768-kHz oscillator.

This module can generate a periodic interrupt by dividing the crystal frequency, CGMXCLK. The counter is initialized to all 0s when TBON bit is cleared. The counter, shown in Figure 16-1, starts counting when the TBON bit is set. When the counter overflows at the tap selected by TBR2:TBR0, the TBIF bit gets set. If the TBIE bit is set, an interrupt request is sent to the CPU. The TBIF flag is cleared by writing a 1 to the TACK bit. The first time the TBIF flag is set after enabling the timebase module, the interrupt is generated at approximately half of the overflow period. Subsequent events occur at the exact period.

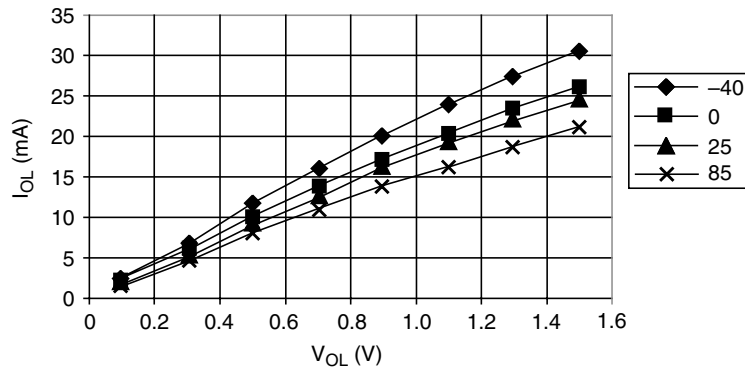
Electrical Specifications

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Pullup resistors (as input only) Ports PTA7/ $\overline{\text{KBD7}}$ –PTA0/ $\overline{\text{KBD0}}$, PTC6–PTC0, PTD7/T2CH1–PTD0/ $\overline{\text{SS}}$	R_{PU}	20	45	65	k Ω
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
Monitor mode entry voltage	V_{TST}	$V_{\text{DD}} + 2.5$	—	9	V
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	3.90	4.25	4.50	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	4.20	4.35	4.60	V
Low-voltage inhibit reset/recover hysteresis ($V_{\text{TRIPF}} + V_{\text{HYS}} = V_{\text{TRIPR}}$)	V_{HYS}	—	100	—	mV
POR rearm voltage ⁽¹²⁾	V_{POR}	0	—	100	mV
POR reset voltage ⁽¹³⁾	V_{PORRST}	0	700	800	mV
POR rise time ramp rate ⁽¹⁴⁾	R_{POR}	0.035	—	—	V/ms

Notes:

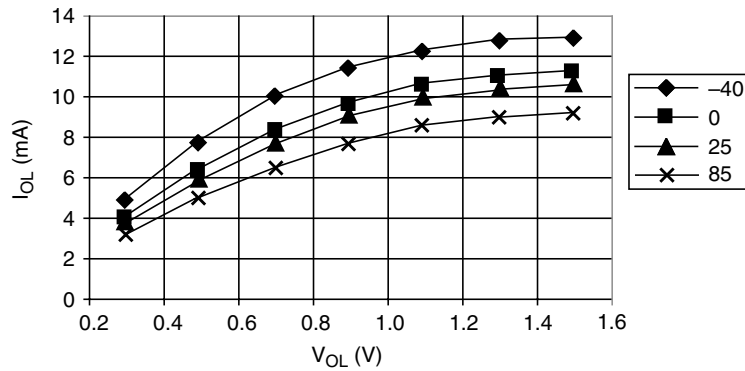
- $V_{\text{DD}} = 5.0 \text{ Vdc} \pm 10\%$, $V_{\text{SS}} = 0 \text{ Vdc}$, $T_{\text{A}} = T_{\text{L}}$ to T_{H} , unless otherwise noted
- Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
- Run (operating) I_{DD} measured using external square wave clock source ($f_{\text{OSC}} = 32.8 \text{ MHz}$). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. $C_{\text{L}} = 20 \text{ pF}$ on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD} . Measured with all modules enabled.
- Wait I_{DD} measured using external square wave clock source ($f_{\text{OSC}} = 32.8 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_{\text{L}} = 20 \text{ pF}$ on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD} . Measured with PLL and LVI enabled.
- Stop I_{DD} is measured with $\text{OSC1} = V_{\text{SS}}$.
- Stop I_{DD} with TBM enabled is measured using an external square wave clock source ($f_{\text{OSC}} = 32.8 \text{ MHz}$). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. All inputs configured as inputs.
- This parameter is characterized and not tested on each device.
- All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{\text{in}} > V_{\text{DD}}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- Pullups and pulldowns are disabled. Port B leakage is specified in 19.12 ADC Characteristics.
- Maximum is highest voltage that POR is guaranteed.
- Maximum is highest voltage that POR is possible.
- If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{\text{RST}}$ must be driven low externally until minimum V_{DD} is reached.

19.10 Output Low-Voltage Characteristics



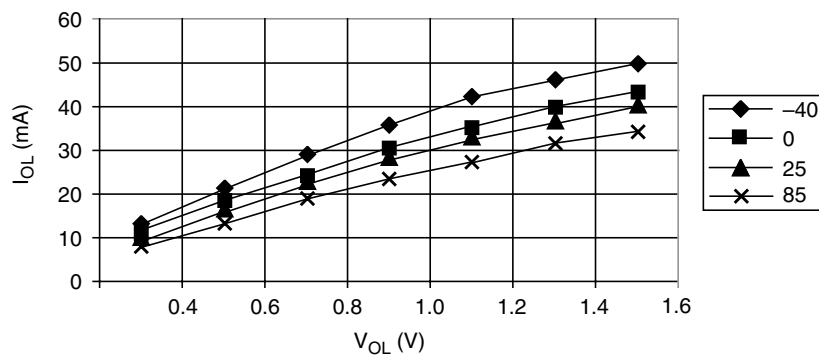
$V_{OL} < 0.4 \text{ V} @ I_{OL} = 1.6 \text{ mA}$
 $V_{OL} < 1.5 \text{ V} @ I_{OL} = 10.0 \text{ mA}$

Figure 19-8. Typical Low-Side Driver Characteristics – Port PTA7–PTA0 ($V_{DD} = 5.5 \text{ Vdc}$)



$V_{OL} < 0.3 \text{ V} @ I_{OL} = 0.5 \text{ mA}$
 $V_{OL} < 1.0 \text{ V} @ I_{OL} = 6.0 \text{ mA}$

Figure 19-9. Typical Low-Side Driver Characteristics – Port PTA7–PTA0 ($V_{DD} = 2.7 \text{ Vdc}$)



$V_{OL} < 1.0 \text{ V} @ I_{OL} = 15 \text{ mA}$

Figure 19-10. Typical Low-Side Driver Characteristics – Port PTC4–PTC0 ($V_{DD} = 4.5 \text{ Vdc}$)

19.12 ADC Characteristics

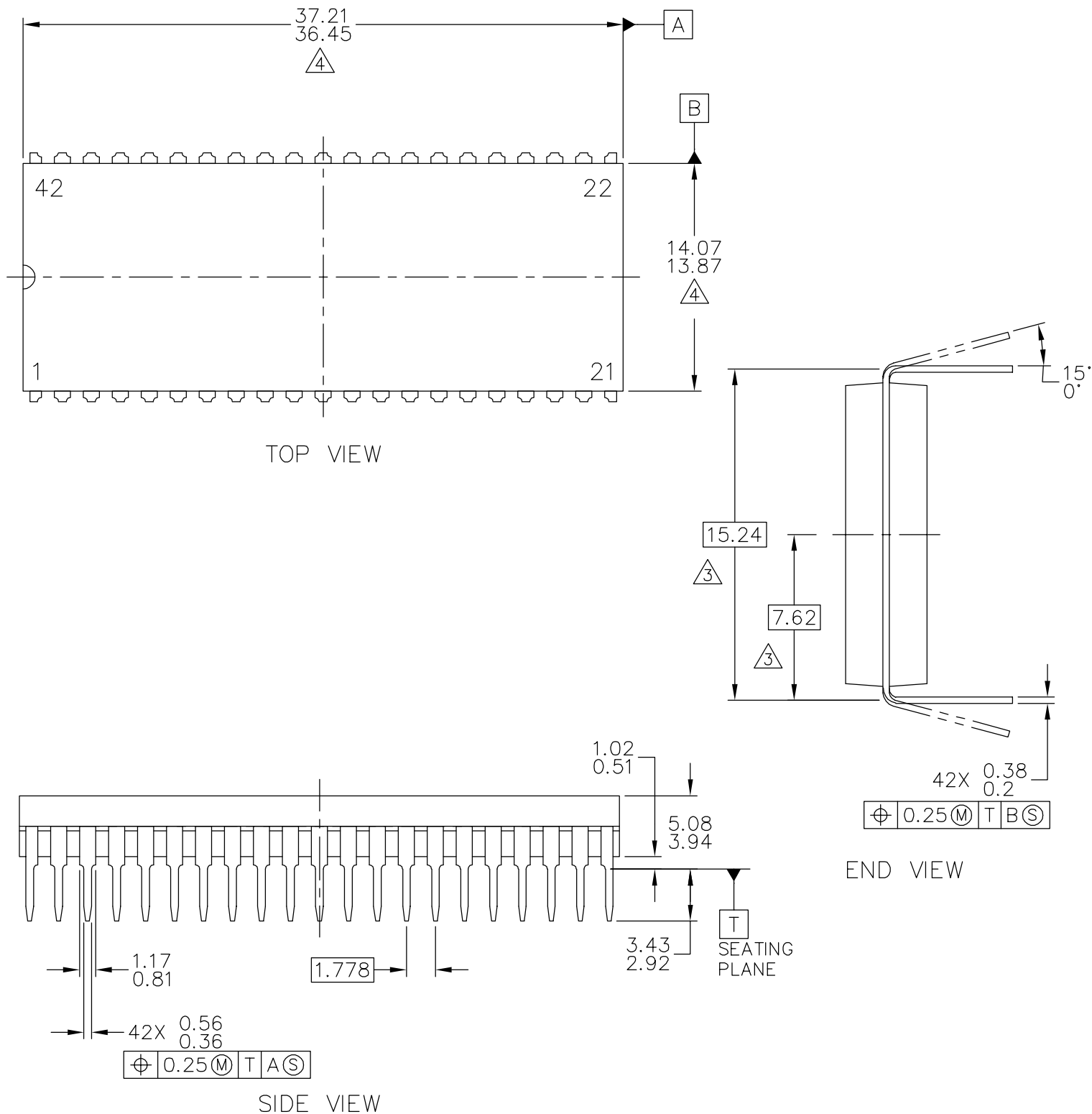
Characteristic ⁽¹⁾	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDAD}	2.7 (V_{DD} min)	5.5 (V_{DD} max)	V	V_{DDAD} should be tied to the same potential as V_{DD} via separate traces.
Input voltages	V_{ADIN}	0	V_{DDAD}	V	$V_{ADIN} \leq V_{REFH}$
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy ($V_{REFL} = 0$ V, $V_{REFH} = V_{DDAD} = 5$ V $\pm$ 10%)	A_{AD}	—	± 1	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.5	1.048	MHz	$t_{AIC} = 1/f_{ADIC}$, tested only at 1 MHz
Conversion range	R_{AD}	V_{REFL}	V_{REFH}	V	$V_{REFH} = V_{DDAD}$ $V_{REFL} = V_{SSAD}$
Power-up time	t_{ADPU}	16		t_{AIC} cycles	
Conversion time	t_{ADC}	16	17	t_{AIC} cycles	
Sample time ⁽²⁾	t_{ADS}	5	—	t_{AIC} cycles	
Zero input reading ⁽³⁾	Z_{ADI}	00	01	Hex	$V_{IN} = V_{REFL}$
Full-scale reading ⁽³⁾	F_{ADI}	FE	FF	Hex	$V_{IN} = V_{REFH}$
Input capacitance	C_{ADI}	—	(20) 8	pF	Not tested
Input leakage ⁽⁴⁾ Port B	—	—	± 1	μ A	
Notes:					

1. $V_{DD} = 5.0$ Vdc $\pm$ 10%, $V_{SS} = 0$ Vdc, $V_{DDAD} = 5.0$ Vdc $\pm$ 10%, $V_{SSAD} = 0$ Vdc, $V_{REFH} = 5.0$ Vdc $\pm$ 10%, $V_{REFL} = 0$

2. Source impedances greater than 10 k Ω adversely affect internal RC charging time during input sampling.

3. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.

4. The external system error caused by input leakage current is approximately equal to the product of R source and input current.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 42 LD PDIP			DOCUMENT NO: 98ASB42767B		REV: A
			CASE NUMBER: 858-01		24 OCT 2005
			STANDARD: NON-JEDEC		