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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3028f25v

Item	Page	Revision (See Manual for Details)
21.1.4 A/D Conversion Characteristics Table 21.8 A/D Conversion Characteristics	658	Conditions amended Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications) Table amended

Permissible signal-source impedance	$\phi \leq 13$ MHz	—	—	5	kΩ

21.1.5 D/A Conversion Characterisitcs Table 21.9 D/A Conversion Characteristics	659	Conditions amended Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)
21.2.1 Absolute Maximum Ratings Table 21.10 Absolute Maximum Ratings	660	Table and note amended

Operating temperature	T_{opr}	Regular specifications: –20 to +75*2	°C
		Wide-range specifications: –40 to +85*2	°C

2. The operating temperature range when programming and erasing the flash memory is: T_a = 0 to +75°C (regular specifications), T_a = 0 to +85°C (wide-range specifications).

21.2.2 DC Characteristics Table 21.11 DC Characteristics	661, 662	Conditions amended Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC}*1 = 3.0 V to 3.6 V, V_{REF}*1 = 3.0 V to AV_{CC}, V_{SS} = AV_{SS}*1 = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications) [Programming/erasing conditions: T_a = 0°C to +75°C (regular specifications), T_a = 0°C to +85°C (wide-range specifications)] Table amended

Input capacitance	FWE	
	NMI	
	All input pins except NMI, and FWE	

Pin No.	Pin Name						
FP-100B TFP-100B	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
55	A_{18}	A_{18}	A_{18}	A_{18}	$P5_2/A_{18}$	$P5_2$	$P5_2$
56	A_{19}	A_{19}	A_{19}	A_{19}	$P5_3/A_{19}$	$P5_3$	$P5_3$
57	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
58	$P6_0/\overline{WAIT}$	$P6_0/\overline{WAIT}$	$P6_0/\overline{WAIT}$	$P6_0/\overline{WAIT}$	$P6_0/\overline{WAIT}$	$P6_0$	$P6_0$
59	$P6_1/\overline{BREQ}$	$P6_1/\overline{BREQ}$	$P6_1/\overline{BREQ}$	$P6_1/\overline{BREQ}$	$P6_1/\overline{BREQ}$	$P6_1$	$P6_1$
60	$P6_2/\overline{BACK}$	$P6_2/\overline{BACK}$	$P6_2/\overline{BACK}$	$P6_2/\overline{BACK}$	$P6_2/\overline{BACK}$	$P6_2$	$P6_2$
61	ϕ	ϕ	ϕ	ϕ	$P6_7/\phi$	$P6_7/\phi$	$P6_7/\phi$
62	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$
63	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
64	NMI	NMI	NMI	NMI	NMI	NMI	NMI
65	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
66	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
67	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL
68	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
69	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$P6_3$	$P6_3$
70	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$P6_4$	$P6_4$
71	$\overline{HWR}$	$\overline{HWR}$	$\overline{HWR}$	$\overline{HWR}$	$\overline{HWR}$	$P6_5$	$P6_5$
72	$\overline{LWR}$	$\overline{LWR}$	$\overline{LWR}$	$\overline{LWR}$	$\overline{LWR}$	$P6_6$	$P6_6$
73	MD_0	MD_0	MD_0	MD_0	MD_0	MD_0	MD_0
74	MD_1	MD_1	MD_1	MD_1	MD_1	MD_1	MD_1
75	MD_2	MD_2	MD_2	MD_2	MD_2	MD_2	MD_2
76	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}
77	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}
78	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$
79	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$
80	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$
81	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$
82	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$
83	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$
84	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$	$P7_6/AN_6/DA_0$
85	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$	$P7_7/AN_7/DA_1$
86	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}
87	$P8_0/\overline{IRQ_0}/\overline{RFSH}$	$P8_0/\overline{IRQ_0}/\overline{RFSH}$	$P8_0/\overline{IRQ_0}/\overline{RFSH}$	$P8_0/\overline{IRQ_0}/\overline{RFSH}$	$P8_0/\overline{IRQ_0}/\overline{RFSH}$	$P8_0/\overline{IRQ_0}$	$P8_0/\overline{IRQ_0}$

4.4 Trap Instruction

Trap instruction exception handling starts when a TRAPA instruction is executed. If the UE bit is set to 1 in the system control register (SYSCR), the exception handling sequence sets the I bit to 1 in CCR. If the UE bit is 0, the I and UI bits are both set to 1. The TRAPA instruction fetches a start address from a vector table entry corresponding to a vector number from 0 to 3, which is specified in the instruction code.

4.6 Notes on Stack Usage

When accessing word data or longword data, the H8/3028 Group regards the lowest address bit as 0. The stack should always be accessed by word access or longword access, and the value of the stack pointer (SP, ER7) should always be kept even.

Use the following instructions to save registers:

PUSH.W Rn (or MOV.W Rn, @–SP)

PUSH.L ERn (or MOV.L ERn, @–SP)

Use the following instructions to restore registers:

POP.W Rn (or MOV.W @SP+, Rn)

POP.L ERn (or MOV.L @SP+, ERn)

Setting SP to an odd value may lead to a malfunction. Figure 4.7 shows an example of what happens when the SP value is odd.

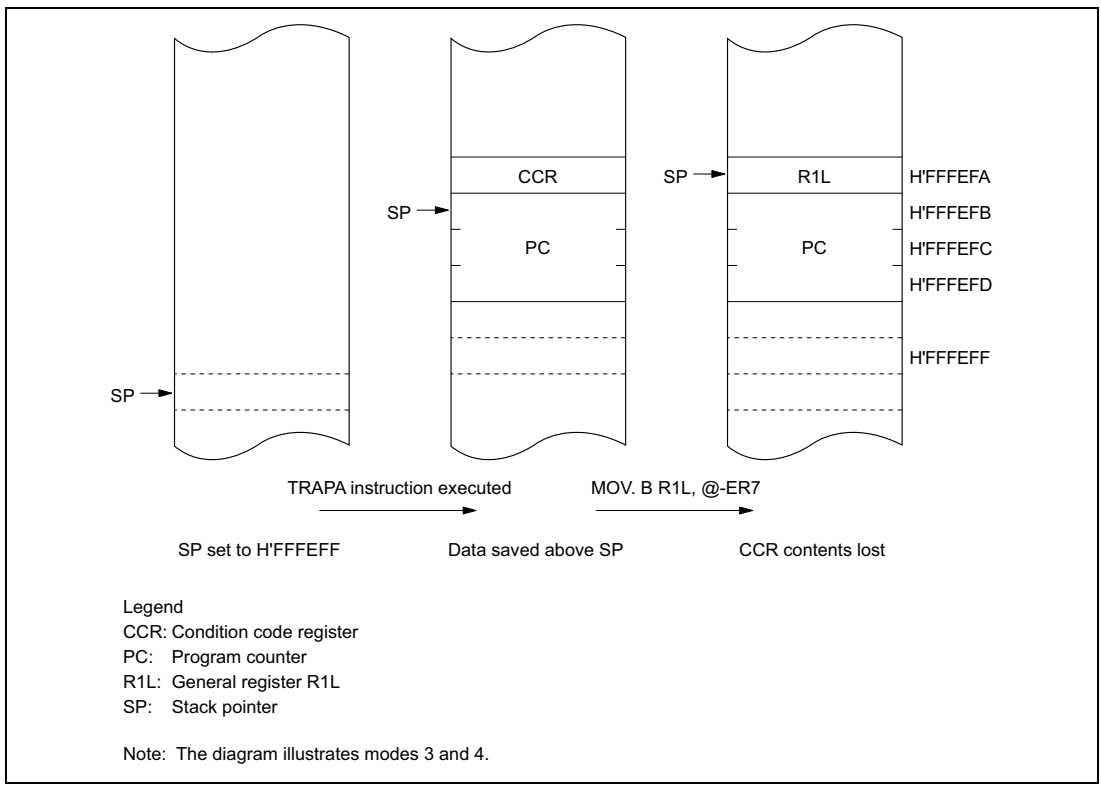


Figure 4.7 Operation when SP Value is Odd

Bit 7 MXC1	Bit 6 MXC0	Description		
0	0	Column address: 8 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_8
			16-bit access space	A_{19} to A_9
		Modes 3, 4, 5	8-bit access space	A_{23} to A_8
			16-bit access space	A_{23} to A_9
	1	Column address: 9 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_9
			16-bit access space	A_{19} to A_{10}
		Modes 3, 4, 5	8-bit access space	A_{23} to A_9
			16-bit access space	A_{23} to A_{10}
1	0	Column address: 10 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_{10}
			16-bit access space	A_{19} to A_{11}
		Modes 3, 4, 5	8-bit access space	A_{23} to A_{10}
			16-bit access space	A_{23} to A_{11}
	1	Illegal setting		

Bit 5—$\overline{\text{CAS}}$ Output Pin Select (CSEL): Selects the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ output pins when areas 2 to 5 are designated as DRAM space.

Bit 5 CSEL	Description	
0	PB4 and PB5 selected as $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ output pins	(Initial value)
1	$\overline{\text{HWR}}$ and $\overline{\text{LWR}}$ selected as $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ output pins	

Bit 4—Refresh Cycle Enable (RCYCE): Enables or disables CAS-before-RAS refresh cycle insertion. When none of areas 2 to 5 has been designated as DRAM space, refresh cycles are not inserted regardless of the setting of this bit.

Bit 4 RCYCE	Description	
0	Refresh cycles disabled	(Initial value)
1	DRAM refresh cycles enabled	

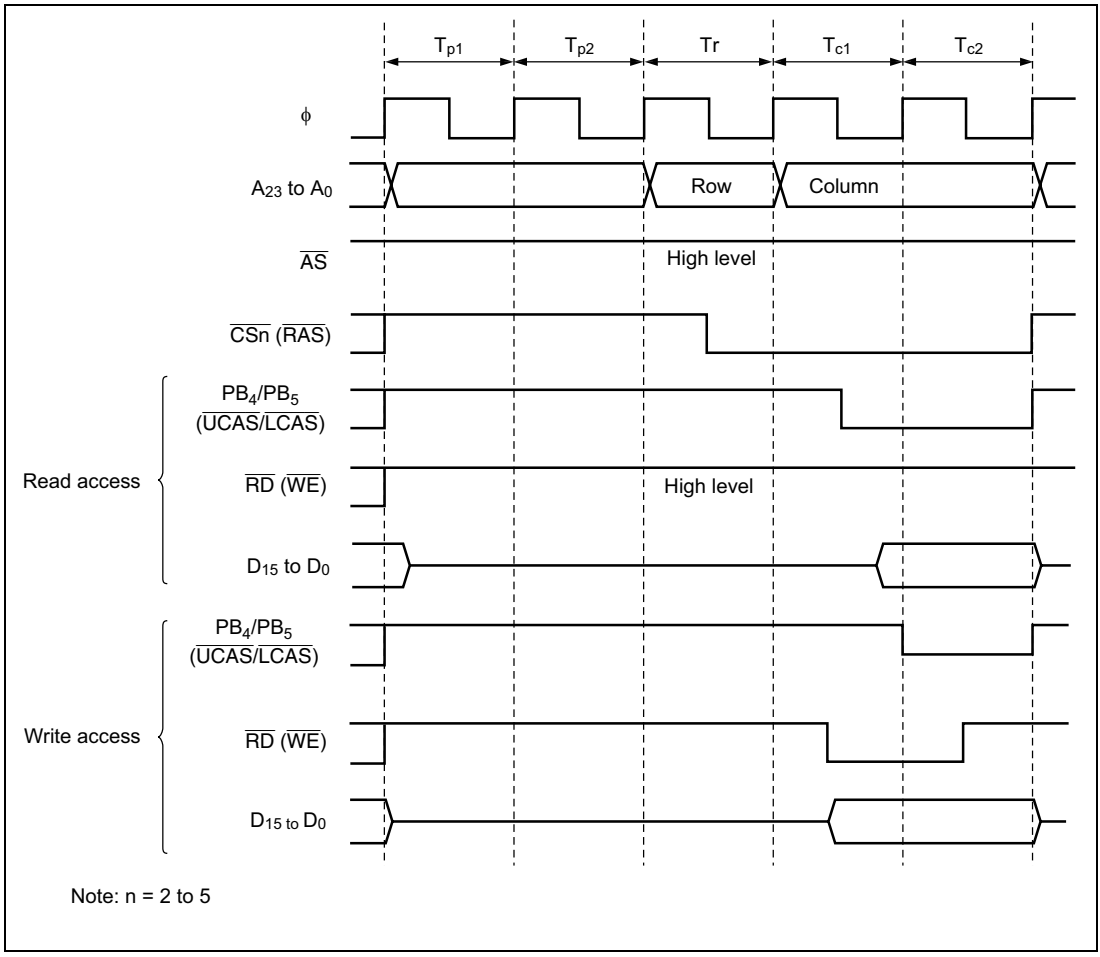


Figure 6.19 Timing with Two Precharge States (CSEL = 0 in DRCRB)

6.5.8 Wait Control

In a DRAM access cycle, wait states can be inserted (1) between the T_r state and T_{c1} state, and (2) between the T_{c1} state and T_{c2} state.

Insertion of T_{rw} Wait State between T_r and T_{c1}: One T_{rw} state can be inserted between T_r and T_{c1} by setting the RCW bit to 1 in DRCRB.

Insertion of T_w Wait State(s) between T_{c1} and T_{c2}: When the bit in ASTCR corresponding to an area designated as DRAM space is set to 1, from 0 to 3 wait states can be inserted between the T_{c1} state and T_{c2} state by means of settings in WCRH and WCRL.

Figure 6.20 shows an example of the timing for wait state insertion.

Table 8.20 Port A Pin Functions (Modes 3, 4, and 5)

Pin	Pin Functions and Selection Method
$PA_7/TP_7/TIOCB_2/A_{20}$	Modes 3 and 4: Always used as A_{20} output.

Pin function	A_{20} output

Mode 5:
Bit PWM2 in TMDR, bits IOB2 to IOB0 in TIOR2, bit NDER7 in NDERA, bit A20E in BRCR, and bit PA_7DDR select the pin function as follows.

A20E	1				0
16-bit timer channel 2 settings	(1) in table below	(2) in table below			—
PA_7DDR	—	0	1	1	—
NDER7	—	—	0	1	—
Pin function	$TIOCB_2$ output	PA_7 input	PA_7 output	TP_7 output	A_{20} output
		$TIOCB_2$ input*			

Note: * $TIOCB_2$ input when IOB2 = 1 and PWM2 = 0.

16-bit timer channel 2 settings	(2)	(1)		(2)
IOB2	0			1
IOB1	0	0	1	—
IOB0	0	1	—	—

11.3.4 Non-Overlapping TPC Output

Sample Setup Procedure for Non-Overlapping TPC Output: Figure 11.6 shows a sample procedure for setting up non-overlapping TPC output.

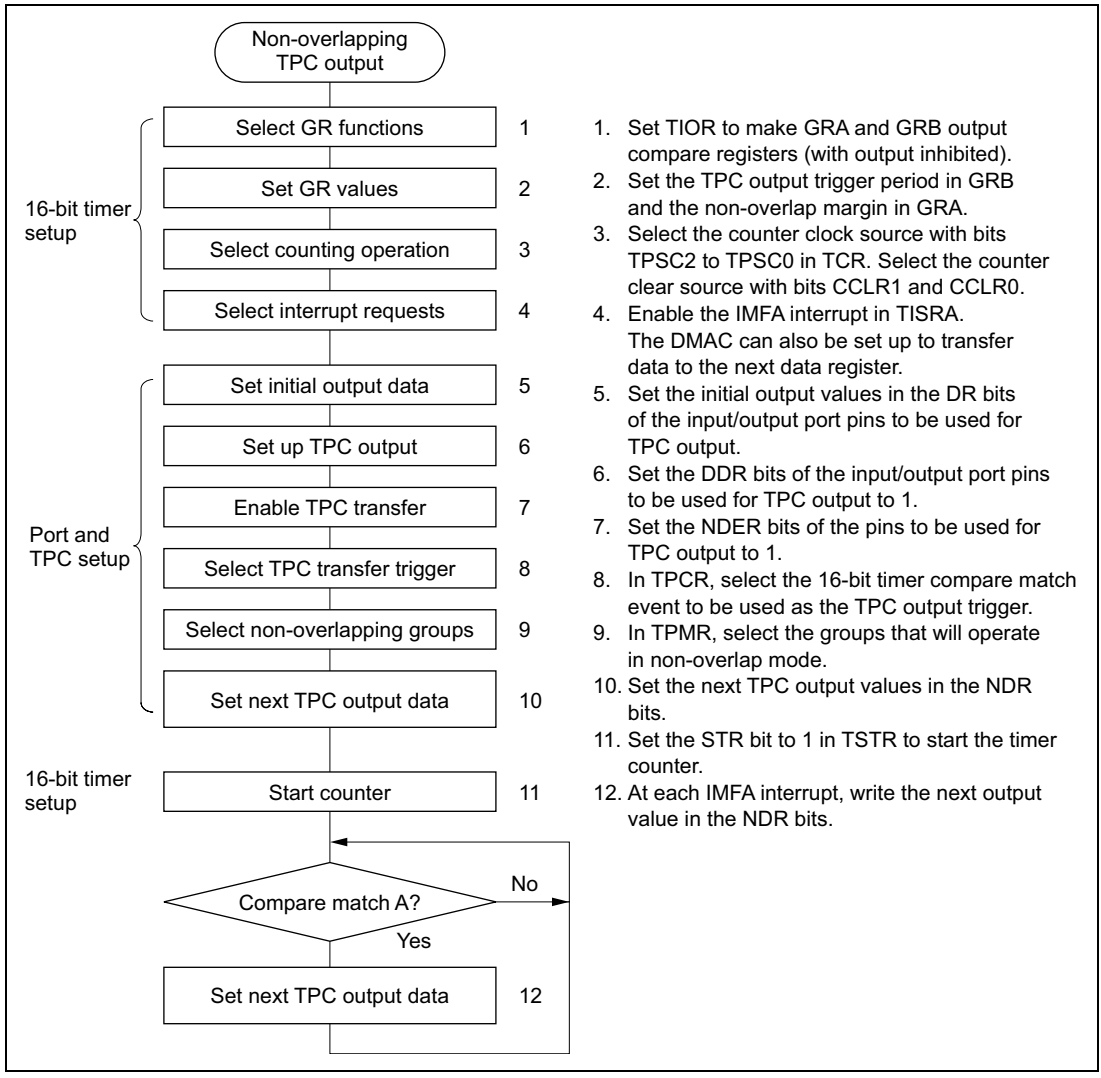


Figure 11.6 Setup Procedure for Non-Overlapping TPC Output (Example)

Bit 5—Overrun Error (ORER): Indicates that data reception ended abnormally due to an overrun error.

Bit 5 ORER	Description	
0	Receiving is in progress or has ended normally[*1]	(Initial value)
	[Clearing conditions]	
	• The chip is reset or enters standby mode	
	• Read ORER when ORER = 1, then write 0 in ORER	
1	A receive overrun error occurred[*2]	
	[Setting condition]	
	Reception of the next serial data ends when RDRF = 1	

Notes: 1. Clearing the RE bit to 0 in SCR does not affect the ORER flag, which retains its previous value.
2. RDR continues to hold the receive data prior to the overrun error, so subsequent receive data is lost. Serial receiving cannot continue while the ORER flag is set to 1. In synchronous mode, serial transmitting is also disabled.

Bit 4—Framing Error (FER)/Error Signal Status (ERS): The function of this bit differs for the normal serial communication interface and for the smart card interface. Its function is switched with the SMIF bit in SCMR.

For serial communication interface (SMIF bit in SCMR cleared to 0): Indicates that data reception ended abnormally due to a framing error in asynchronous mode.

Bit 4 FER	Description	
0	Receiving is in progress or has ended normally[*1]	(Initial value)
	[Clearing conditions]	
	• The chip is reset or enters standby mode	
	• Read FER when FER = 1, then write 0 in FER	
1	A receive framing error occurred[*2]	
	[Setting condition]	
	The stop bit at the end of the receive data is checked and found to be 0	

Notes: 1. Clearing the RE bit to 0 in SCR does not affect the FER flag, which retains its previous value.
2. When the stop bit length is 2 bits, only the first bit is checked. The second stop bit is not checked. When a framing error occurs the SCI transfers the receive data into RDR but does not set the RDRF flag. Serial receiving cannot continue while the FER flag is set to 1. In synchronous mode, serial transmitting is also disabled.

14.3.6 Transmitting and Receiving Data

Initialization: Before transmitting or receiving data, the smart card interface must be initialized as described below. Initialization is also necessary when switching from transmit mode to receive mode, or vice versa.

1. Clear the TE and RE bits to 0 in the serial control register (SCR).
2. Clear error flags FER/ERS, PER, and ORER to 0 in the serial status register (SSR).
3. Set the parity bit (O/$\overline{E}$) and baud rate generator select bits (CKS1 and CKS0) in the serial mode register (SMR). Clear the C/$\overline{A}$, CHR, and MP bits to 0, and set the STOP and PE bits to 1.
4. Set the SMIF, SDIR, and SINV bits in the smart card mode register (SCMR).
   When the SMIF bit is set to 1, the TxD pin and RxD pin are both switched from port to SCI pin functions and go to the high-impedance state.
5. Set a value corresponding to the desired bit rate in the bit rate register (BRR).
6. Set the CKE0 bit in SCR. Clear the TIE, RIE, TE, RE, MPIE, TEIE, and CKE1 bits to 0. If the CKE0 bit is set to 1, the clock is output from the SCK pin.
7. Wait at least one bit interval, then set the TIE, RIE, TE, and RE bits in SCR. Do not set the TE bit and RE bit at the same time, except for self-diagnosis.

Transmitting Serial Data: As data transmission in smart card mode involves error signal sampling and retransmission processing, the processing procedure is different from that for the normal SCI. Figure 14.5 shows a sample transmission processing flowchart.

1. Perform smart card interface mode initialization as described in Initialization above.
2. Check that the FER/ERS error flag is cleared to 0 in SSR.
3. Repeat steps 2 and 3 until it can be confirmed that the TEND flag is set to 1 in SSR.
4. Write the transmit data in TDR, clear the TDRE flag to 0, and perform the transmit operation. The TEND flag is cleared to 0.
5. To continue transmitting data, go back to step 2.
6. To end transmission, clear the TE bit to 0.

The above processing may include interrupt handling DMA transfer.

If transmission ends and the TEND flag is set to 1 while the TIE bit is set to 1 and interrupt requests are enabled, a transmit-data-empty interrupt (TXI) will be requested. If an error occurs in transmission and the ERS flag is set to 1 while the RIE bit is set to 1 and interrupt requests are enabled, a transmit/receive-error interrupt (ERI) will be requested.

The timing of TEND flag setting depends on the GM bit in SMR (see figure 14.4).

If the TXI interrupt activates the DMAC, the number of bytes designated in the DMAC can be transmitted automatically, including automatic retransmission.

Examples of Operation in GSM Mode: When switching between smart card interface mode and software standby mode, use the following procedures to maintain the clock duty cycle.

- Switching from smart card interface mode to software standby mode

1. Set the $P9_4$ data register (DR) and data direction register (DDR) to the values for the fixed output state in software standby mode.
2. Write 0 in the TE and RE bits in the serial control register (SCR) to stop transmit/receive operations. At the same time, set the CKE1 bit to the value for the fixed output state in software standby mode.
3. Write 0 in the CKE0 bit in SCR to stop the clock.
4. Wait for one serial clock cycle. During this period, the duty cycle is preserved and clock output is fixed at the specified level.
5. Write H'00 in the serial mode register (SMR) and smart card mode register (SCMR).
6. Make the transition to the software standby state.

- Returning from software standby mode to smart card interface mode

1. Clear the software standby state.
2. Set the CKE1 bit in SCR to the value for the fixed output state at the start of software standby (the current $P9_4$ pin state).
3. Set smart card interface mode and output the clock. Clock signal generation is started with the normal duty cycle.

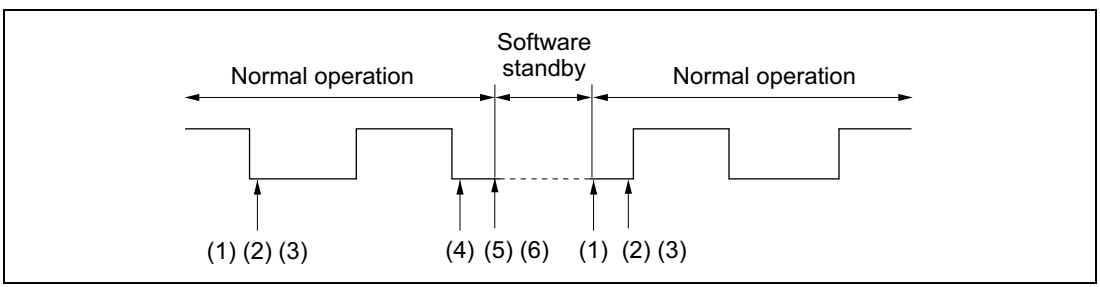


Figure 14.10 Procedure for Stopping and Restarting the Clock

Use the following procedure to secure the clock duty cycle after powering on.

1. The initial state is port input and high impedance. Use pull-up or pull-down resistors to fix the potential.
2. Fix at the output specified by the CKE1 bit in SCR.
3. Set SMR and SCMR, and switch to smart card interface mode operation.
4. Set the CKE0 bit to 1 in SCR to start clock output.

15.5 Interrupts

The A/D converter generates an interrupt (ADI) at the end of A/D conversion. The ADI interrupt request can be enabled or disabled by the ADIE bit in ADCSR. The ADI interrupt request can be designated as a DMAC activation source. In this case, an interrupt request is not sent to the CPU.

15.6 Usage Notes

When using the A/D converter, note the following points:

1. Analog Input Voltage Range: During A/D conversion, the voltages input to the analog input pins should be in the range $AV_{SS} \leq AN_n \leq V_{REF}$.

2. Relationships of AV_{CC} and AV_{SS} to V_{CC} and V_{SS}: AV_{CC}, AV_{SS}, V_{CC}, and V_{SS} should be related as follows: $AV_{SS} = V_{SS}$. AV_{CC} and AV_{SS} must not be left open, even if the A/D converter is not used.

3. V_{REF} Programming Range: The reference voltage input at the V_{REF} pin should be in the range $V_{REF} \leq AV_{CC}$.

4. Note on Board Design: In board layout, separate the digital circuits from the analog circuits as much as possible. Particularly avoid layouts in which the signal lines of digital circuits cross or closely approach the signal lines of analog circuits. Induction and other effects may cause the analog circuits to operate incorrectly, or may adversely affect the accuracy of A/D conversion. The analog input signals (AN_0 to AN_7), analog reference voltage (V_{REF}), and analog supply voltage (AV_{CC}) must be separated from digital circuits by the analog ground (AV_{SS}). The analog ground (AV_{SS}) should be connected to a stable digital ground (V_{SS}) at one point on the board.

5. Note on Noise: To prevent damage from surges and other abnormal voltages at the analog input pins (AN_0 to AN_7) and analog reference voltage pin (V_{REF}), connect a protection circuit like the one in figure 15.7 between AV_{CC} and AV_{SS}. The bypass capacitors connected to AV_{CC} and V_{REF} and the filter capacitors connected to AN_0 to AN_7 must be connected to AV_{SS}. If filter capacitors like the ones in figure 15.7 are connected, the voltage values input to the analog input pins (AN_0 to AN_7) will be smoothed, which may give rise to error. Error can also occur if A/D conversion is frequently performed in scan mode so that the current that charges and discharges the capacitor in the sample-and-hold circuit of the A/D converter becomes greater than that input to the analog input pins via input impedance Rin. The circuit constants should therefore be selected carefully.

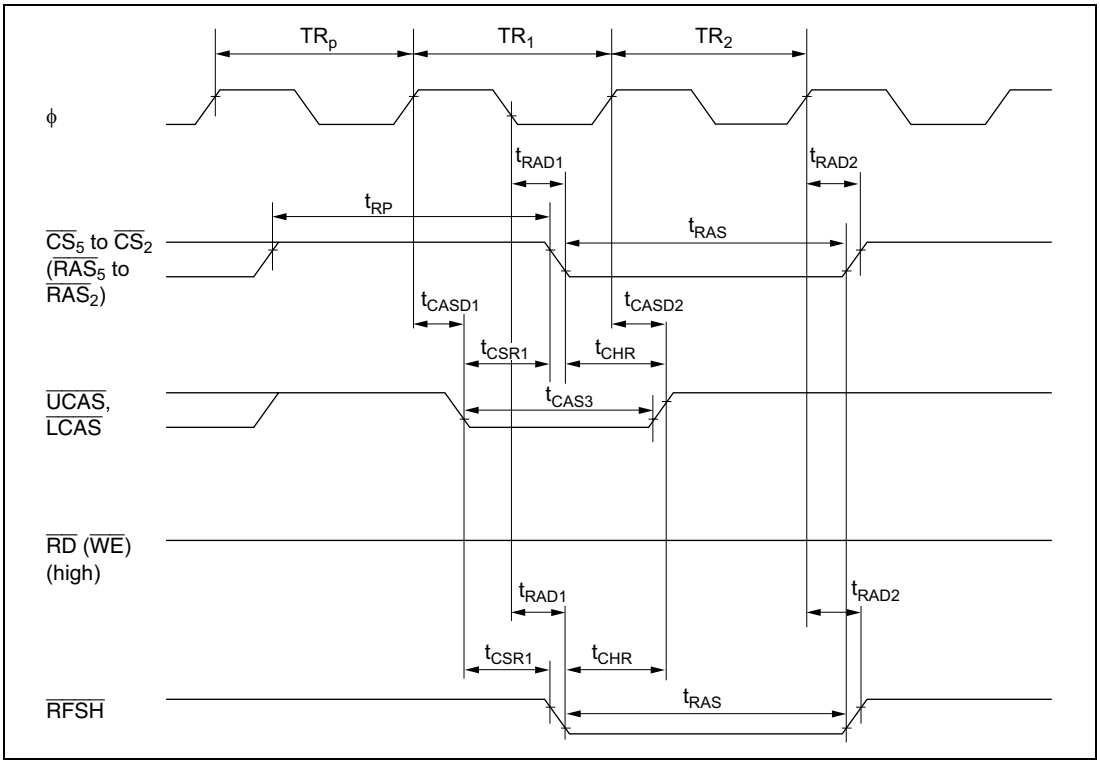


Figure 21.18 DRAM Bus Timing (CAS Before RAS Refresh)

Mnemonic	Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
		#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	|		I	H	N	Z	V	C	Normal	Advanced
BLD #xx:3, @ERd	B			4							(#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
BLD #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BILD #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BILD #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
BILD #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'EE0B0	Reserved area (access prohibited)										
H'EE0B1											
H'EE0B2											
H'EE0B3											
H'EE0B4											
H'EE0B5											
H'EE0B6											
H'EE0B7											
H'EE0B8											
H'EE0B9											
H'EE0BA											
H'EE0BB											
H'EE0BC											
H'EE0BD											
H'EE0BE											
H'EE0BF											
H'EE0C0											
H'EE0C1											
H'EE0C2											
H'EE0C3											
H'EE0C4											
H'EE0C5											
H'EE0C6											
H'EE0C7											
H'EE0C8											
H'EE0C9											
H'EE0CA											
H'EE0CB											
H'EE0CC											
H'EE0CD											
H'EE0CE											
H'EE0CF											

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFE30	—		—	—	—	—	—	—	—	—	
H'FFE31	—		—	—	—	—	—	—	—	—	
H'FFE32	—		—	—	—	—	—	—	—	—	
H'FFE33	—		—	—	—	—	—	—	—	—	
H'FFE34	—		—	—	—	—	—	—	—	—	
H'FFE35	—		—	—	—	—	—	—	—	—	
H'FFE36	—		—	—	—	—	—	—	—	—	
H'FFE37	—		—	—	—	—	—	—	—	—	
H'FFE38	—		—	—	—	—	—	—	—	—	
H'FFE39	—		—	—	—	—	—	—	—	—	
H'FFE3A	—		—	—	—	—	—	—	—	—	
H'FFE3B	—		—	—	—	—	—	—	—	—	
H'FFE3C	—		—	—	—	—	—	—	—	—	
H'FFE3D	—		—	—	—	—	—	—	—	—	
H'FFE3E	—		—	—	—	—	—	—	—	—	
H'FFE3F	—		—	—	—	—	—	—	—	—	
H'FFE40	—		—	—	—	—	—	—	—	—	
H'FFE41	—		—	—	—	—	—	—	—	—	
H'FFE42	—		—	—	—	—	—	—	—	—	
H'FFE43	—		—	—	—	—	—	—	—	—	
H'FFE44	—		—	—	—	—	—	—	—	—	
H'FFE45	—		—	—	—	—	—	—	—	—	
H'FFE46	—		—	—	—	—	—	—	—	—	
H'FFE47	—		—	—	—	—	—	—	—	—	
H'FFE48	—		—	—	—	—	—	—	—	—	
H'FFE49	—		—	—	—	—	—	—	—	—	
H'FFE4A	—		—	—	—	—	—	—	—	—	
H'FFE4B	—		—	—	—	—	—	—	—	—	
H'FFE4C	—		—	—	—	—	—	—	—	—	
H'FFE4D	—		—	—	—	—	—	—	—	—	
H'FFE4E	—		—	—	—	—	—	—	—	—	
H'FFE4F	—		—	—	—	—	—	—	—	—	

Bit	7	6	5	4	3	2	1	0
	IPRA7	IPRA6	IPRA5	IPRA4	IPRA3	IPRA2	IPRA1	IPRA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Priority level A7 to A0

0	Priority level 0 (low priority)
1	Priority level 1 (high priority)

- Interrupt sources controlled by each bit

	Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		IPRA7	IPRA6	IPRA5	IPRA4	IPRA3	IPRA2	IPRA1	IPRA0
IPRA	Interrupt source	IRQ_0	IRQ_1	IRQ_2, IRQ_3	IRQ_4, IRQ_5	WDT, DRAM interface, A/D converter	16-bit timer channel 0	16-bit timer channel 1	16-bit timer channel 2

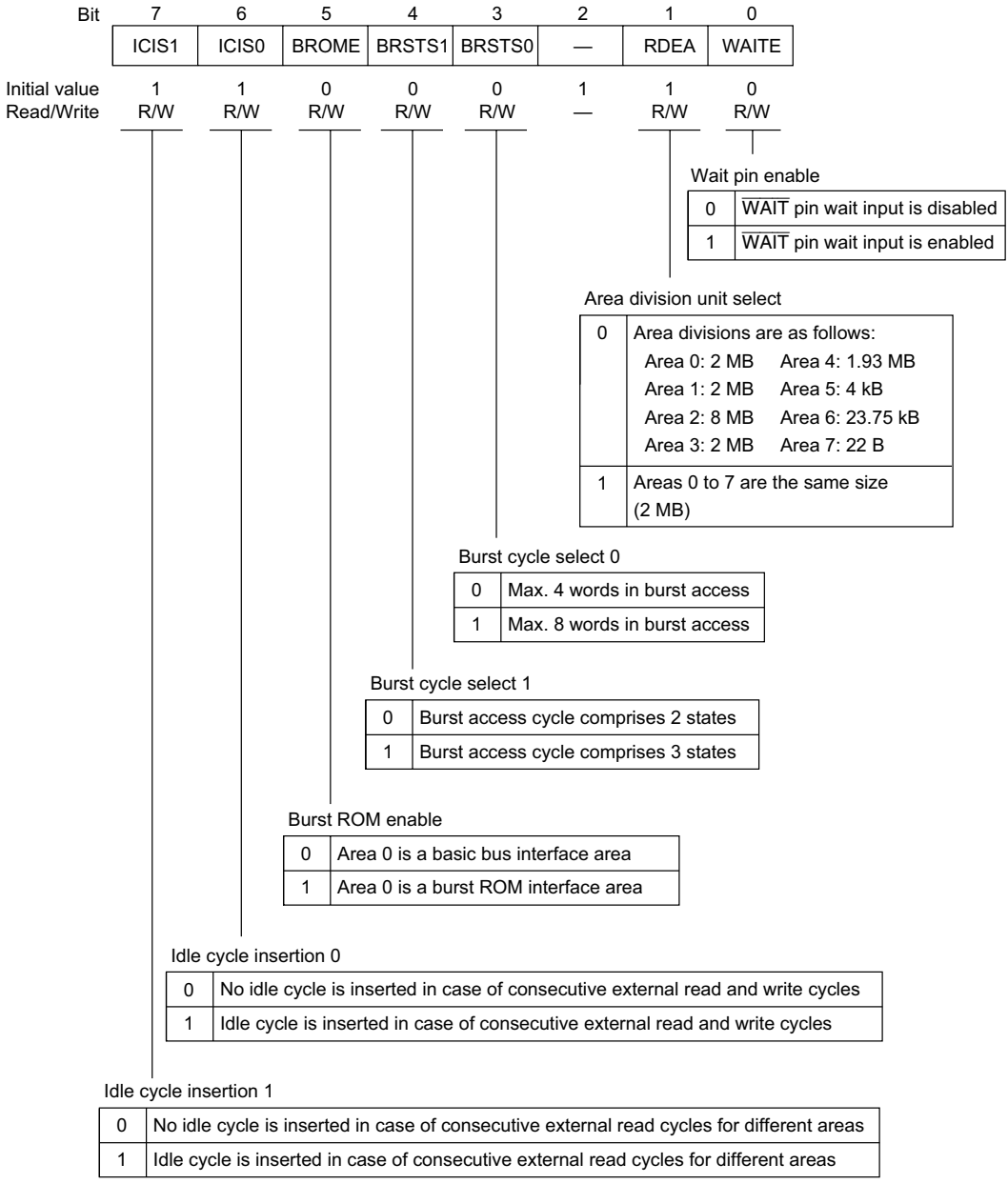
Bit	7	6	5	4	3	2	1	0
	IPRB7	IPRB6	IPRB5	—	IPRB3	IPRB2	IPRB1	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Priority level B7 to B5, B3 to B1

0	Priority level 0 (low priority)
1	Priority level 1 (high priority)

- Interrupt sources controlled by each bit

	Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		IPRB7	IPRB6	IPRB5	—	IPRB3	IPRB2	IPRB1	—
IPRB	Interrupt source	8-bit timer channels 0 and 1	8-bit timer channels 2 and 3	DMAC	—	SCI channel 0	SCI channel 1	SCI channel 2	—



Bit	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BROME	BRSTS1	BRSTS0	—	RDEA	WAITE
Initial value	1	1	0	0	0	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W

Wait pin enable

0	$\overline{\text{WAIT}}$ pin wait input is disabled
1	$\overline{\text{WAIT}}$ pin wait input is enabled

Area division unit select

0	Area divisions are as follows: Area 0: 2 MB Area 4: 1.93 MB Area 1: 2 MB Area 5: 4 kB Area 2: 8 MB Area 6: 23.75 kB Area 3: 2 MB Area 7: 22 B
1	Areas 0 to 7 are the same size (2 MB)

Burst cycle select 0

0	Max. 4 words in burst access
1	Max. 8 words in burst access

Burst cycle select 1

0	Burst access cycle comprises 2 states
1	Burst access cycle comprises 3 states

Burst ROM enable

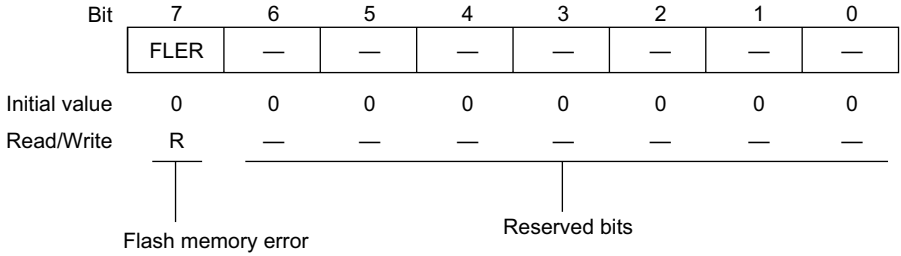
0	Area 0 is a basic bus interface area
1	Area 0 is a burst ROM interface area

Idle cycle insertion 0

0	No idle cycle is inserted in case of consecutive external read and write cycles
1	Idle cycle is inserted in case of consecutive external read and write cycles

Idle cycle insertion 1

0	No idle cycle is inserted in case of consecutive external read cycles for different areas
1	Idle cycle is inserted in case of consecutive external read cycles for different areas



Notes: 1. Writes to FLMCR2 are prohibited.
2. This register is used only by the flash memory version and do not exist in the mask ROM version. In the mask ROM version reading these addresses always returns a value of 1, and it is not possible to write to them.

EBR (EBR1)—Erase Block Register H'EE032 Flash Memory

Bit		7	6	5	4	3	2	1	0
		EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Modes 1 to 4, and 6	Initial value	0	0	0	0	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R
Modes 5 and 7	Initial value	0	0	0	0	0	0	0	0
	Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Block 7 to 0

0	Block EB7 to EB0 is not selected (Initial value)
1	Block EB7 to EB0 is selected

Notes: 1. When not erasing, clear EBR to H'00.
Writes are invalid.
A value of 1 cannot be set in this register in mode 6.
2. This register is used only by the flash memory version and do not exist in the mask ROM version. In the mask ROM version reading these addresses always returns a value of 1, and it is not possible to write to them.