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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16c4-an

7. Memories

7.1 Features

- Flash program memory
 - One linear address space
 - In-system programmable
 - Self-programming and boot loader support
 - Application section for application code
 - Application table section for application code or data storage
 - Boot section for application code or boot loader code
 - Separate read/write protection lock bits for all sections
 - Built in fast CRC check of a selectable flash program memory section
- Data memory
 - One linear address space
 - Single-cycle access from CPU
 - SRAM
 - EEPROM
 - Byte and page accessible
 - Optional memory mapping for direct load and store
 - I/O memory
 - Configuration and status registers for all peripherals and modules
 - Four bit-accessible general purpose registers for global variables or flags
 - Separate buses for SRAM, EEPROM and I/O memory
 - Simultaneous bus access for CPU
- Production signature row memory for factory programmed data
 - ID for each microcontroller device type
 - Serial number for each device
 - Calibration bytes for factory calibrated peripherals
- User signature row
 - One flash page in size
 - Can be read and written from software
 - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering Information” on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but

9. System Clock and Clock Options

9.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
 - 32MHz run-time calibrated and tuneable oscillator
 - 2MHz run-time calibrated oscillator
 - 32.768kHz calibrated oscillator
 - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
 - 0.4MHz - 16MHz crystal oscillator
 - 32.768kHz crystal oscillator
 - External clock
- PLL with 20MHz - 128MHz output frequency
 - Internal and external clock options and 1x to 31x multiplication
 - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

9.2 Overview

Atmel AVR XMEGA C4 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 9-1 on page 20 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 22.

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes:
 - Idle
 - Power down
 - Power save
 - Standby
 - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

12. WDT – Watchdog Timer

12.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
 - Normal mode
 - Window mode
- Configuration lock to prevent unwanted changes

12.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
 - 32.768kHz external crystal
 - External clock
 - 32.768kHz internal oscillator
 - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

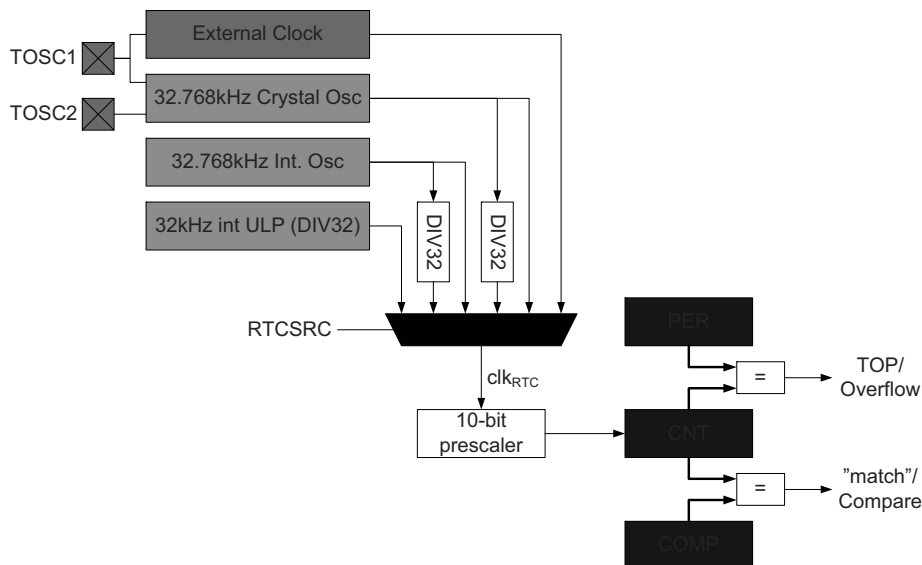
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5 μ s, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than 18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview



Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

21. TWI – Two-Wire Interface

21.1 Features

- Two Identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
 - Phillips I²C compatible
 - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
 - Slave operation
 - Single bus master operation
 - Bus master in multi-master bus environment
 - Multi-master arbitration
- Flexible slave address match functions
 - 7-bit and general call address recognition in hardware
 - 10-bit addressing supported
 - Address mask register for dual address match or address range masking
 - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

21.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I²C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V_{CC} voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

29. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

29.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

29.1.1 Operation/Power Supply

V _{CC}	Digital supply voltage
AV _{CC}	Analog supply voltage
GND	Ground

29.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYN	Port pin with full synchronous and full asynchronous interrupt function

29.1.3 Analog Functions

AC _n	Analog Comparator input pin n
AC _n OUT	Analog Comparator n output
ADC _n	Analog to Digital Converter input pin n
A _{REF}	Analog Reference input pin

29.1.4 Timer/Counter and AWEX Functions

OC _n LS	Output Compare Channel x Low Side for Timer/Counter n
OC _n HS	Output Compare Channel x High Side for Timer/Counter n

29.1.5 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
XCK _n	Transfer Clock for USART n
RXD _n	Receiver Data for USART n
TXD _n	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI

Table 33-11. Gain Stage Characteristics

R_{in}	Input resistance	Switched in normal mode		4.0		k Ω
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		$AV_{CC} - 0.6$	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk _{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain Error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		10		
	Offset Error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-150		

33.1.7 Analog Comparator Characteristics

Table 33-12. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage	$V_{CC}=1.6V - 3.6V$		$\leq \pm 10$		mV
I_{lk}	Input leakage current	$V_{CC}=1.6V - 3.6V$		< 1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		μs
V_{hys1}	Hysteresis, none	$V_{CC}=1.6V - 3.6V$		0		mV
V_{hys2}	Hysteresis, small	$V_{CC}=1.6V - 3.6V$		11		
V_{hys3}	Hysteresis, large	$V_{CC}=1.6V - 3.6V$		26		
t_{delay}	Propagation delay	$V_{CC} = 3.0V, T = 85^{\circ}C$		16	90	ns
		$V_{CC}=1.6V - 3.6V$		16		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

33.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.2.13.6 External Clock Characteristics

Figure 33-10. External Clock Drive Waveform

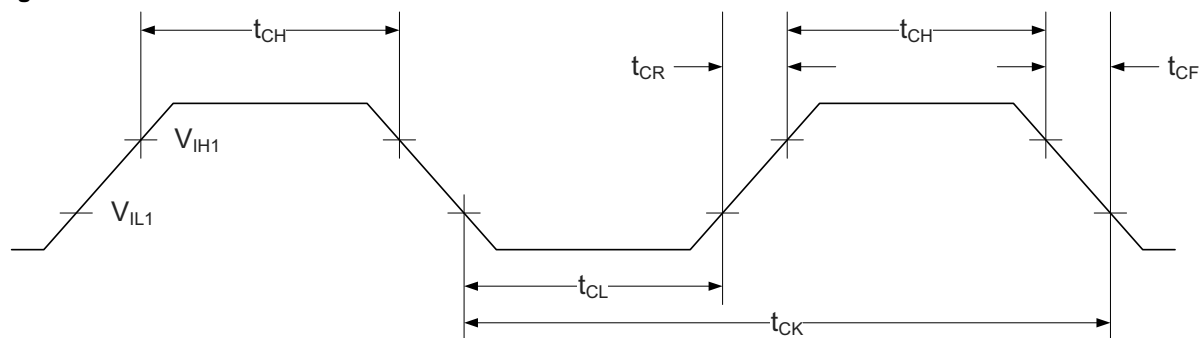


Table 33-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock high time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock low time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.2.14 SPI Characteristics

Figure 33-12. SPI Timing Requirements in Master Mode

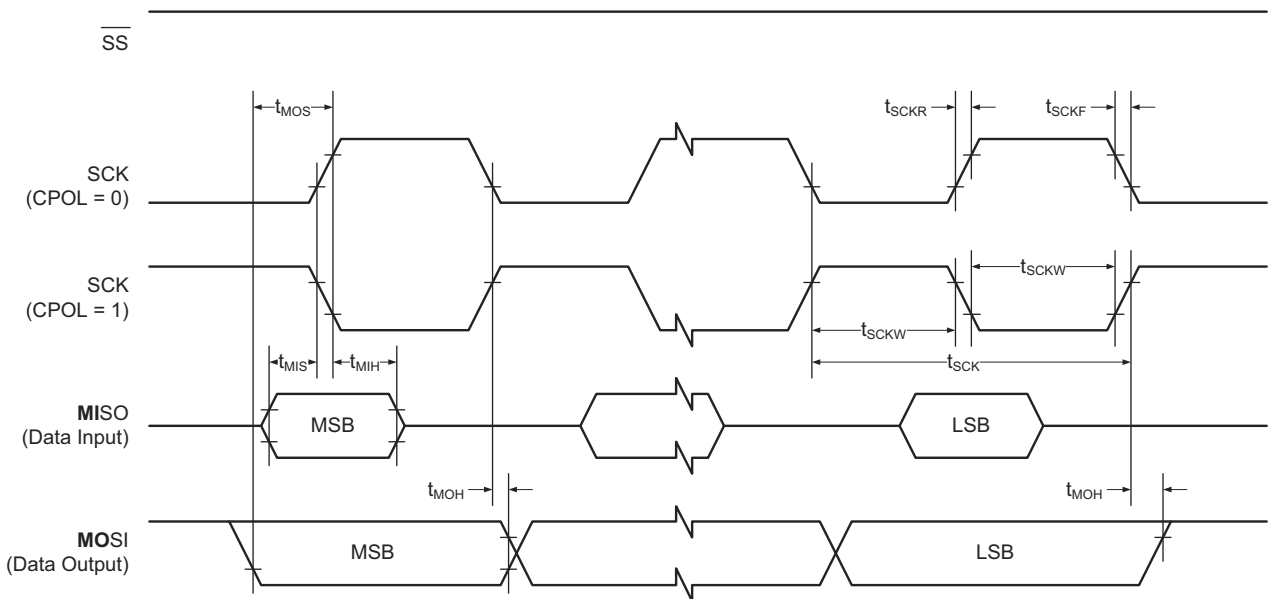


Figure 33-13. SPI Timing Requirements in Slave Mode

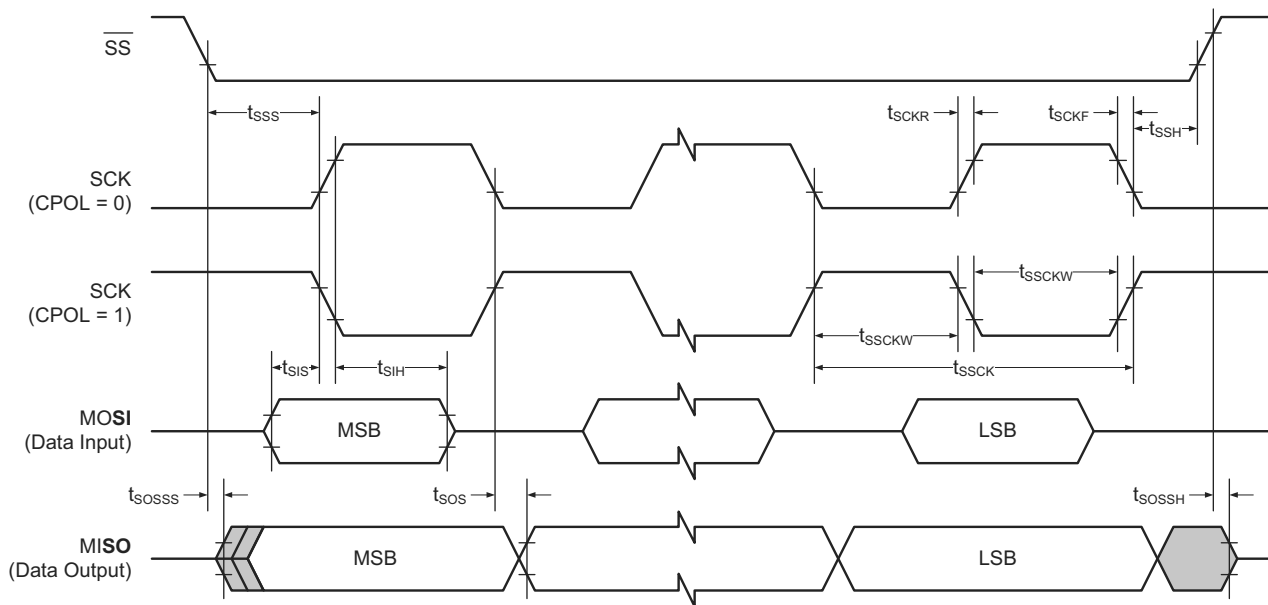


Figure 34-11. Idle Mode Supply Current vs. V_{CC}

$f_{SYS} = \text{MHz external clock}$

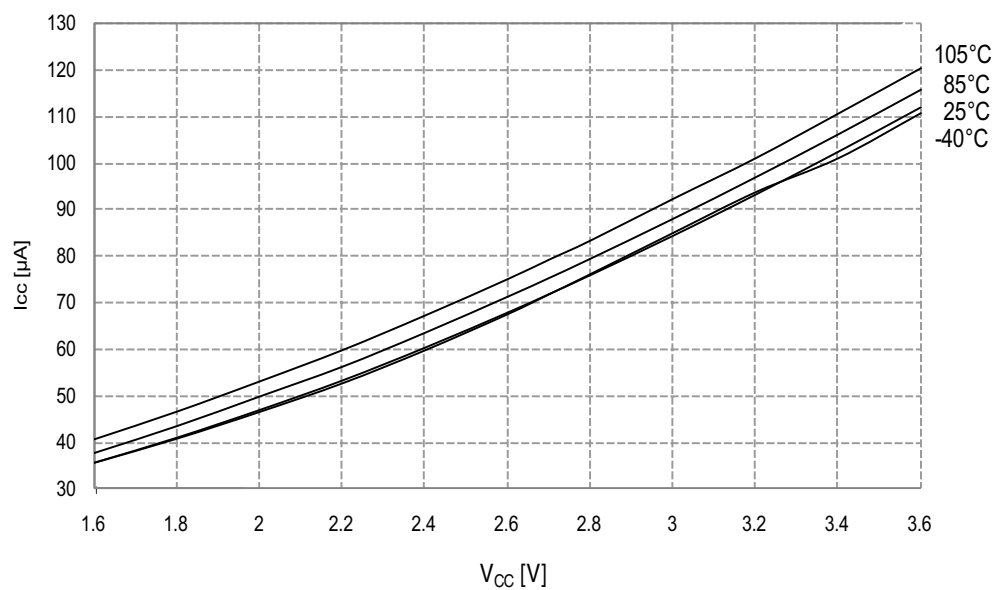
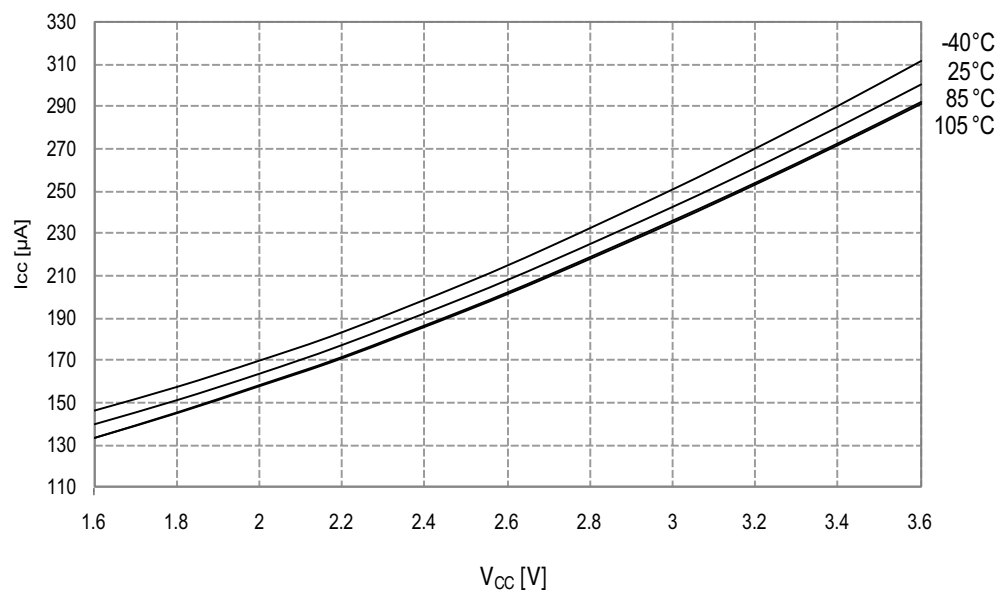


Figure 34-12. Idle Mode Supply Current vs. V_{CC}

$f_{SYS} = 2\text{MHz internal oscillator}$



34.1.6 BOD Characteristics

Figure 34-55. BOD Thresholds vs. Temperature
BOD level = 1.6V

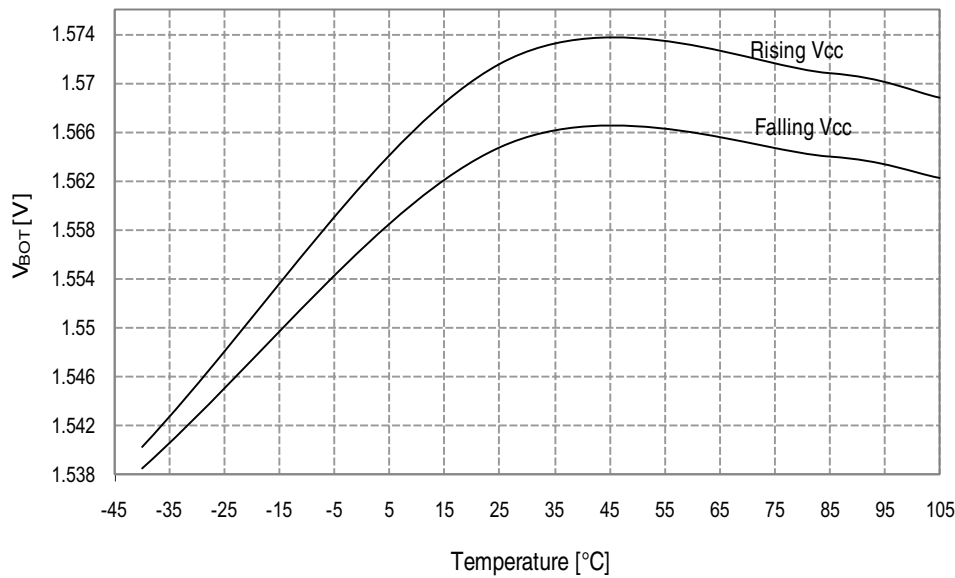


Figure 34-56. BOD Thresholds vs. Temperature
BOD level = 3.0V

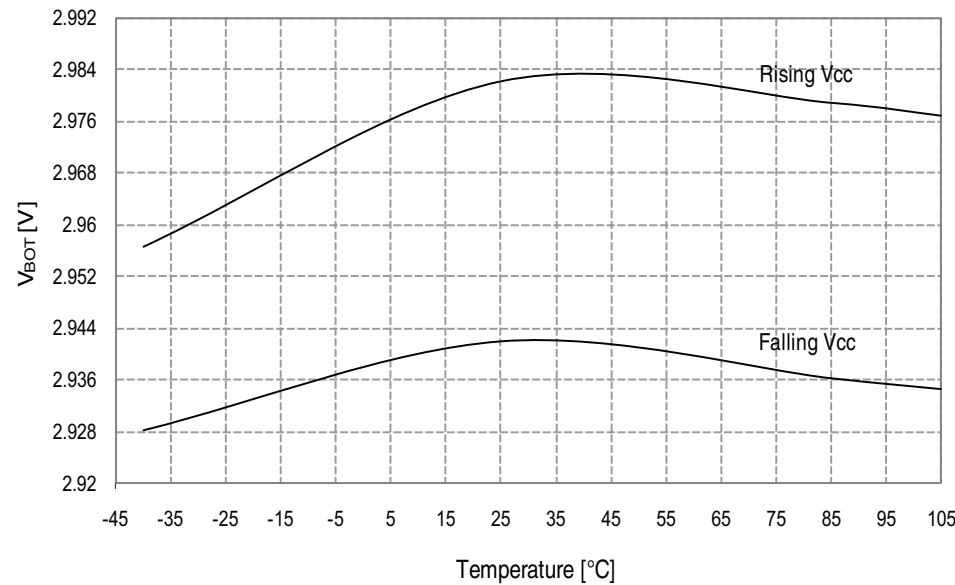


Figure 34-88. Idle Mode Supply Current vs. Frequency

$f_{SYS} = 1 - 32\text{MHz}$ external clock, $T = 25^\circ\text{C}$

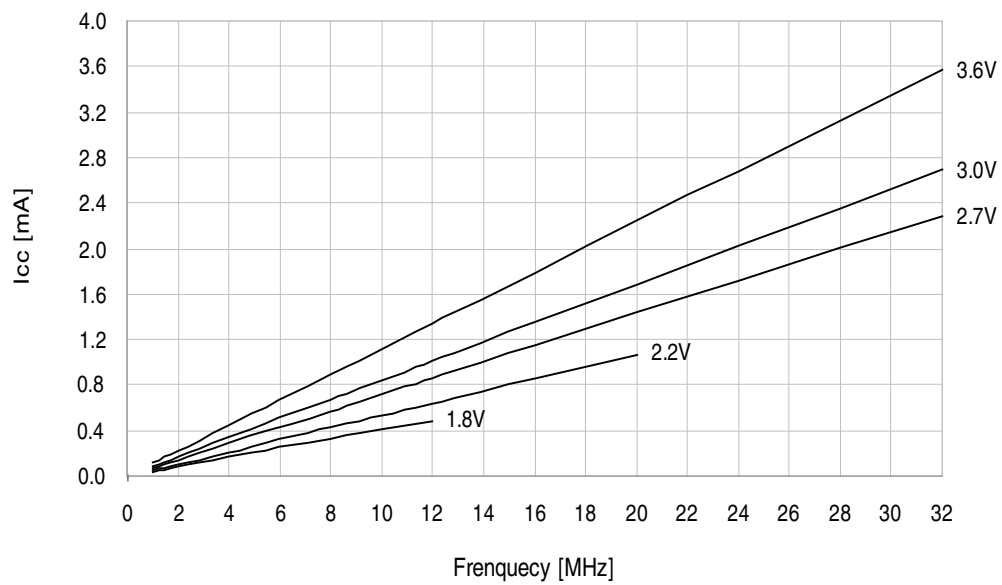


Figure 34-89. Idle Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator

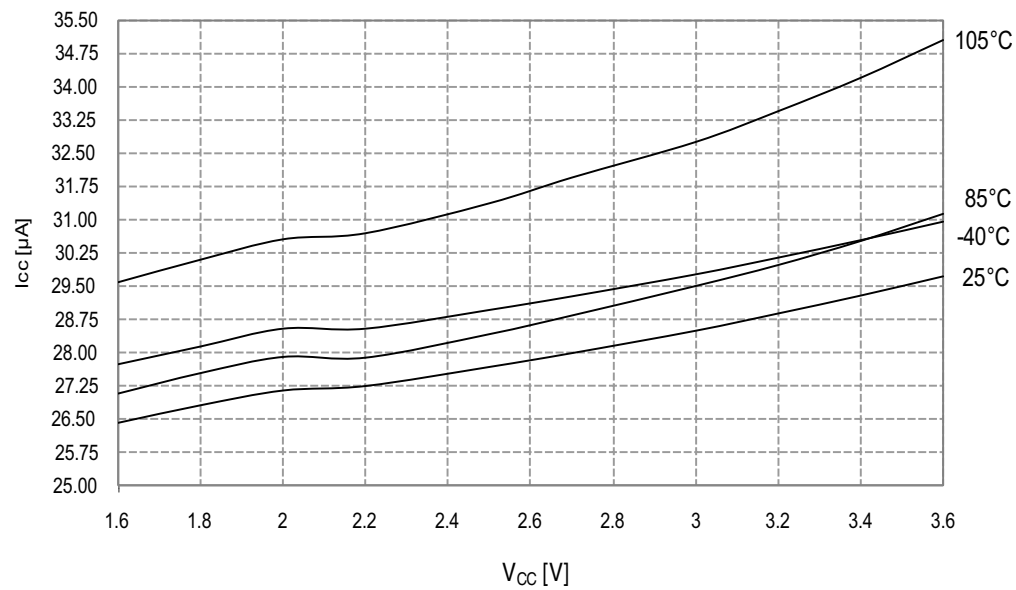


Figure 34-130. Analog Comparator Current Source vs. Calibration Value

$T = 25^{\circ}\text{C}$

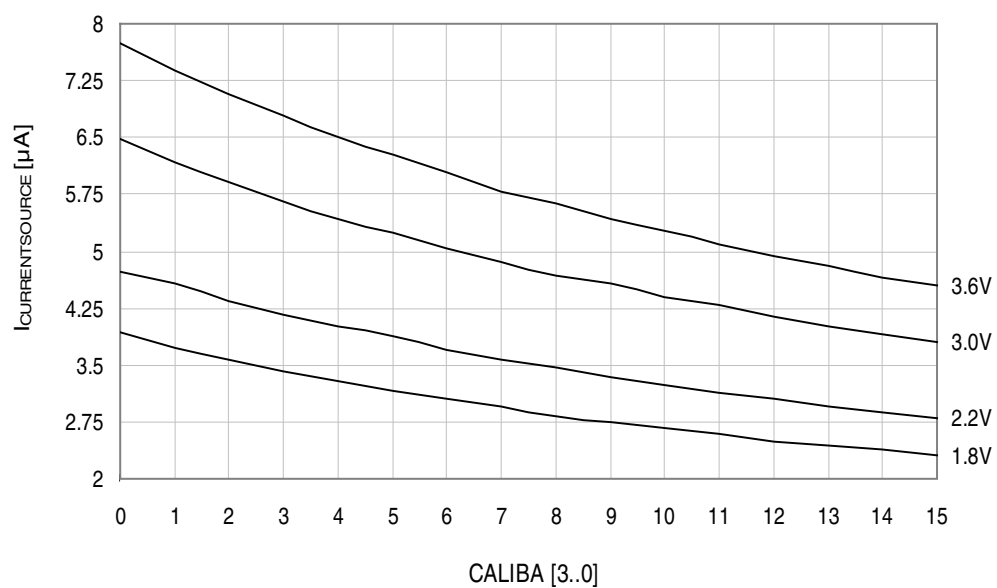
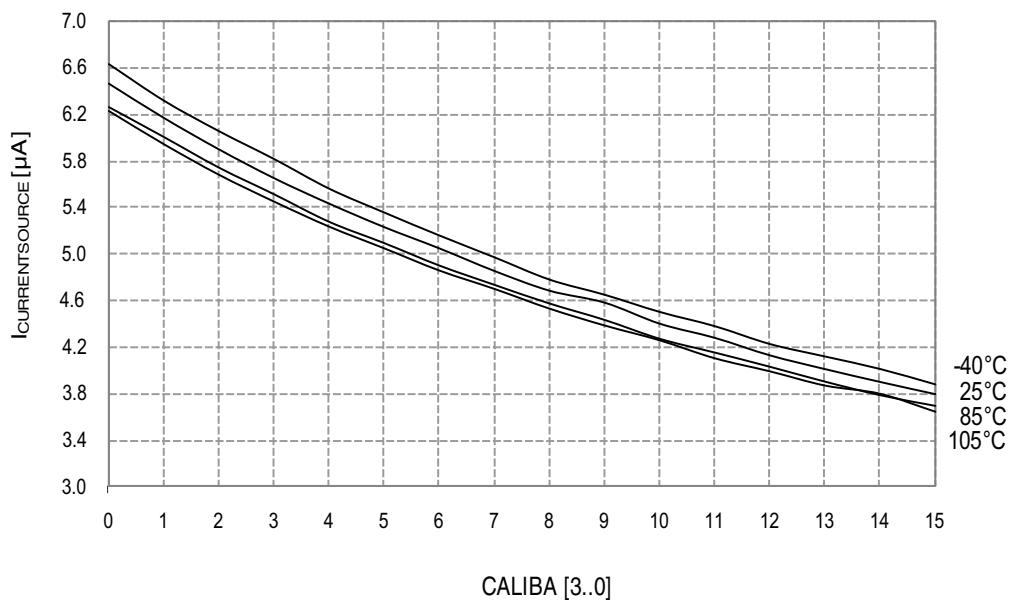


Figure 34-131. Analog Comparator Current Source vs. Calibration Value

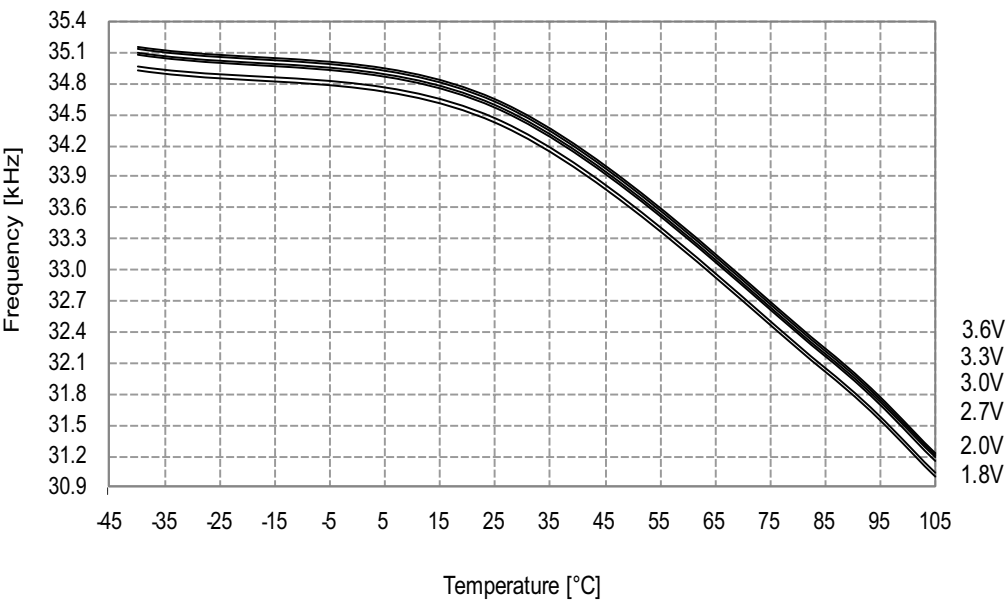
$V_{\text{CC}} = 3.0\text{V}$



34.2.9 Oscillator Characteristics

34.2.9.1 Ultra Low-Power Internal Oscillator

Figure 34-144. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.2.9.2 32.768kHz Internal Oscillator

Figure 34-145. 32.768kHz Internal Oscillator Frequency vs. Temperature

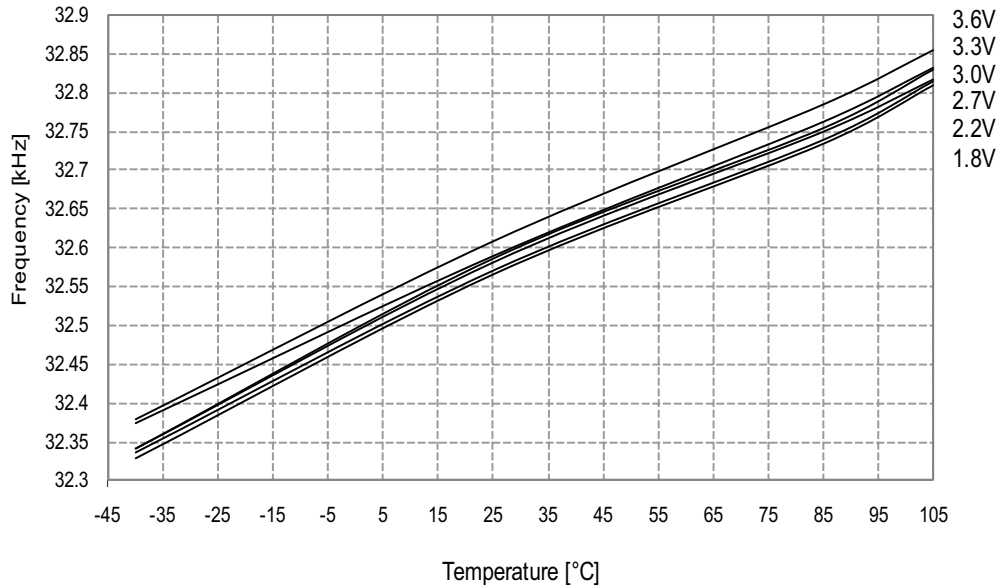
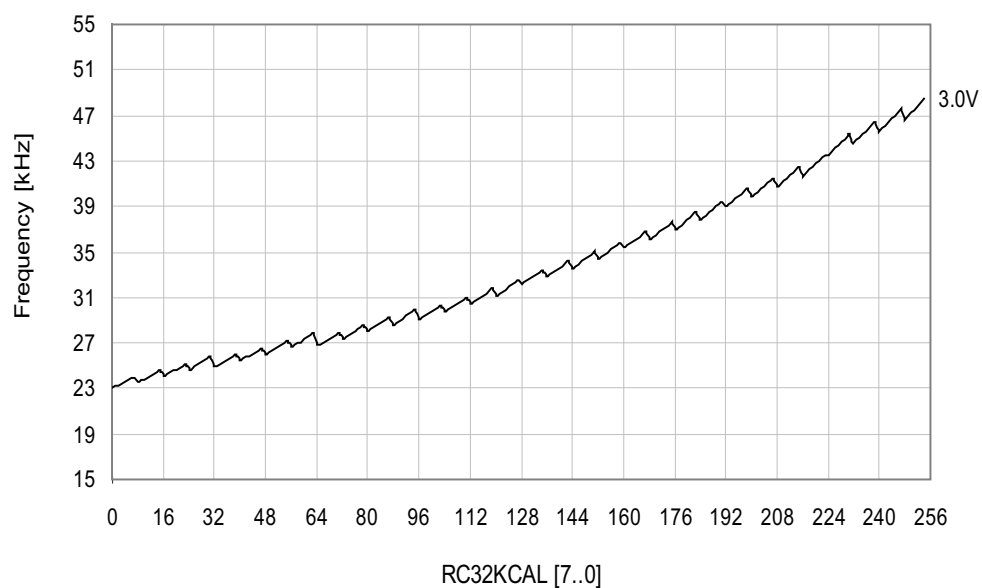


Figure 34-146. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

$V_{CC} = 3.0V$, $T = 25^{\circ}C$



34.2.9.3 2MHz Internal Oscillator

Figure 34-147. 2MHz Internal Oscillator Frequency vs. Temperature

DPLL disabled

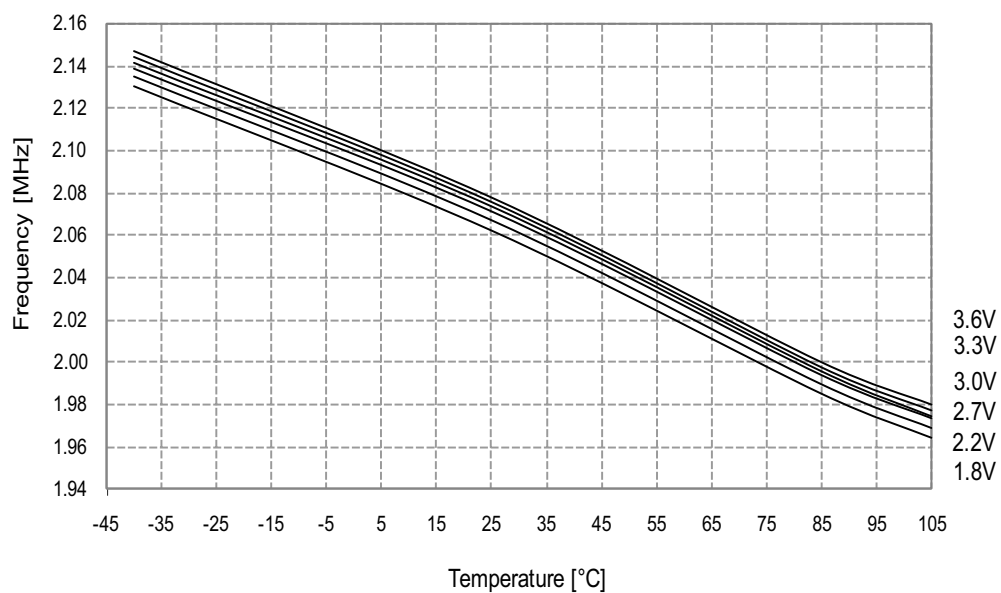


Figure 34-148. 2MHz Internal Oscillator Frequency vs. Temperature
DFLL enabled, from the 32.768kHz internal oscillator

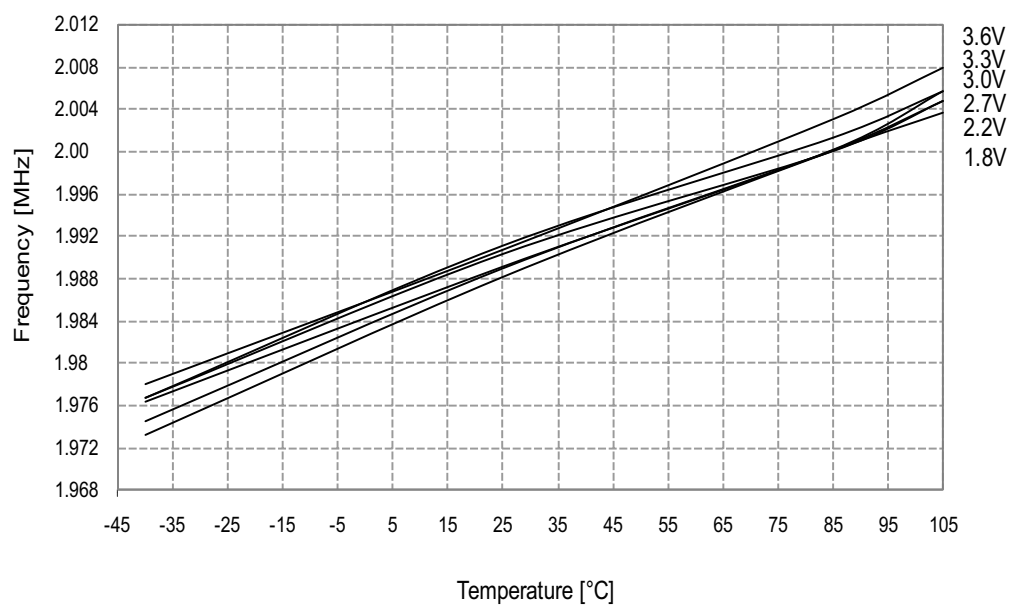


Figure 34-149. 2MHz Internal Oscillator CALA Calibration Step Size
 $V_{CC} = 3V$

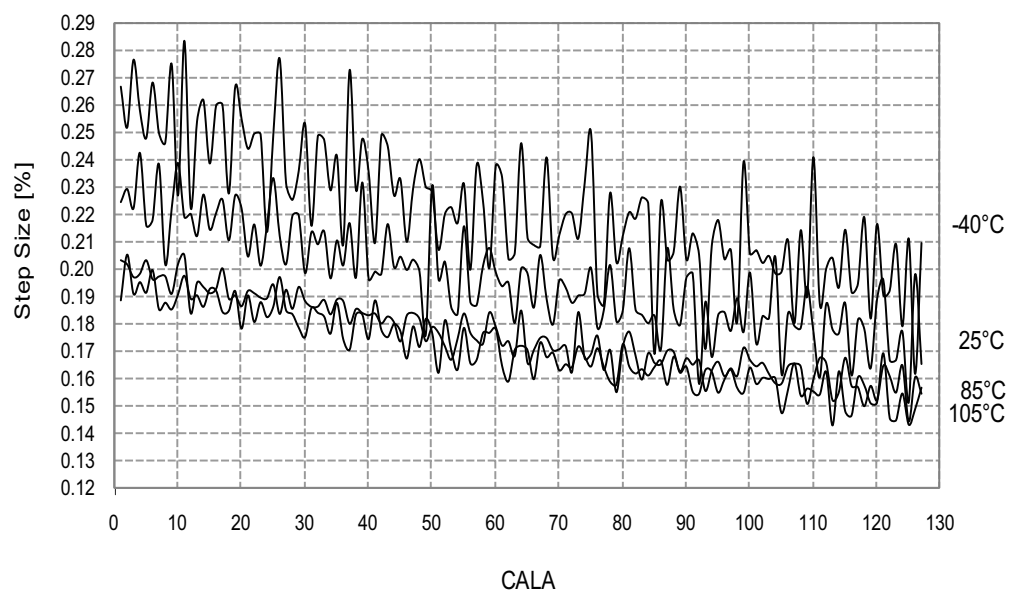
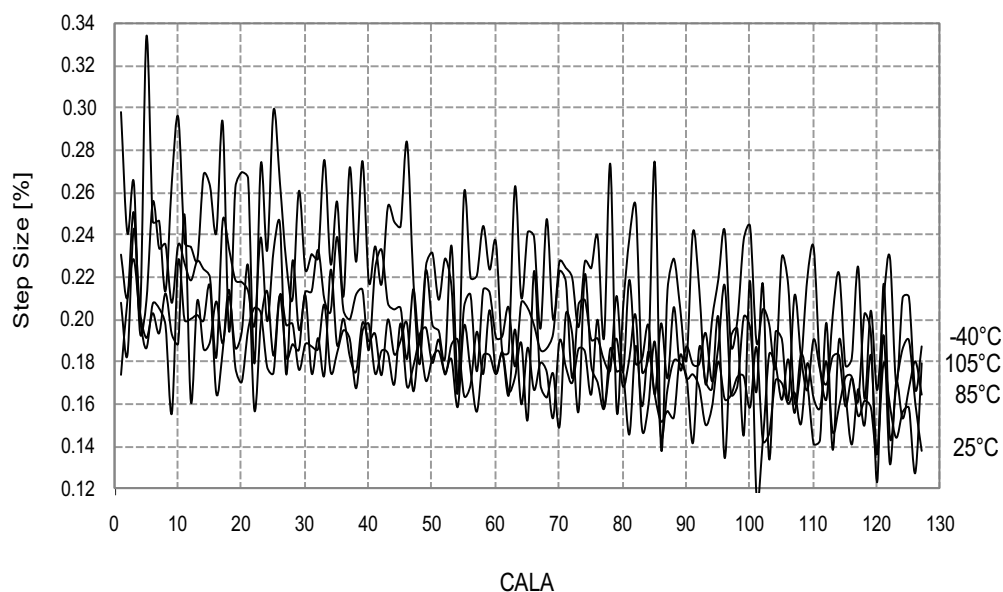


Figure 34-152. 32MHz Internal Oscillator CALA Calibration Step Size

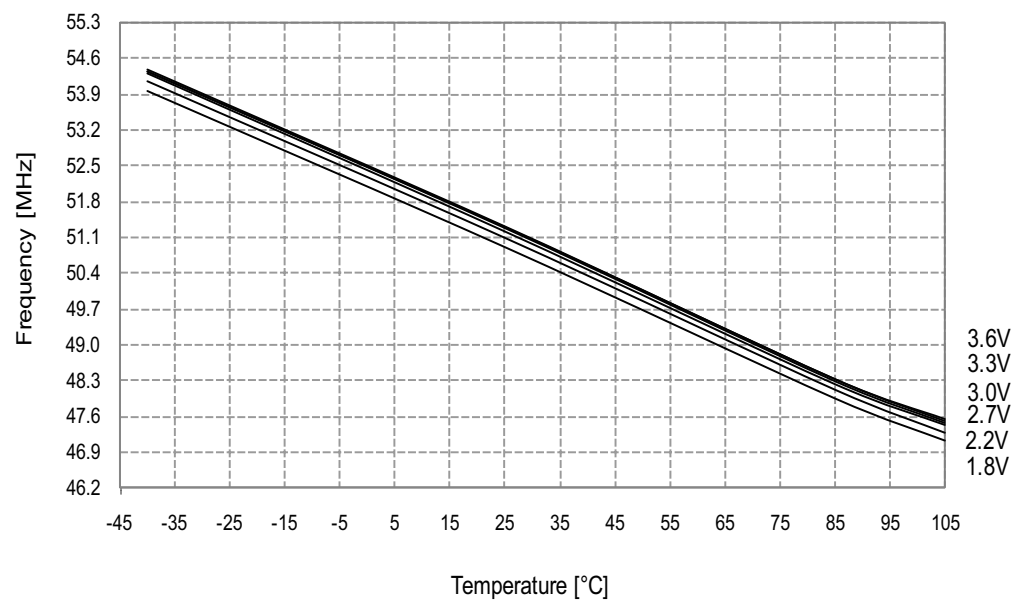
$V_{CC} = 3.0V$

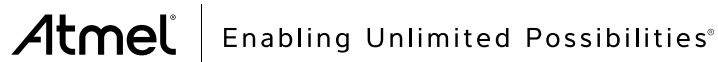


34.2.9.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-153. 48MHz Internal Oscillator Frequency vs. Temperature

DPLL disabled





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