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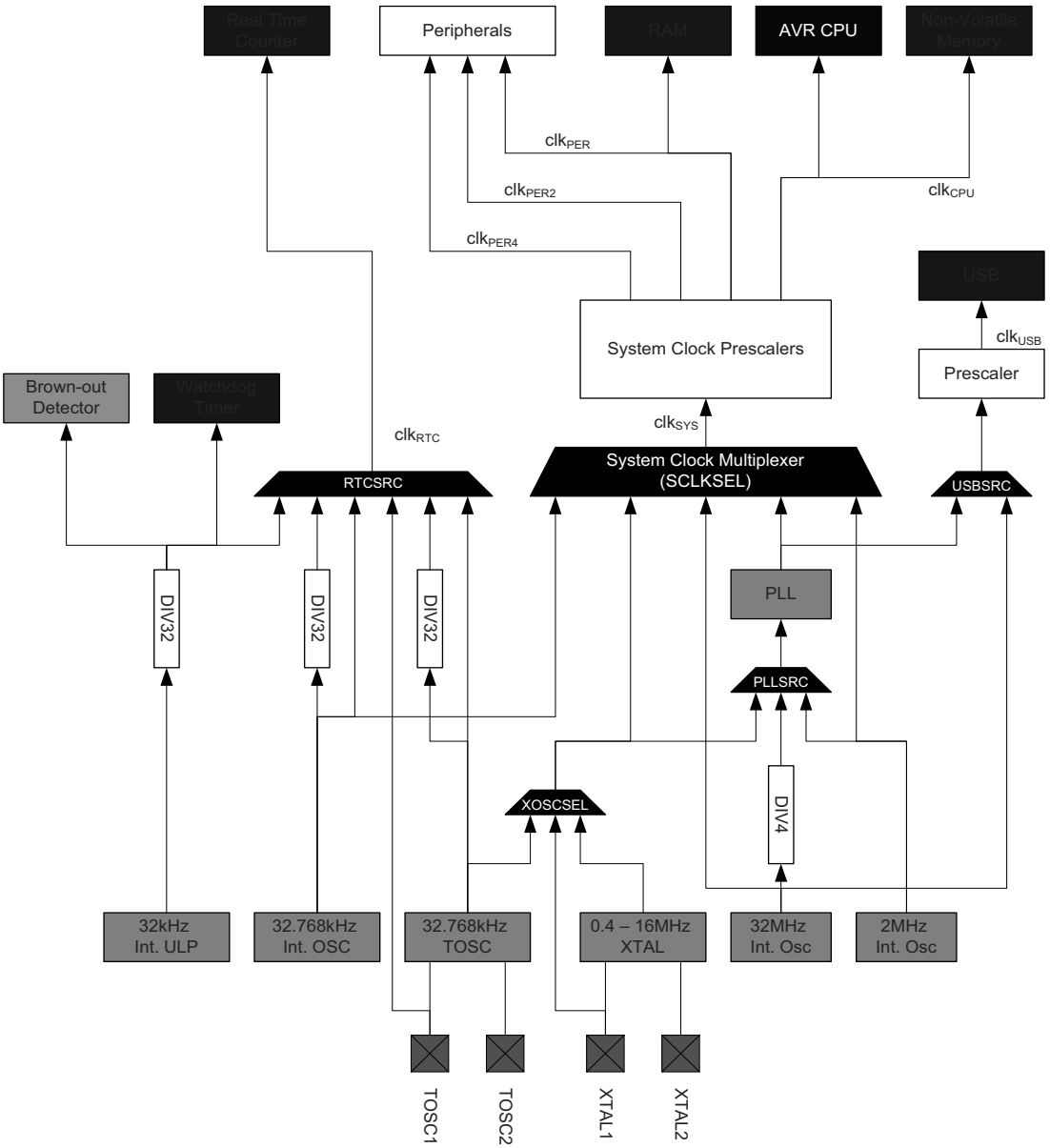
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16c4-aur

Figure 9-1. The Clock System, Clock Sources, and Clock Distribution



9.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources (DFLLs and PLL) are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

9.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes:
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

22. SPI – Serial Peripheral Interface

22.1 Features

- Two Identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

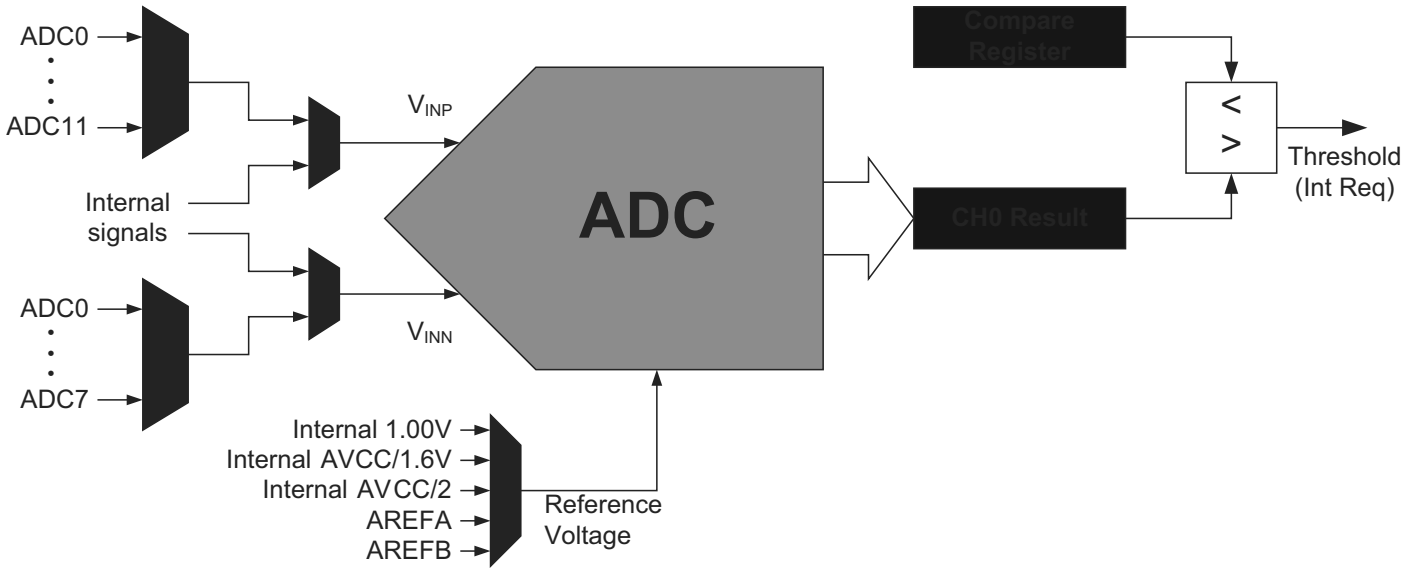
22.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

Figure 26-1. ADC Overview

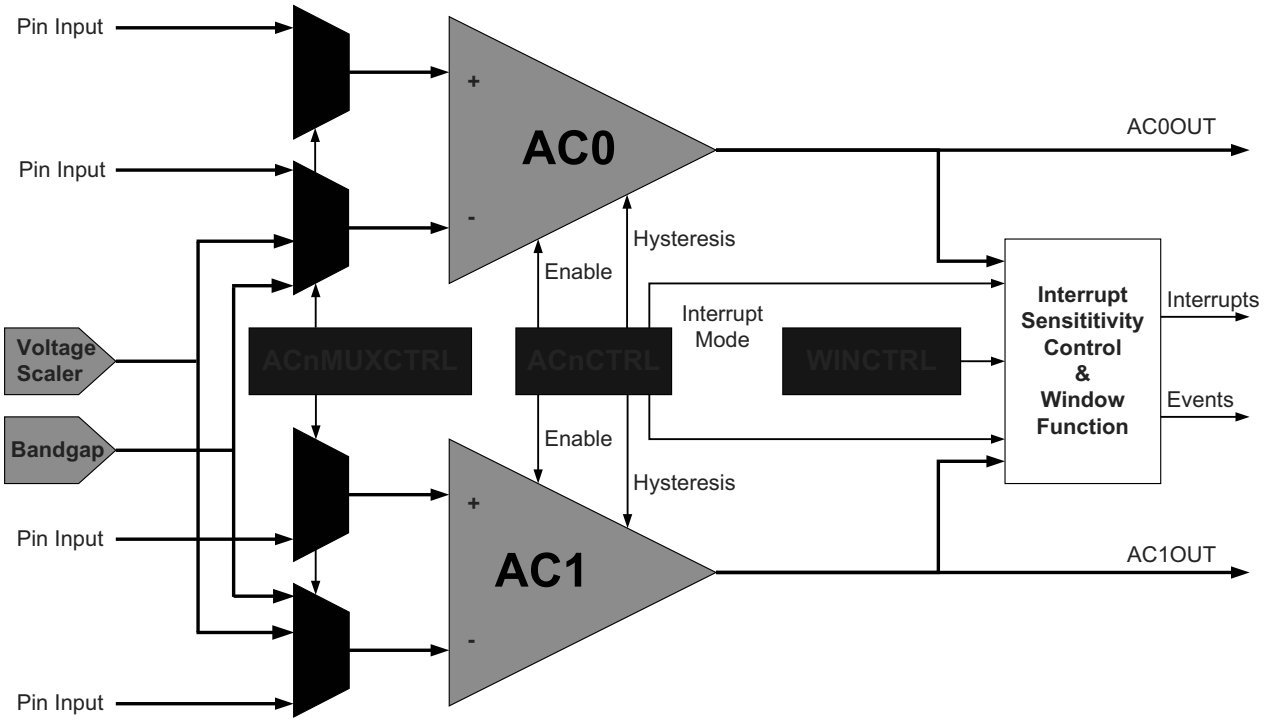


The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.35µs for 12-bit to 2.3µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

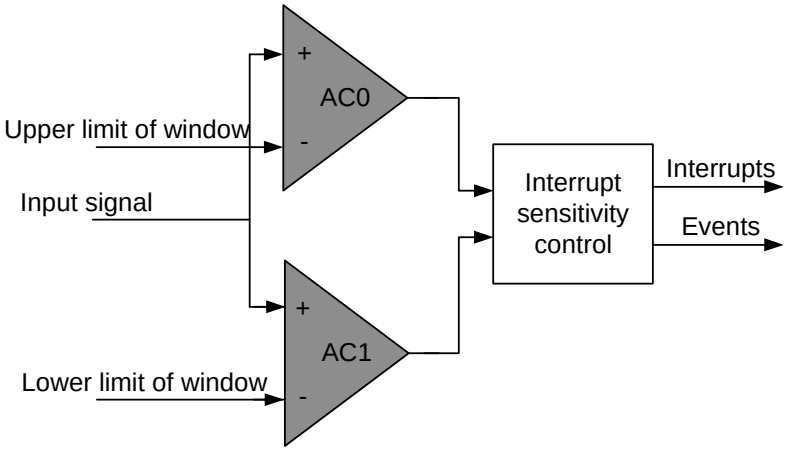
PORTA has one ADC. Notation of this peripheral is ADCA.

Figure 27-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog Comparator Window Function



30. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA C4. For complete register description and summary for each peripheral module, refer to the XMEGA C manual.

Table 30-1. Peripheral Module Address Map

Base address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock control
0x0048	SLEEP	Sleep controller
0x0050	OSC	Oscillator control
0x0060	DFLLRC32M	DFLL for the 32 MHz internal RC oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC oscillator
0x0070	PR	Power reduction
0x0078	RST	Reset controller
0x0080	WDT	Watch-dog timer
0x0090	MCU	MCU control
0x00A0	PMIC	Programmable multilevel interrupt controller
0x00B0	PORTCFG	Port configuration
0x0180	EVSYS	Event system
0x00D0	CRC	CRC module
0x01C0	NVM	Nonvolatile memory (NVM) controller
0x0200	ADCA	Analog to digital converter on port A
0x0380	ACA	Analog comparator pair on port A
0x0400	RTC	Real time counter
0x0480	TWIC	Two wire interface on port C
0x04C0	USB	Universal serial Bus interface
0x04A0	TWIE	Two wire interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing internal SRAM.

32.2 PW

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Notes :

02/17/2012

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat	ZCP	PW	H

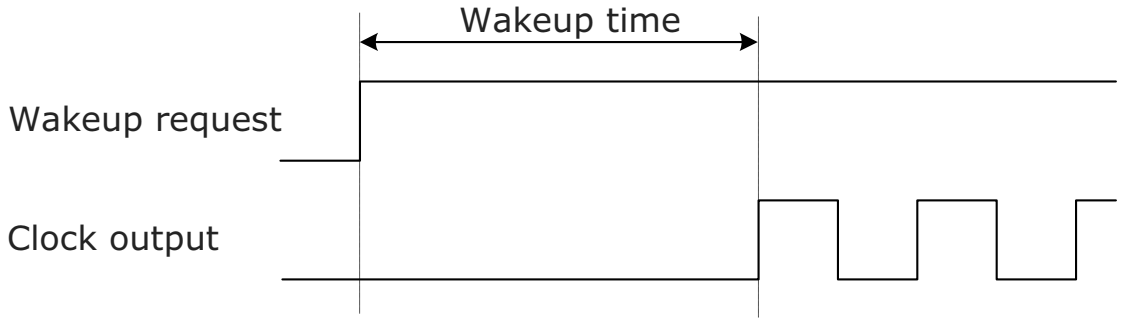
33.1.4 Wake-up Time from Sleep Fodes

Table 33-6. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		5.0		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-2. Wake-up Time Definition



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, C_L=20pF		67k		
			2MHz crystal, C_L=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, C_L=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, C_L=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, C_L=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, C_L=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
R_Q	Negative impedance	XOSCPWR=1, FRQRANGE=1, C_L=20pF	9MHz crystal		1500		Ω
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, C_L=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, C_L=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, C_L=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, C_L=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, C_L=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, C_L=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, C_L=20pF		1.4		

Table 33-58. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05*V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

34.1.1.3 Power-down Mode Supply Current

Figure 34-15.Power-down Mode Supply Current vs. V_{CC}

All functions disabled

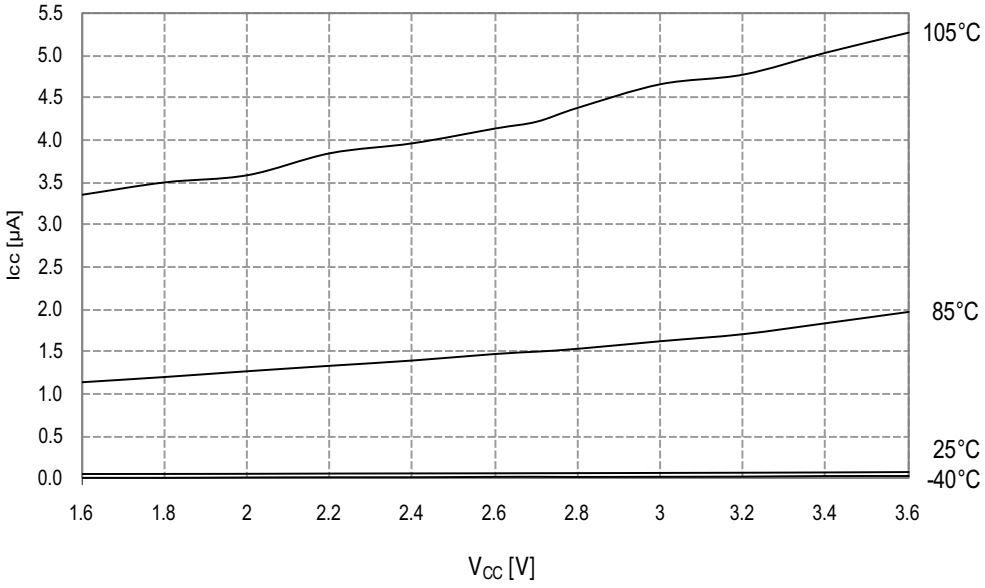


Figure 34-16.Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

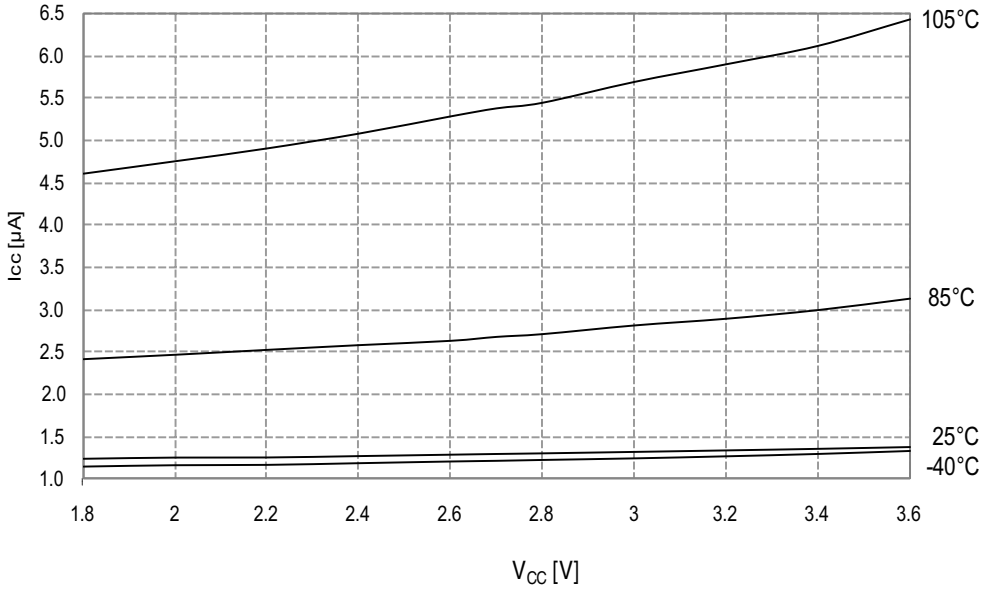


Figure 34-25. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

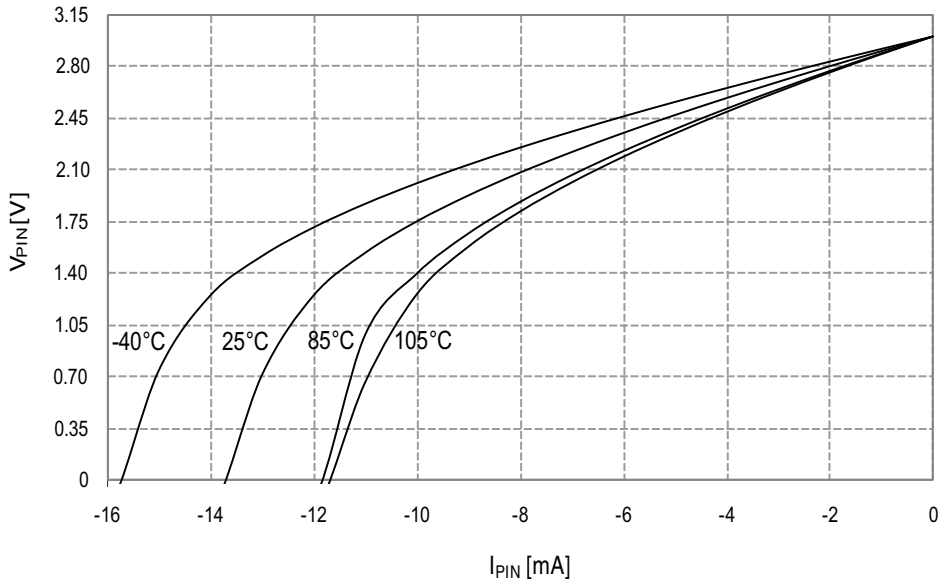


Figure 34-26. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

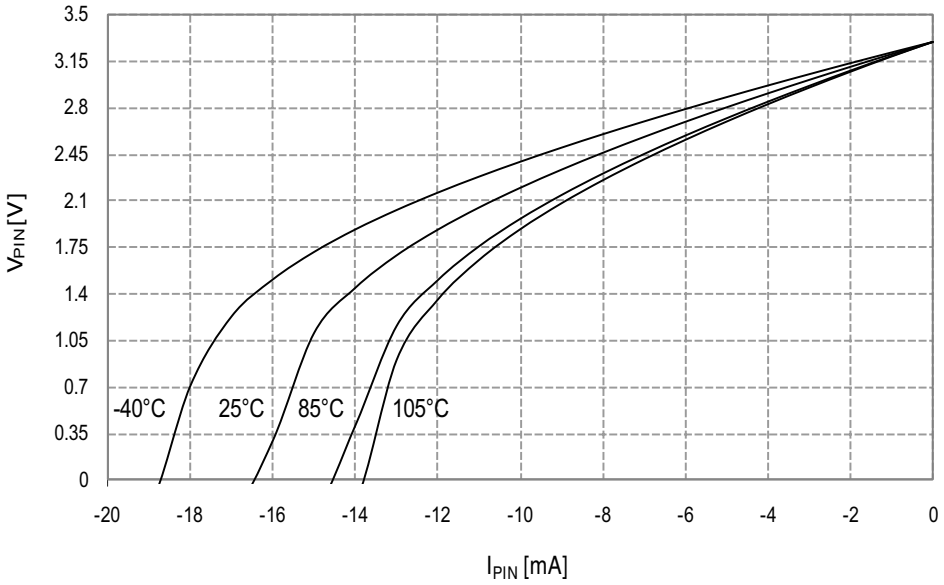


Figure 34-33. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

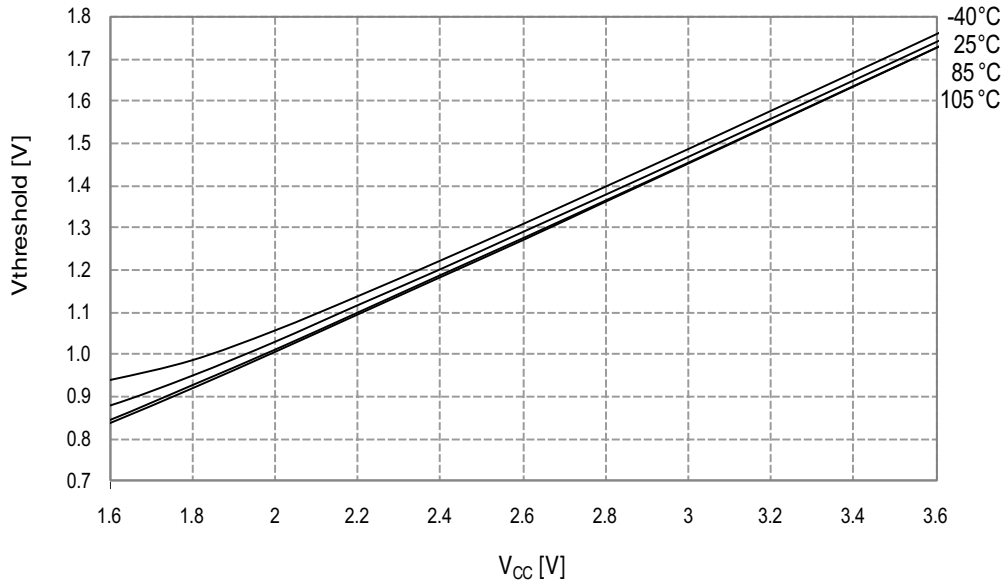
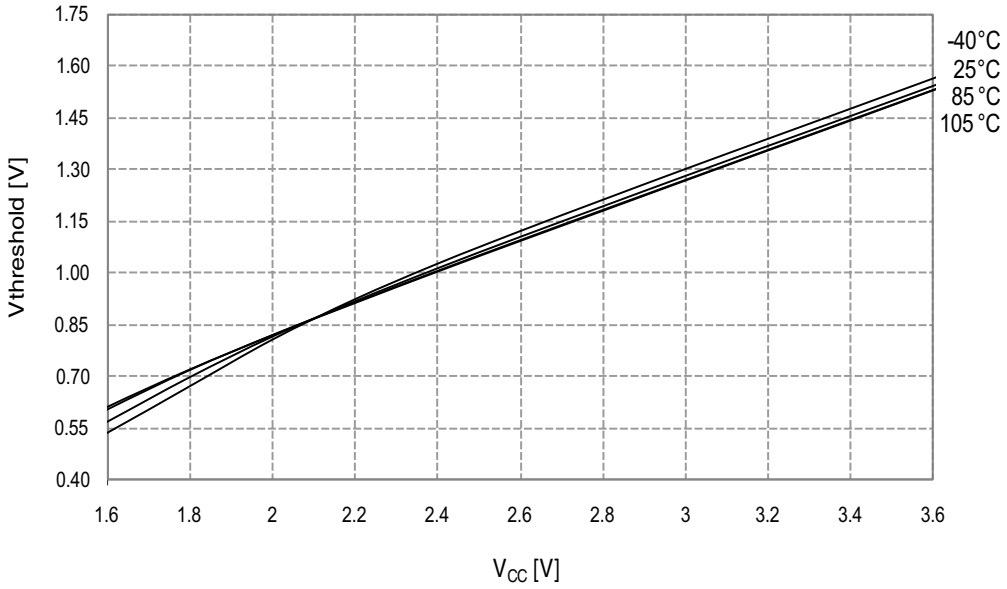


Figure 34-34. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"



34.1.7 External Reset Characteristics

Figure 34-57. Minimum Reset Pin Pulse Width vs. V_{CC}

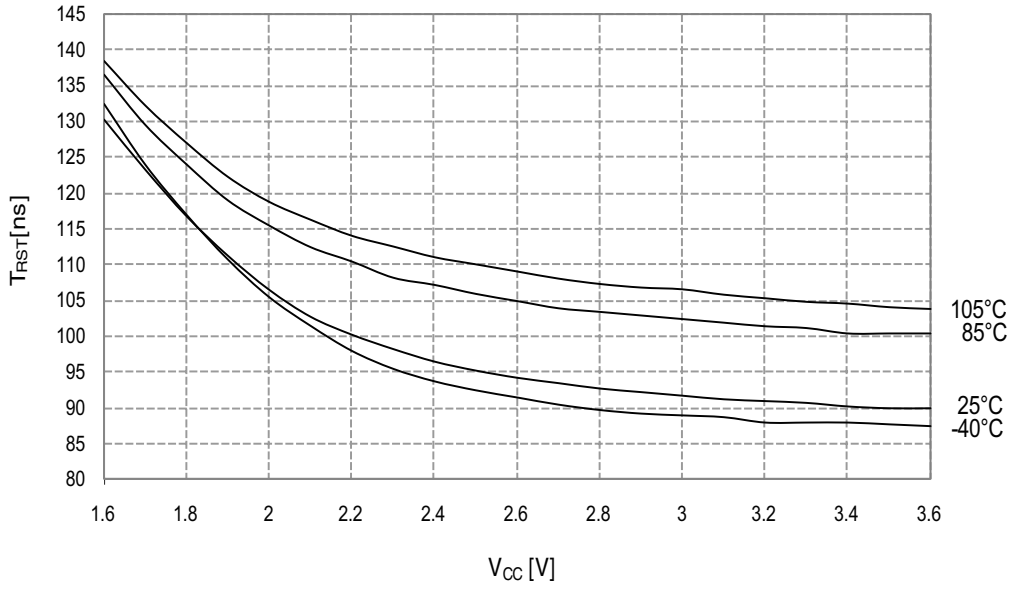


Figure 34-58. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

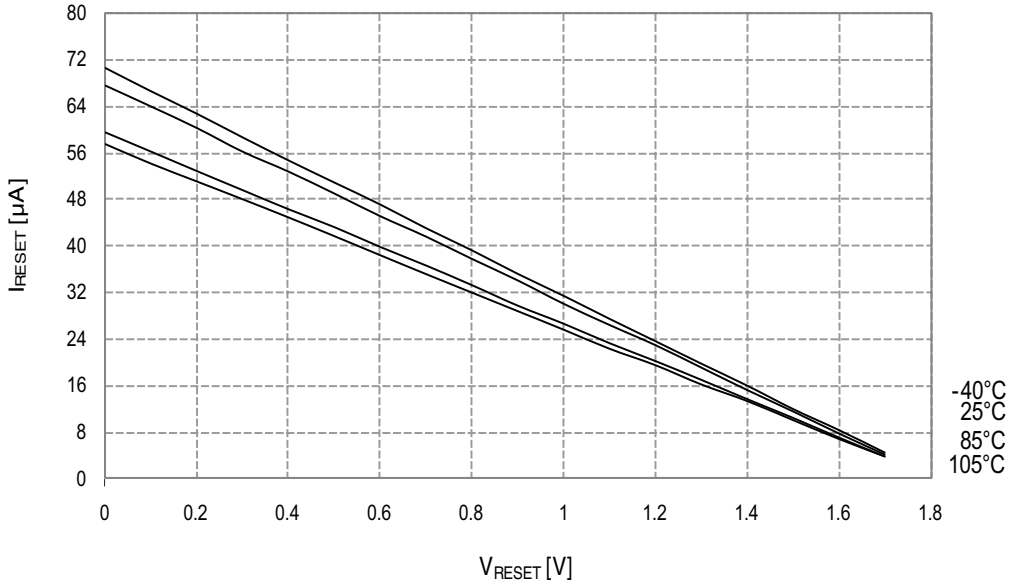
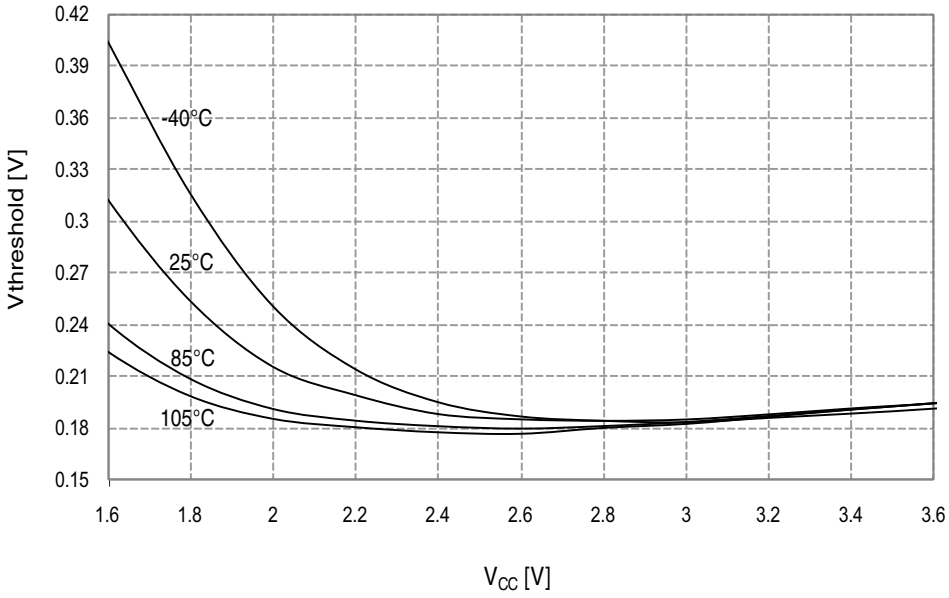


Figure 34-114. I/O Pin Input Hysteresis vs. V_{CC}



34.2.3 ADC Characteristics

Figure 34-115. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

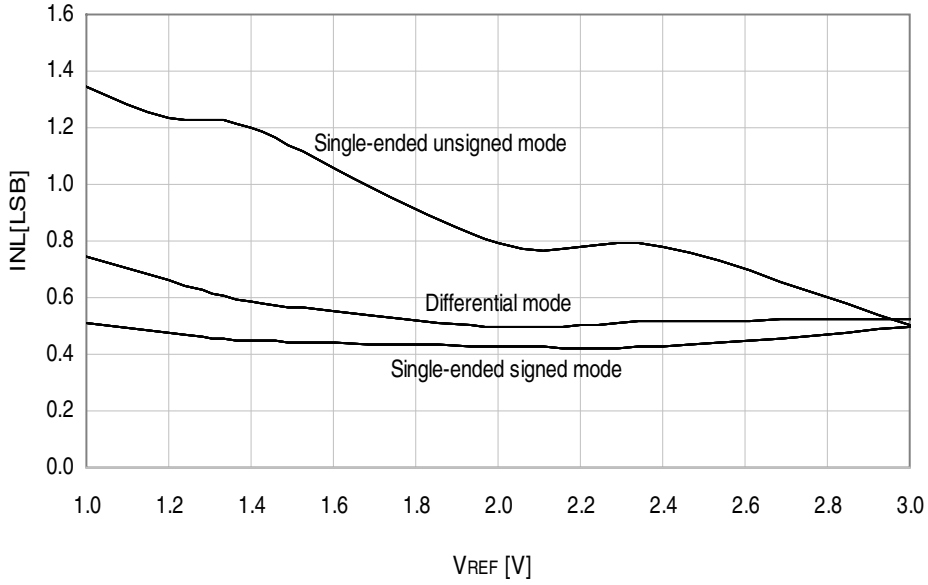


Figure 34-124. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

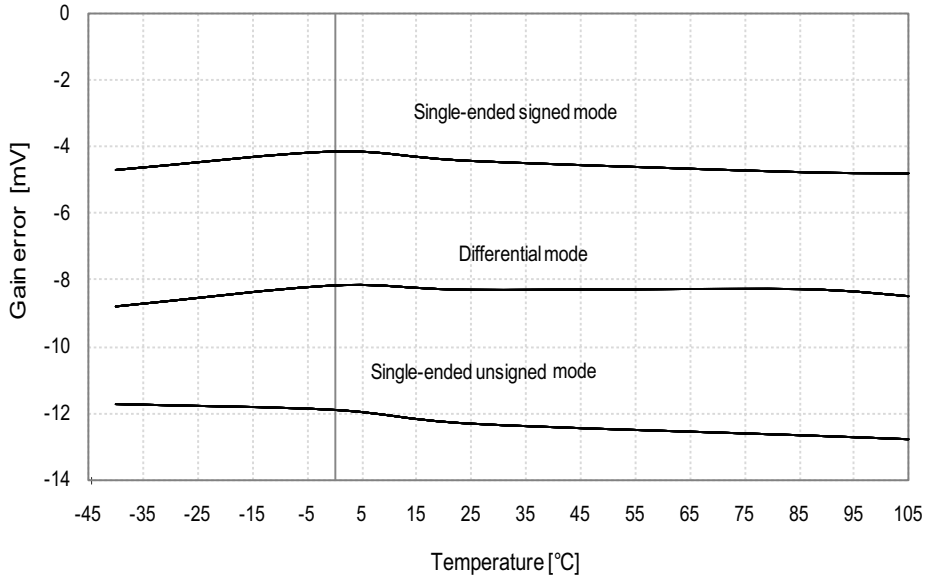
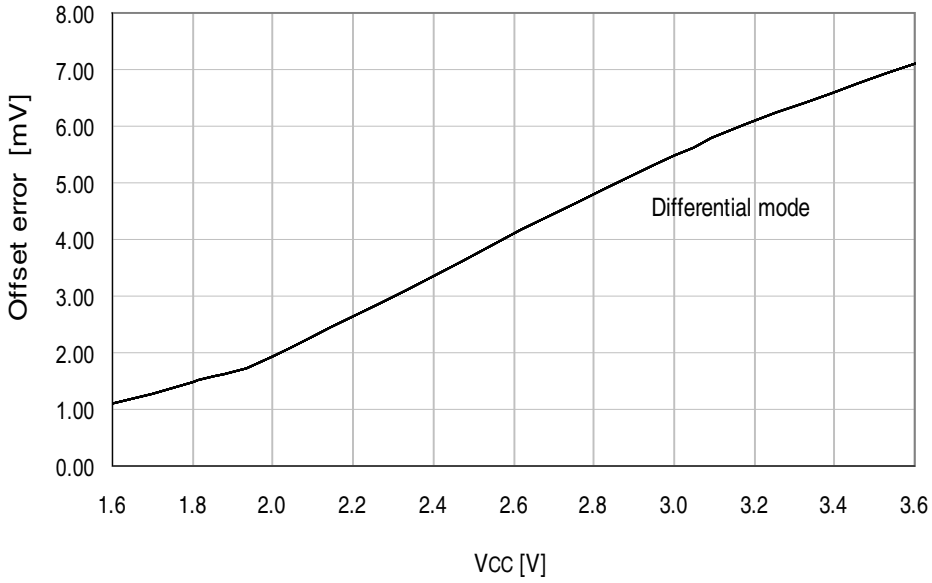


Figure 34-125. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



34.2.7 External Reset Characteristics

Figure 34-136. Minimum Reset Pin Pulse Width vs. V_{CC}

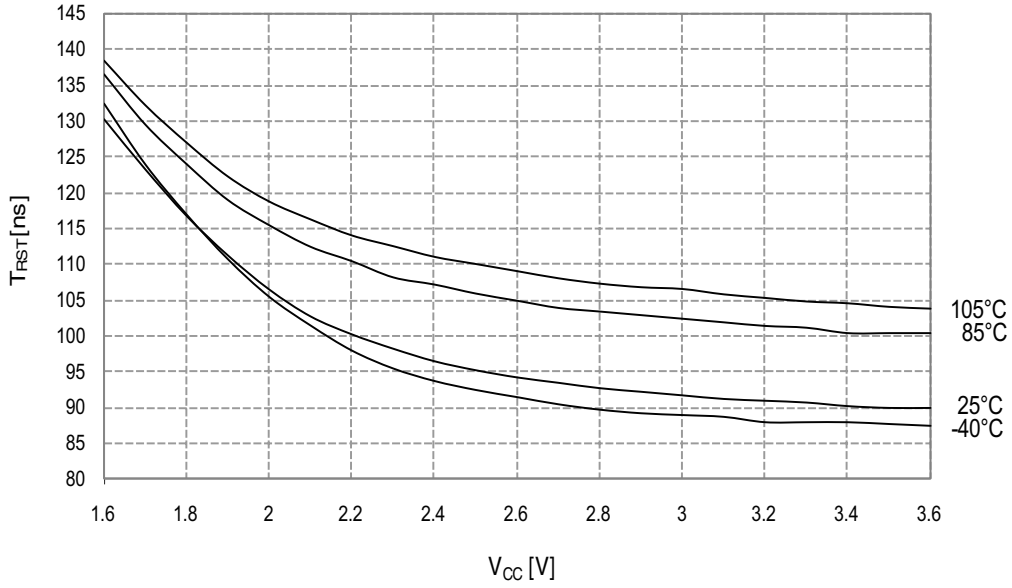
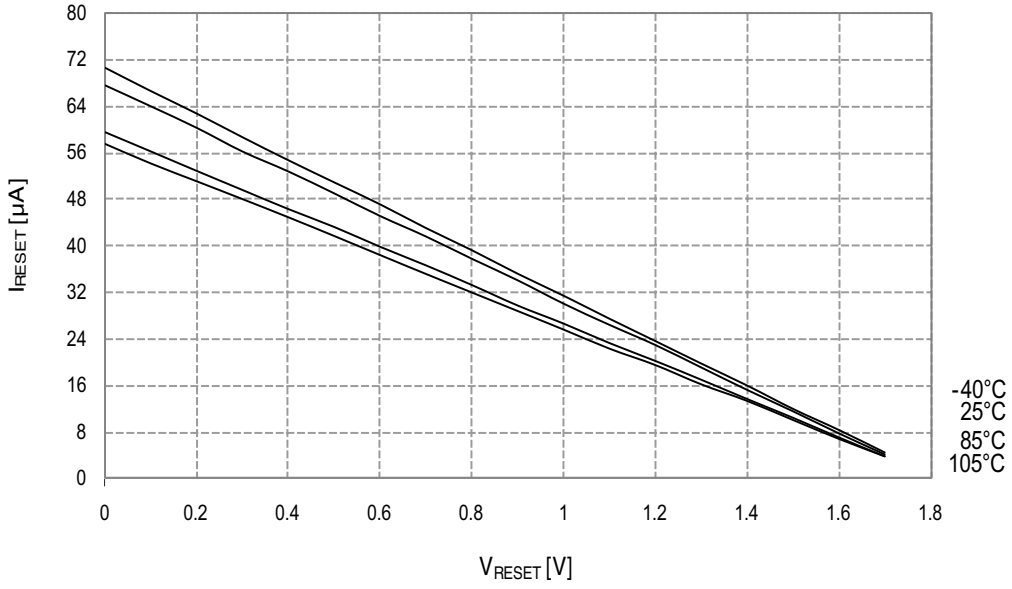


Figure 34-137. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V



34.2.10 Two-Wire Interface Characteristics

Figure 34-156. SDA Hold Time vs. Temperature

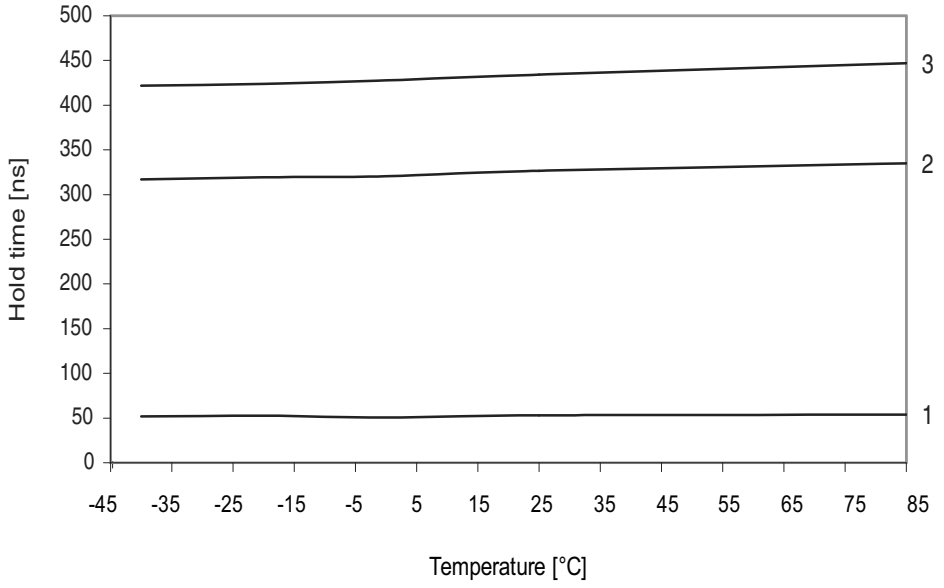
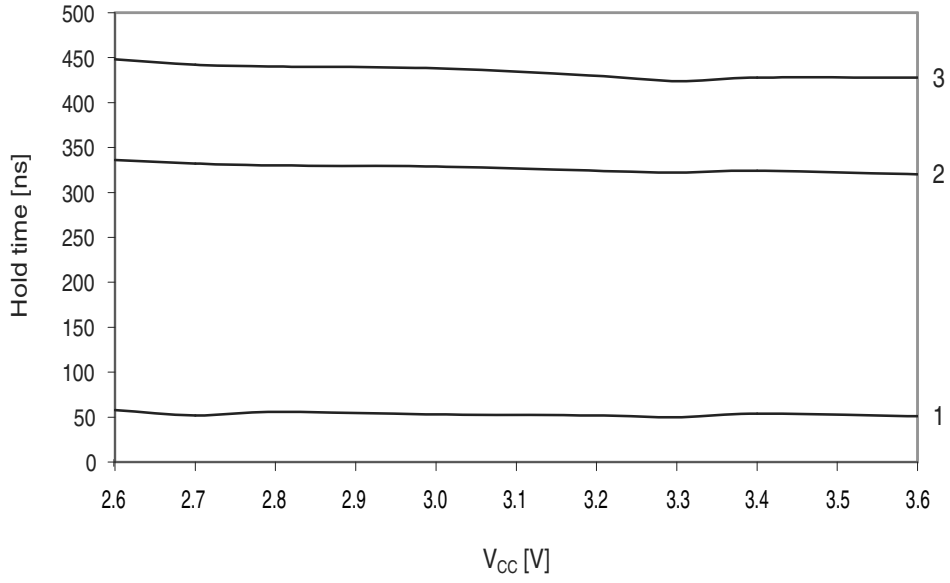


Figure 34-157. SDA Hold Time vs. Supply Voltage



36. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 8493I – 12/2014

1.	Some minor corrections according to the template.
2.	Trademark corrections.
3.	Several cross-references have been corrected.

36.2 8493H – 07/2014

1.	Updated the “Ordering Information” on page 2. Added ordering codes for ATxmega16C4/32C4 @ 105°C.
2.	Updated Table 33-4 on page 67 and Table 33-33 on page 86. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
3.	Updated Table 33-17 on page 75 and Table 33-46 on page 94. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
4.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and in Section 27.1 “Features” on page 48.
5.	Updated the typical characteristics of “Atmel ATxmega16C4” and “Atmel ATxmega32C4” with characterizations @105°C
6.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 27. “AC – Analog Comparator” on page 48.
7.	Changed values for TCCO in Table 29-3 on page 53.

36.3 8493G – 01/2014

1.	Updated the typical characteristics with characterization at 105°C.

36.4 8493F – 10/2013

1.	Updated pin locations of TOSC1 and TOSC2 in Port E - Alternate functions in Table 29-5 on page 54.
2.	Updated pin locations of XTAL1, XTAL2, TOSC1, and TOSC2 in Port R - Alternate functions in Table 29-6 on page 54.

36.5 8493E – 10/2013

1.	Updated Port C - Alternate functions in Table 29-3 on page 53.