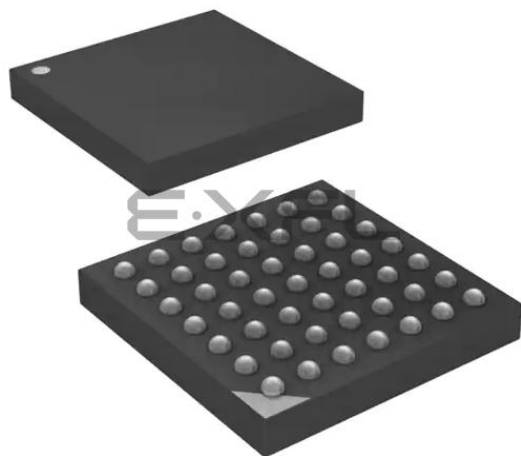




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16c4-cu

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA C4 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); four, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The XMEGA C4 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

16. TC2 – Timer/Counter Type 2

16.1 Features

- Four eight-bit timer/counters
 - Two Low-byte timer/counter
 - Two High-byte timer/counter
- Up to eight compare channels in each timer/counter 2
 - Four compare channels for the low-byte timer/counter
 - Four compare channels for the high-byte timer/counter
- Waveform generation
 - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control

16.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts and events. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC and PORTD each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2) and TCD2 respectively.

20. USB – Universal Serial Bus Interface

20.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 31 endpoints
 - One input endpoint per endpoint address
 - One output endpoint per endpoint address
- Endpoint address transfer type selectable to
 - Control transfers
 - Interrupt transfers
 - Bulk transfers
 - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023 bytes
- Endpoint configuration and data buffers located in internal SRAM
 - Configurable location for endpoint configuration data
 - Configurable location for each endpoint's data buffer
- Built-in direct memory access (DMA) to internal SRAM for:
 - Endpoint configurations
 - Reading and writing endpoint data
- Ping-pong operation for higher throughput and double buffered operation
 - Input and output endpoint data buffers used in a single direction
 - CPU can update data buffer during transfer
- Multipacket transfer for reduced interrupt load and software intervention
 - Data payload exceeding maximum packet size is transferred in one continuous transfer
 - No interrupts or software interaction on packet transaction level
- Transaction complete FIFO for workflow management when using multiple endpoints
 - Tracks all completed transactions in a first-come, first-served work queue
- Clock selection independent of system clock source and selection
- Minimum 1.5MHz CPU clock required for low speed USB operation
- Minimum 12MHz CPU clock required for full speed operation
- Connection to event system
- On chip debug possibilities during USB transactions

20.2 Overview

The USB module is a USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

The USB supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 31 configurable endpoints and one control endpoint. Each endpoint address is fully configurable and can be configured for any of the four transfer types; control, interrupt, bulk, or isochronous. The data payload size is also selectable, and it supports data payloads up to 1023 bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic, according to the number of endpoints in use and the configuration of these. The USB module has built-in direct memory access (DMA), and will read/write data from/to the SRAM when a USB transaction takes place.

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

23. USART

23.1 Features

- Three identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
 - Synchronous clock rates up to 1/2 of the device clock frequency
 - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits, and 1 or 2 stop bits
- Fractional baud rate generator
 - Can generate desired baud rate from any system clock frequency
 - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
 - Odd or even parity generation and parity check
 - Data overrun and framing error detection
 - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
 - Transmit complete
 - Transmit data register empty
 - Receive complete
- Multiprocessor communication mode
 - Addressing scheme to address a specific devices on a multidevice bus
 - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
 - Double buffered operation
 - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

23.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC has two USARTs and PORTD has one USART. Notation of these peripherals are USARTC0, USARTC1, and USARTD0 respectively.

24. IRCOM – IR Communication Module

24.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
 - 3/16 of the baud rate period
 - Fixed pulse period, 8-bit programmable
 - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

24.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

Base address	Name	Description
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/counter 0 on port C
0x0840	TCC1	Timer/counter 1 on port C
0x0880	AWEXC	Advanced waveform extension on port C
0x0890	HIRES	High resolution extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial peripheral interface on port C
0x08F8	IRCOM	Infrared communication module
0x0900	TCD0	Timer/counter 0 on port D
0x09A0	USARTD0	USART 0 on port D
0x09C0	SPID	Serial peripheral interface on port D
0x0A00	TCE0	Timer/counter 0 on port E

Table 33-25. External Clock with Prescaler ⁽¹⁾ for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
1/t _{CK}	Clock Frequency ⁽²⁾	V _{CC} = 1.6 - 1.8V	0		90	MHz
		V _{CC} = 2.7 - 3.6V	0		142	
t _{CK}	Clock Period	V _{CC} = 1.6 - 1.8V	11			ns
		V _{CC} = 2.7 - 3.6V	7			
t _{CH}	Clock High Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CL}	Clock Low Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CR}	Rise Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
t _{CF}	Fall Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
Δt _{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.1.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 33-26. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0	0		ns
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0	0		
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Frequency error	XOSCPWR=0	FRQRANGE=0	0.03		%
			FRQRANGE=1	0.03		
			FRQRANGE=2 or 3	0.03		
		XOSCPWR=1		0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0	50		
			FRQRANGE=1	50		
			FRQRANGE=2 or 3	50		
		XOSCPWR=1		50		

33.2.8 Bandgap and Internal 1.0V Reference Characteristics

Table 33-42. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk _{PER} + 2.5μs			μs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.98	1	1.02	
	Variation over voltage and temperature	Calibrated at T= 85°C, V _{CC} = 3.0V		±1.0		%

33.2.9 Brownout Detection Characteristics

Table 33-43. Brownout Detection Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{BOT}	BOD level 0 falling V _{CC}		1.50	1.62	1.75	V
	BOD level 1 falling V _{CC}			1.8		
	BOD level 2 falling V _{CC}			2.0		
	BOD level 3 falling V _{CC}			2.2		
	BOD level 4 falling V _{CC}			2.4		
	BOD level 5 falling V _{CC}			2.6		
	BOD level 6 falling V _{CC}			2.8		
	BOD level 7 falling V _{CC}			3.0		
t _{BOD}	Detection time	Continuous mode		0.4		μs
		Sampled mode		1000		
V _{HYST}	Hysteresis			1.2		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

33.2.10 External Reset Characteristics

Table 33-44. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t _{EXT}	Minimum reset pulse width		1000	90		ns
V _{RST}	Reset threshold voltage (V _{IH})	V _{CC} = 2.7 - 3.6V	0.6*V _{CC}			V
		V _{CC} = 1.6 - 2.7V	0.6*V _{CC}			
	Reset threshold voltage (V _{IL})	V _{CC} = 2.7 - 3.6V			0.5*V _{CC}	
		V _{CC} = 1.6 - 2.7V			0.4*V _{CC}	
R _{RST}	Reset pin pull-up resistor			25		kΩ

33.2.11 Power-on Reset Characteristics

Table 33-45. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{POT-}^{(1)}$	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

33.2.12 Flash and EEPROM Memory Characteristics

Table 33-46. Endurance and Data Retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K		Cycle
			85°C	10K		
			105°C	2K		
		Data retention	25°C	100		Year
			85°C	25		
			105°C	10		
	EEPROM	Write/Erase cycles	25°C	100K		Cycle
			85°C	100K		
			105°C	30K		
		Data retention	25°C	100		Year
			85°C	25		
			105°C	10		

Table 33-47. Programming time.

Symbol	Parameter	Condition	Min.	Typ. ⁽¹⁾	Max.	Units
	Chip erase ⁽²⁾	32KB Flash, EEPROM		50		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

33.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.2.13.6 External Clock Characteristics

Figure 33-10. External Clock Drive Waveform

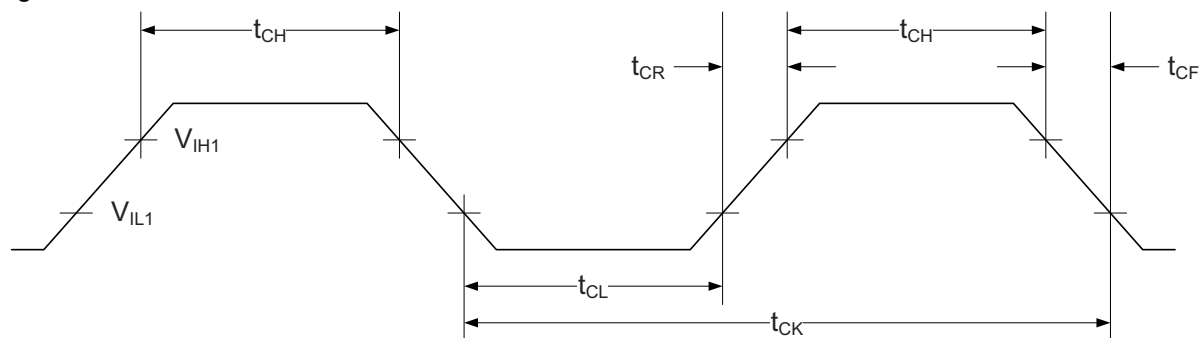


Table 33-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock high time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock low time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Figure 34-3. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768kHz$ internal oscillator

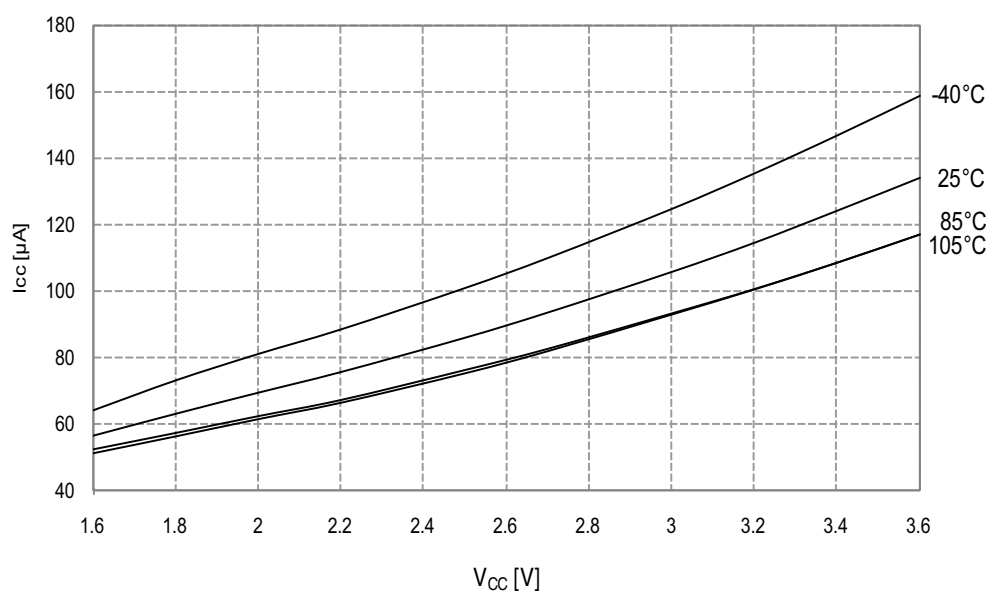
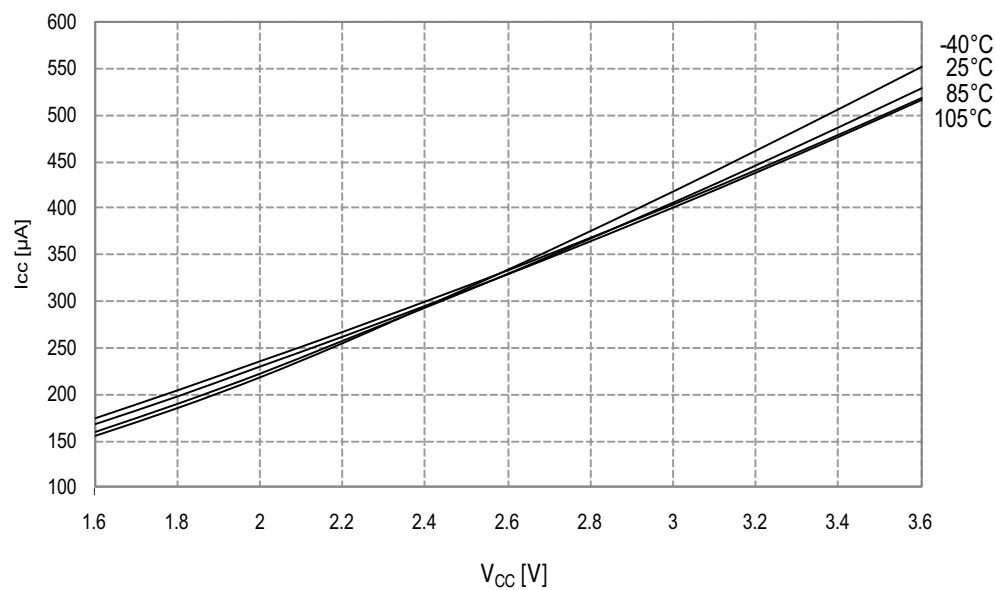


Figure 34-4. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 1MHz$ external clock



34.1.1.5 Standby Mode Supply Current

Figure 34-19. Standby Supply Current vs. V_{CC}
Standby, $f_{SYS} = 1\text{MHz}$

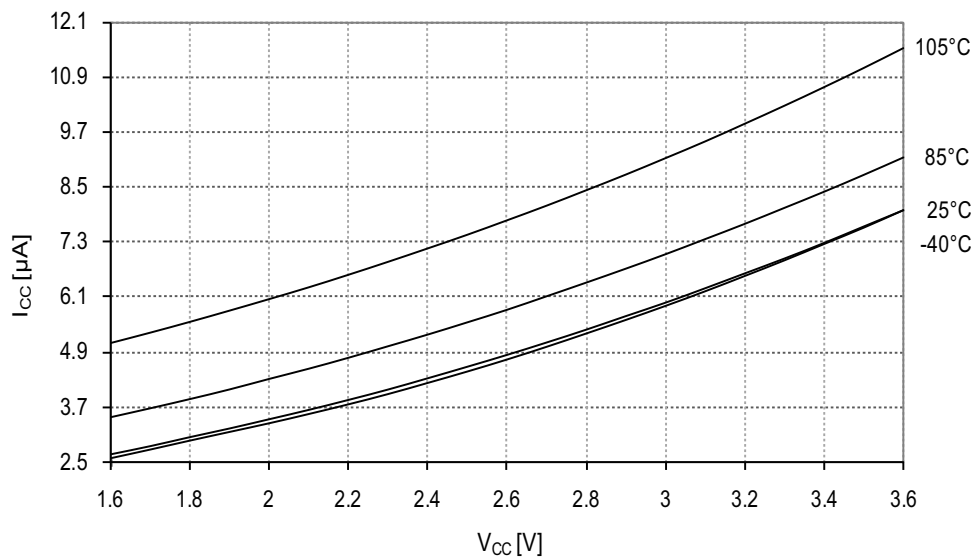


Figure 34-20. Standby Supply Current vs. V_{CC}
25°C, running from different crystal oscillators

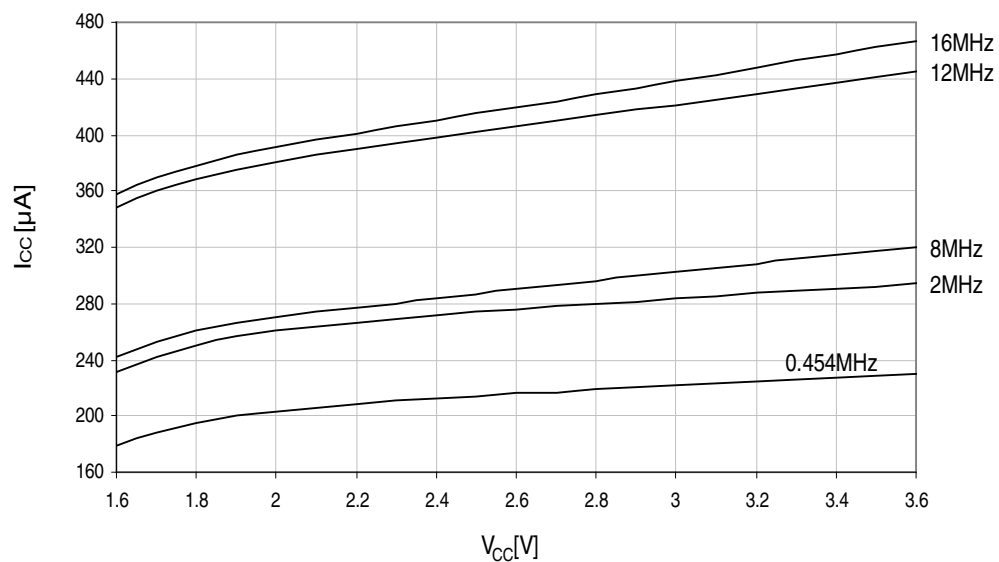


Figure 34-88. Idle Mode Supply Current vs. Frequency

$f_{SYS} = 1 - 32\text{MHz}$ external clock, $T = 25^\circ\text{C}$

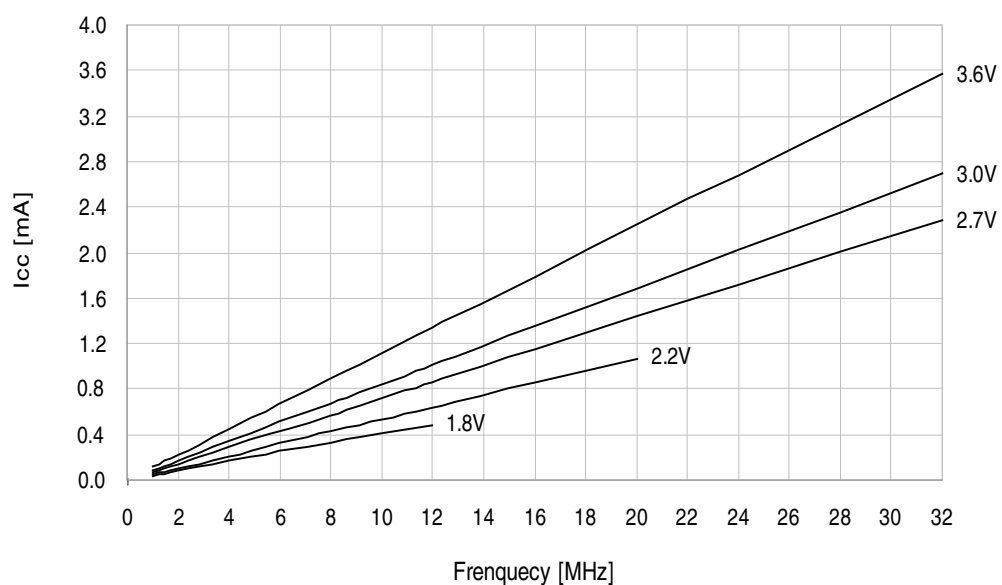
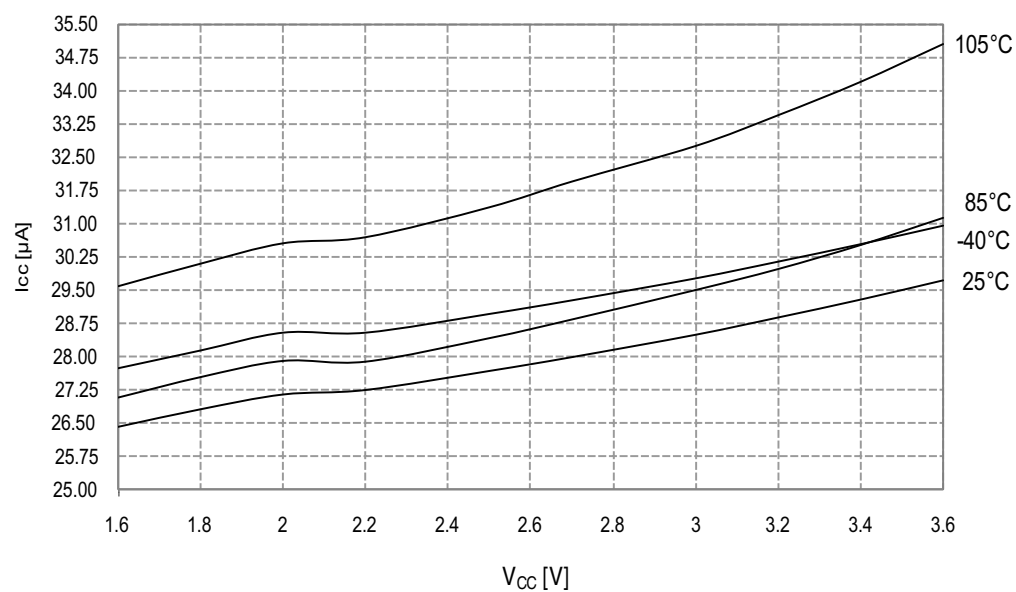


Figure 34-89. Idle Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator



34.2.2 I/O Pin Characteristics

34.2.2.1 Pull-up

Figure 34-100. I/O Pin Pull-up Resistor Current vs. Input Voltage
 $V_{CC} = 1.8V$

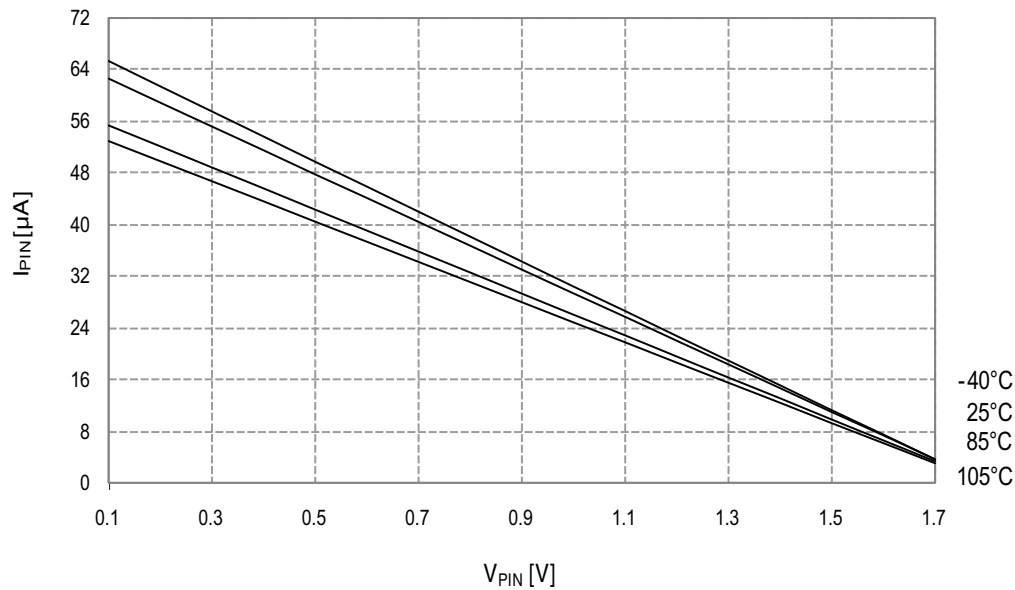


Figure 34-101. I/O Pin Pull-up Resistor Current vs. Input Voltage
 $V_{CC} = 3.0V$

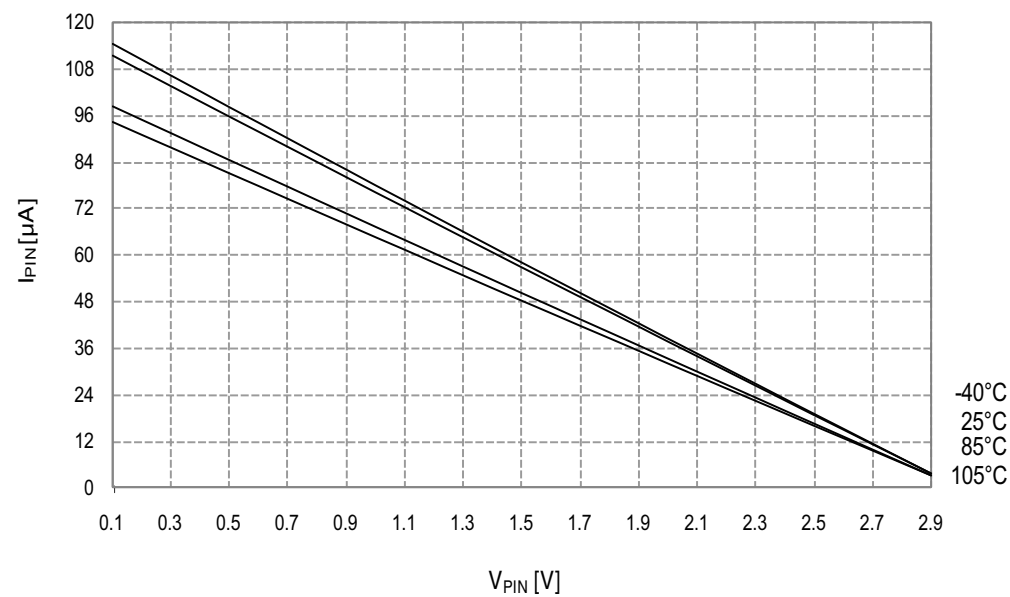


Figure 34-116. INL Error vs. Sample Rate

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, $V_{REF} = 3.0\text{V external}$

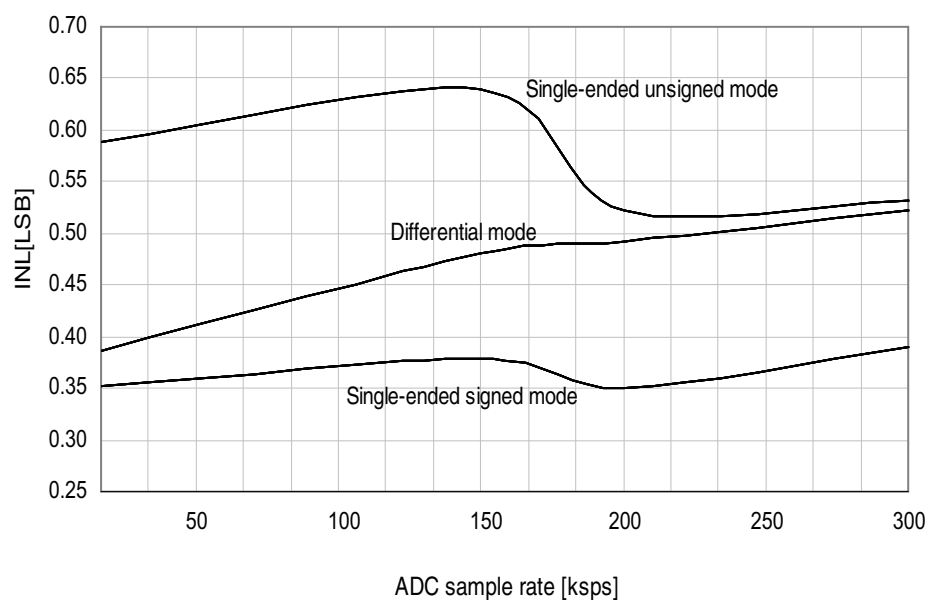
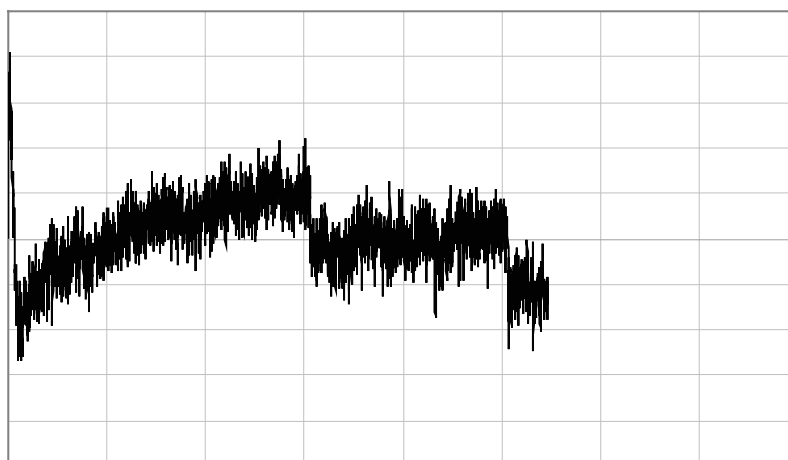


Figure 34-117. INL Error vs. Input Code



34.2.8 Power-on Reset Characteristics

Figure 34-142. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode

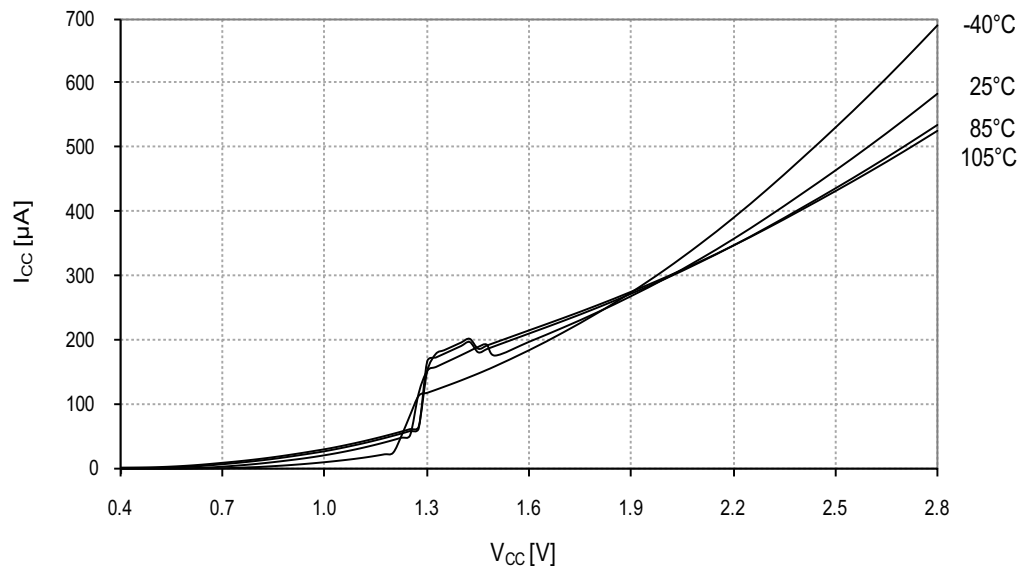


Figure 34-143. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode

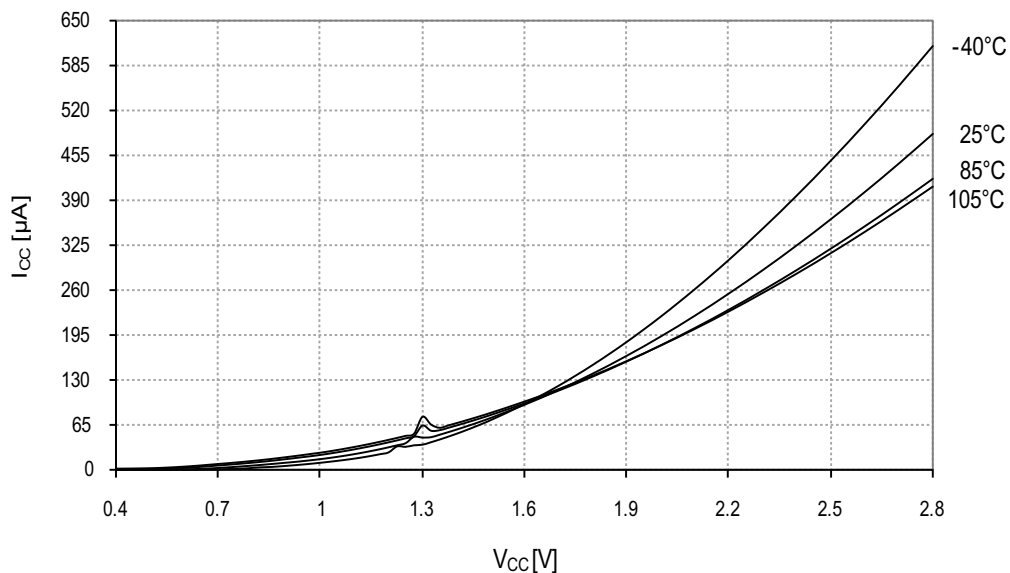
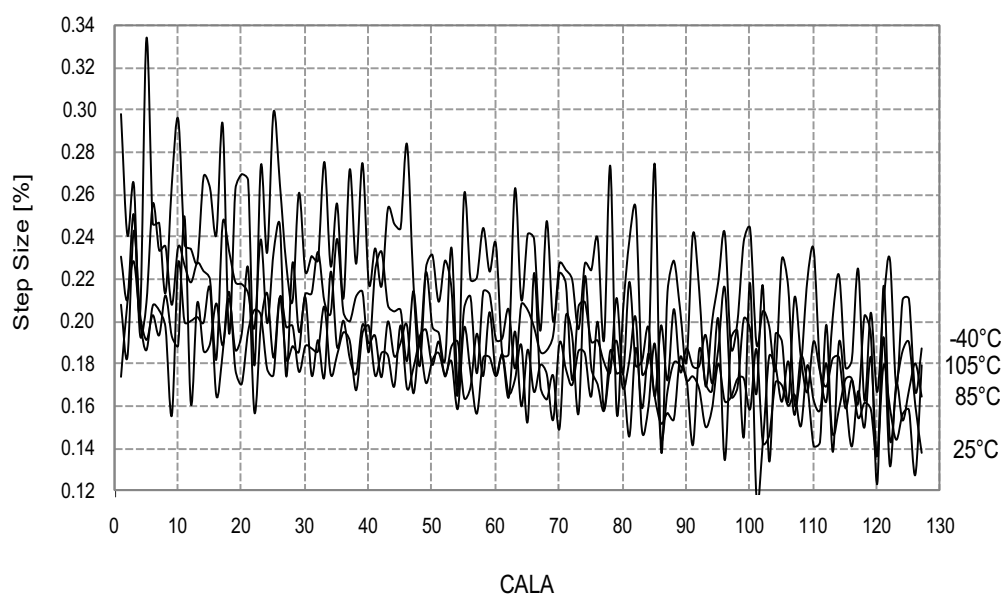


Figure 34-152. 32MHz Internal Oscillator CALA Calibration Step Size

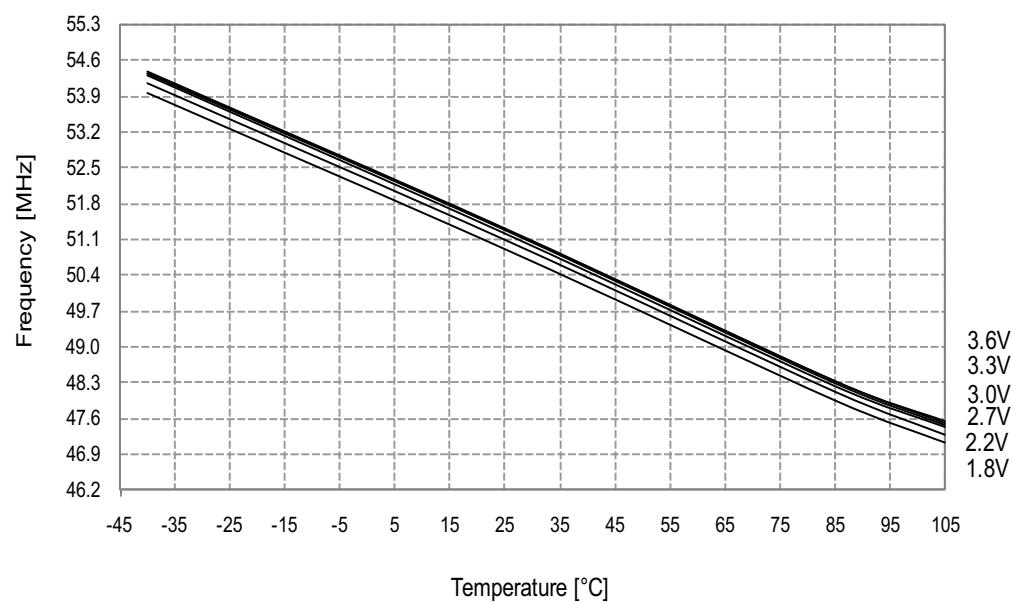
$V_{CC} = 3.0V$



34.2.9.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-153. 48MHz Internal Oscillator Frequency vs. Temperature

DPLL disabled



36.6 8493D – 07/2013.

1.	Errata Temperature sensor not calibrated added to: • ATxmega32C4 “Rev. H” on page 183 • ATxmega16C4 “Rev. H” on page 183
----	---

36.7 8493C – 02/2013

1.	Updated the datasheet with Atmel new blue logo.
2.	Updated Figure 2-1 on page 4. PE2/PE3 are now half gray.
3.	Updated Figure 2-1 on page 4. Pin 19 is V_{CC} and not V_{DD} .
4.	Added Figure 2-2 on page 5.
5.	Updated Table 7-1 on page 15. Device ID for ATxmega32C4 is 44; 95; 1E. Device ID for ATxmega16 is 43; 94; 1E
6.	Updated “I/O Ports” on page 29. Removed “Optional slew rate control”. The feature doesn't exist in XMEGA C and XMEGA D devices.
7.	Updated Figure 27-1 on page 49, “Analog Comparator Overview”
8.	Updated “Pinout and Pin Functions” on page 51, to take into account the “Pinout/Block Diagram” on page 4.
9.	Updated “External Clock Characteristics” on page 77 and “ External Clock Characteristics” on page 96. Added Table 33-24 on page 77, Table 33-25 on page 78, Table 33-53 on page 96, and Table 33-54 on page 97.
10.	Updated Table 33-26 on page 78, and Table 33-55 on page 97. Added ESR parameter.
11.	Updated Table 33-29 on page 83 and Table 33-58 on page 102. Input low voltage V_{IL} min for I ² C is -0.5V.
12.	Added “Electrical Characteristics” for “Atmel ATxmega16C4” on page 65.
13.	Added “Typical Characteristics” for “Atmel ATxmega16C4” on page 103.
15.	Updated “Errata” on page 183. Added Errata to all rev H: AC system status flags are only valid if AC-system is enabled.

36.8 8493B – 05/2012

1.	Updated “Packaging Information” on page 62. Added “7P” on page 64.
2.	Added “Electrical Characteristics” on page 65.
3.	Added “Typical Characteristics” on page 103.

36.9 8493A – 02/2012

1.	Initial revision.
----	-------------------

11. System Control and Reset	24
11.1 Features	24
11.2 Overview	24
11.3 Reset Sequence	24
11.4 Reset Sources	25
12. WDT – Watchdog Timer	26
12.1 Features	26
12.2 Overview	26
13. Interrupts and Programmable Multilevel Interrupt Controller	27
13.1 Features	27
13.2 Overview	27
13.3 Interrupt Vectors	27
14. I/O Ports	29
14.1 Features	29
14.2 Overview	29
14.3 Output Driver	30
14.4 Input Sensing	32
14.5 Alternate Port Functions	32
15. TC0/1 – 16-bit Timer/Counter Type 0 and 1	33
15.1 Features	33
15.2 Overview	33
16. TC2 – Timer/Counter Type 2	35
16.1 Features	35
16.2 Overview	35
17. AWeX – Advanced Waveform Extension	36
17.1 Features	36
17.2 Overview	36
18. Hi-Res – High Resolution Extension	37
18.1 Features	37
18.2 Overview	37
19. RTC – 16-bit Real-Time Counter	38
19.1 Features	38
19.2 Overview	38
20. USB – Universal Serial Bus Interface	39
20.1 Features	39
20.2 Overview	39
21. TWI – Two-Wire Interface	41
21.1 Features	41
21.2 Overview	41
22. SPI – Serial Peripheral Interface	42
22.1 Features	42
22.2 Overview	42

23. USART	43
23.1 Features	43
23.2 Overview	43
24. IRCOM – IR Communication Module	44
24.1 Features	44
24.2 Overview	44
25. CRC – Cyclic Redundancy Check Generator	45
25.1 Features	45
25.2 Overview	45
26. ADC – 12-bit Analog to Digital Converter	46
26.1 Features	46
26.2 Overview	46
27. AC – Analog Comparator	48
27.1 Features	48
27.2 Overview	48
28. Programming and Debugging	50
28.1 Features	50
28.2 Overview	50
29. Pinout and Pin Functions	51
29.1 Alternate Pin Function Description	51
29.2 Alternate Pin Functions	53
30. Peripheral Module Address Map	55
31. Instruction Set Summary	57
32. Packaging Information	62
32.1 44A	62
32.2 PW	63
32.3 7P	64
33. Electrical Characteristics	65
33.1 Atmel ATxmega16C4	65
33.2 Atmel ATxmega32C4	84
34. Typical Characteristics	103
34.1 Atmel ATxmega16C4	103
34.2 Atmel ATxmega32C4	143
35. Errata	183
35.1 Atmel ATxmega32C4	183
35.2 Atmel ATxmega16C4	183
36. Datasheet Revision History	184
36.1 8493I – 12/2014	184
36.2 8493H – 07/2014	184
36.3 8493G – 01/2014	184
36.4 8493F – 10/2013	184