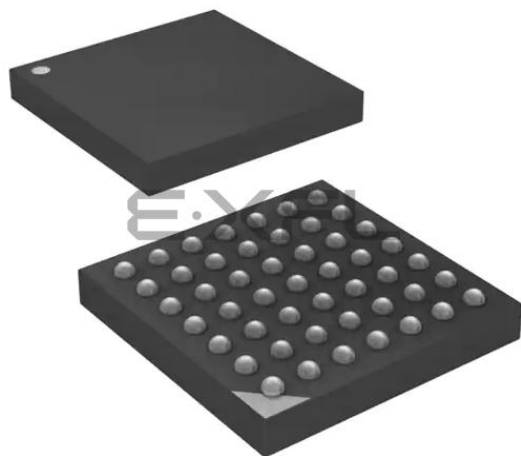




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Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16c4-cur

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes:
 - Idle
 - Power down
 - Power save
 - Standby
 - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

10.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

10.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

10.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

24. IRCOM – IR Communication Module

24.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
 - 3/16 of the baud rate period
 - Fixed pulse period, 8-bit programmable
 - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

24.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

27. AC – Analog Comparator

27.1 Features

- Two Analog Comparators (AC)
- Selectable hysteresis
 - No
 - Small
 - Large
- Analog comparator output available on pin
- Flexible input selection
 - All pins on the port
 - Bandgap reference voltage
 - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
 - Rising edge
 - Falling edge
 - Toggle
- Window function interrupt and event generation on:
 - Signal above window
 - Signal inside window
 - Signal below window
- Constant current source with configurable output pin selection

27.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

The analog comparator hysteresis can be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 ⁽¹⁾
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 ⁽¹⁾
CALL	k	call Subroutine	PC ← k	None	3 / 4 ⁽¹⁾
RET		Subroutine Return	PC ← STACK	None	4 / 5 ⁽¹⁾
RETI		Interrupt Return	PC ← STACK	I	4 / 5 ⁽¹⁾
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRs	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) = 1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

32.2 PW

DRAWINGS NOT SCALED				
TOP VIEW		SIDE VIEW		
BOTTOM VIEW				
Notes :				
02/17/2012				
Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat	ZCP	PW	H

33.1.3 Current Consumption

Table 33-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Active power consumption ⁽¹⁾	32kHz, Ext. Clk	$V_{CC} = 1.8V$	40		μA
			$V_{CC} = 3.0V$	80		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	200		
			$V_{CC} = 3.0V$	410		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	350	600	mA
			$V_{CC} = 3.0V$	0.75	1.4	
	Idle power consumption ⁽¹⁾	32kHz, Ext. Clk	$V_{CC} = 1.8V$	2.0		μA
			$V_{CC} = 3.0V$	2.8		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	42		
			$V_{CC} = 3.0V$	85		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	85	225	mA
			$V_{CC} = 3.0V$	170	350	
	Power-down power consumption	T = 25°C	$V_{CC} = 3.0V$	0.1	1.0	μA
				2.0	4.5	
				0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	$V_{CC} = 3.0V$	1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C		3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C		1.4	10	
	Power-save power consumption ⁽²⁾	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	$V_{CC} = 1.8V$	1.5		
			$V_{CC} = 3.0V$	1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.6	2.0	
			$V_{CC} = 3.0V$	0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.8	3.0	
			$V_{CC} = 3.0V$	1.0	3.0	
	Reset power consumption	Current through $\overline{RESET}$ pin subtracted	$V_{CC} = 3.0V$	300		

- Notes:
1. All Power Reduction Registers set.
 2. Maximum limits are based on characterization, and not tested in production.

33.1.13 Clock and Oscillator Characteristics

33.1.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 33-19. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

33.1.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 33-20. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

33.1.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 33-21. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

33.1.13.4 32kHz Internal ULP Oscillator Characteristics

Table 33-22. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

33.1.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-23. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.1.13.6 External Clock Characteristics

Figure 33-3. External Clock Drive Waveform

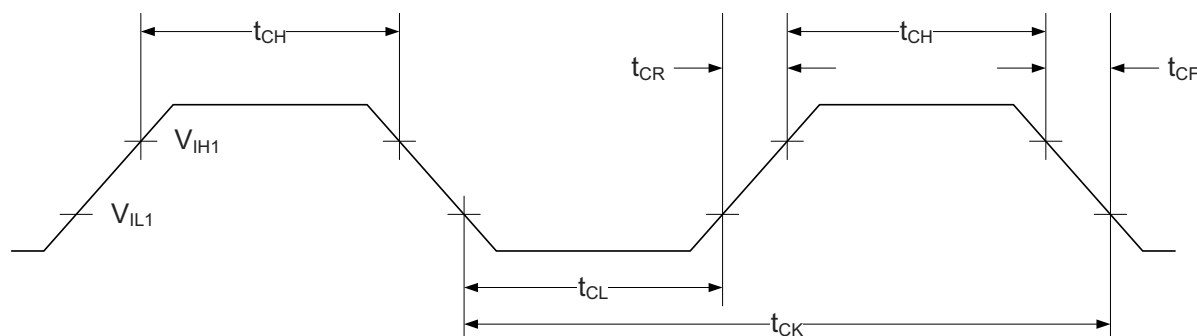


Table 33-24. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock high time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock low time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

33.2.14 SPI Characteristics

Figure 33-12. SPI Timing Requirements in Master Mode

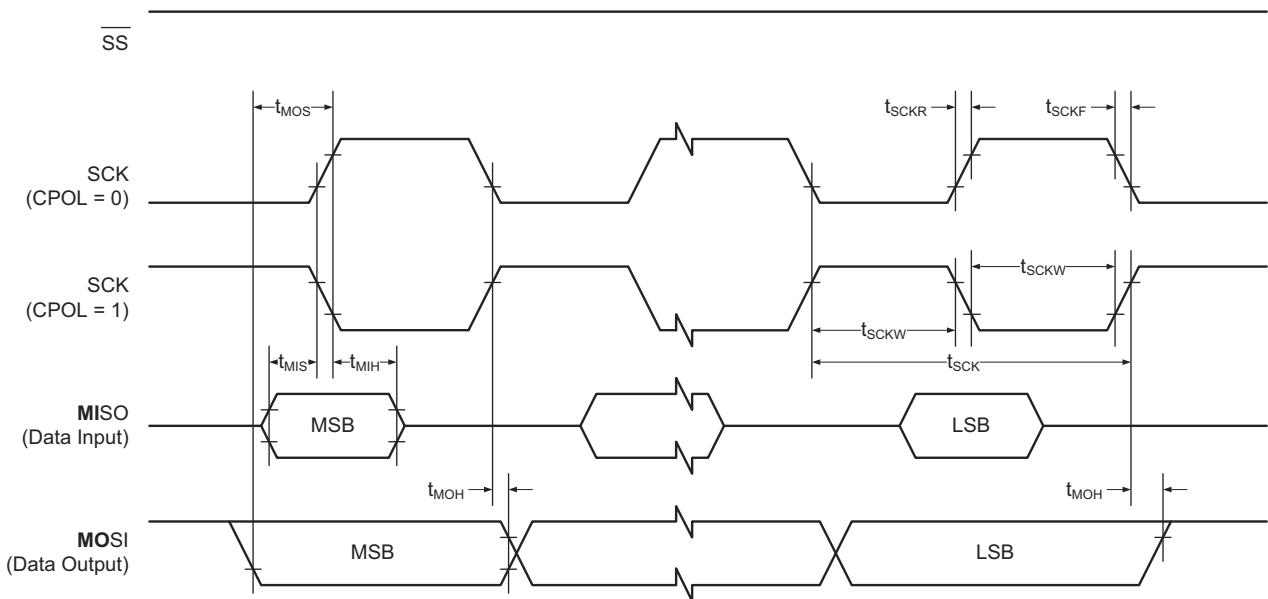


Figure 33-13. SPI Timing Requirements in Slave Mode

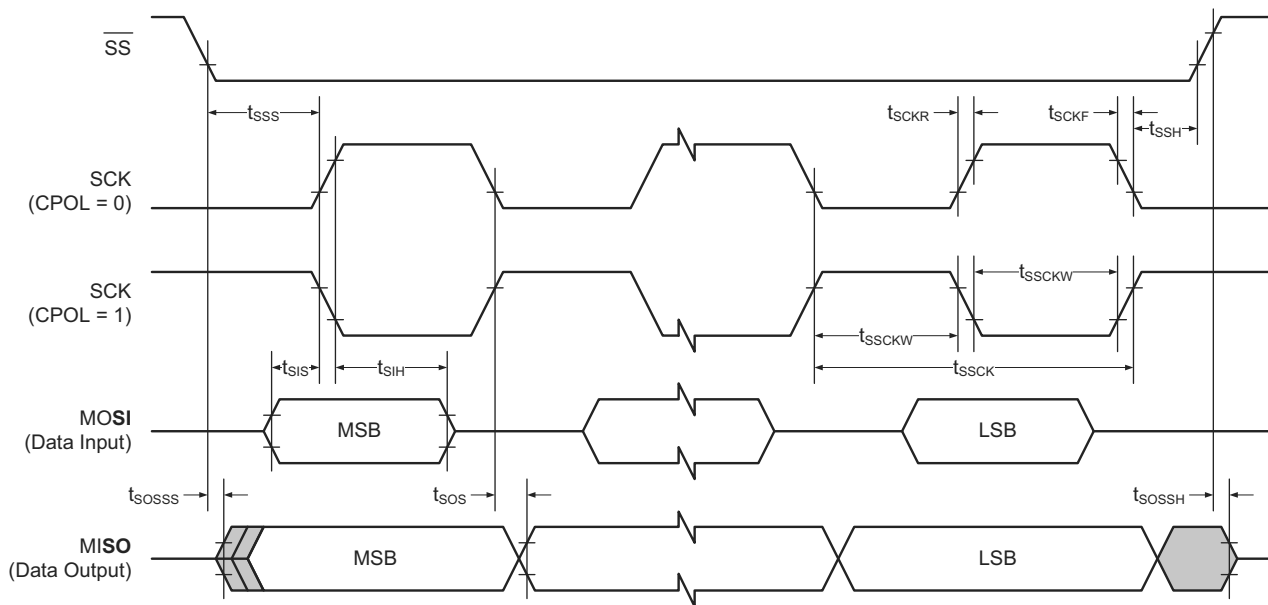
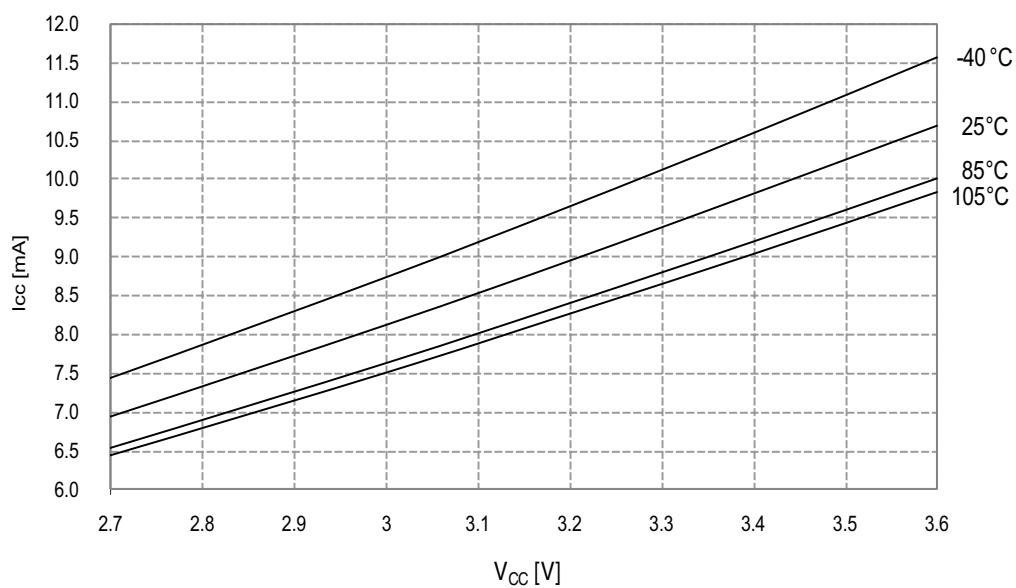


Figure 34-7. Active Mode Supply Current vs. V_{CC}

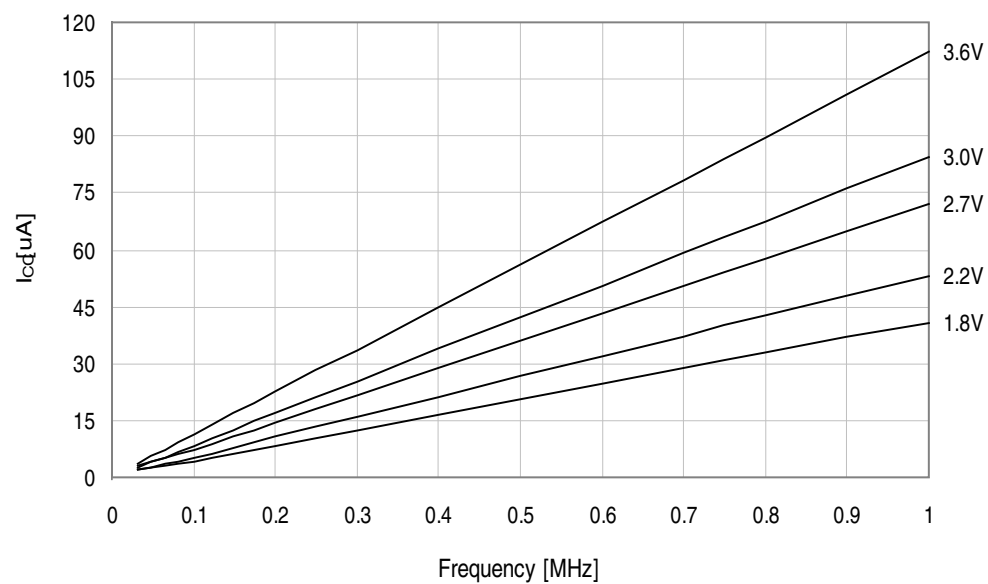
$f_{SYS} = 32\text{MHz}$ internal oscillator



34.1.1.2 Idle Mode Supply Current

Figure 34-8. Idle Mode Supply Current vs. Frequency

$f_{SYS} = 0 - 1\text{MHz}$ external clock, $T = 25^\circ\text{C}$



34.1.2 I/O Pin Characteristics

34.1.2.1 Pull-up

Figure 34-21. I/O Pin Pull-up Resistor Current vs. Input Voltage
 $V_{CC} = 1.8V$

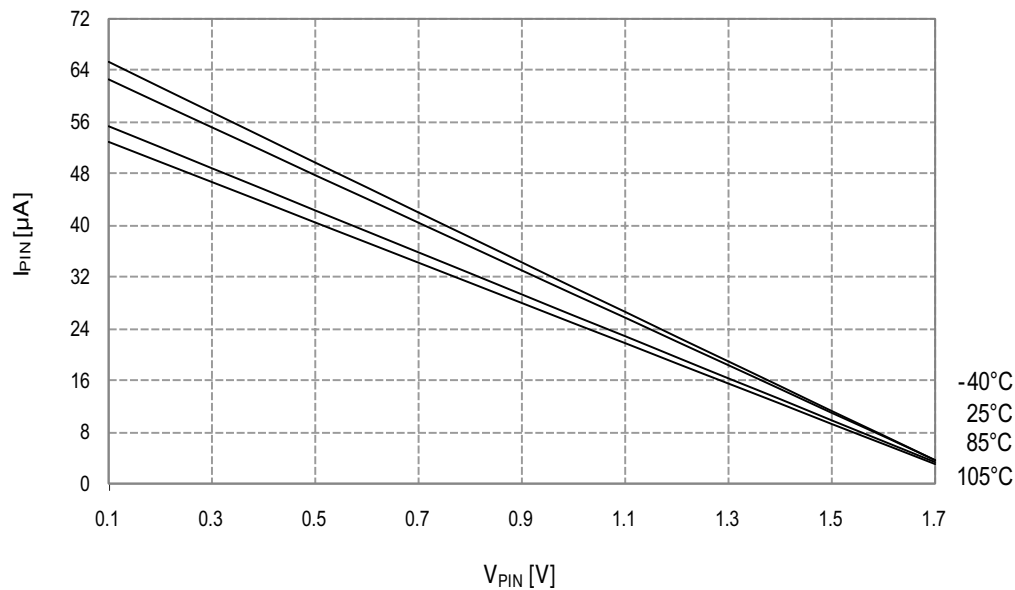


Figure 34-22. I/O Pin Pull-up Resistor Current vs. Input Voltage
 $V_{CC} = 3.0V$

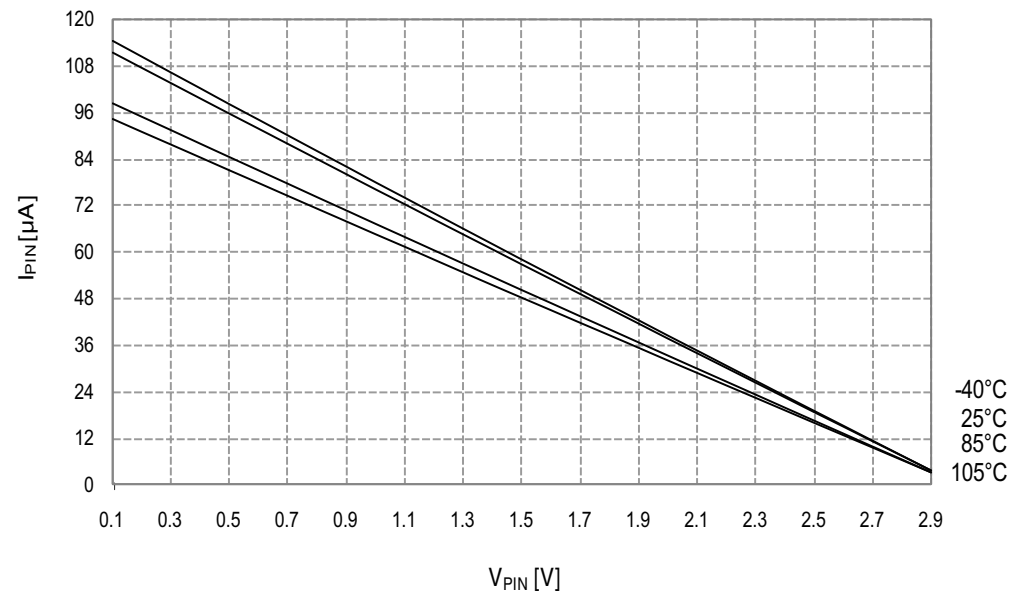
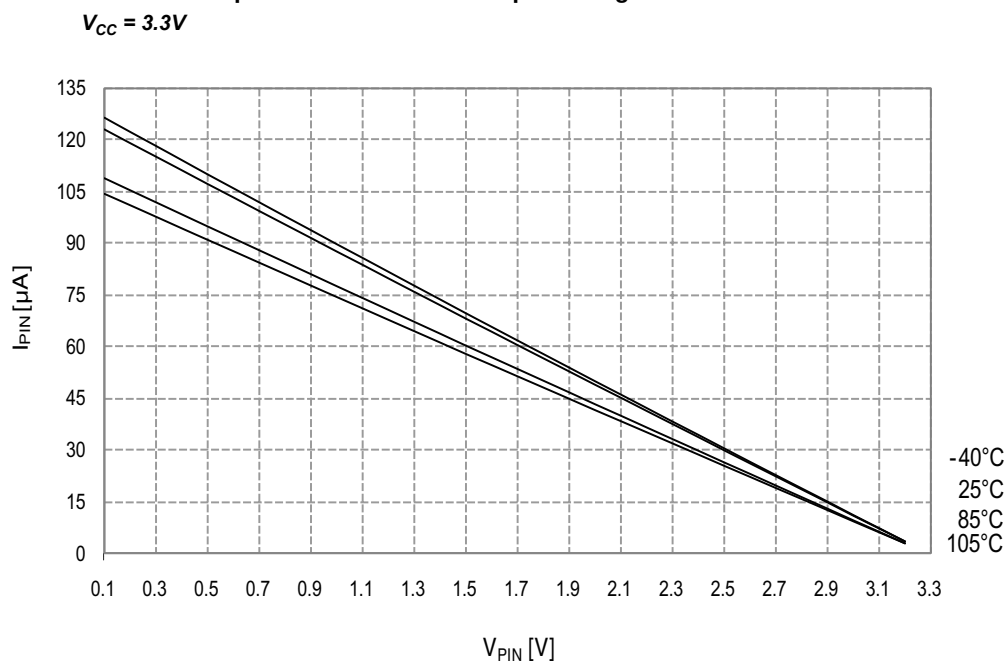


Figure 34-23. I/O Pin Pull-up Resistor Current vs. Input Voltage



34.1.2.2 Output Voltage vs. Sink/Source Current

Figure 34-24. I/O Pin Output Voltage vs. Source Current

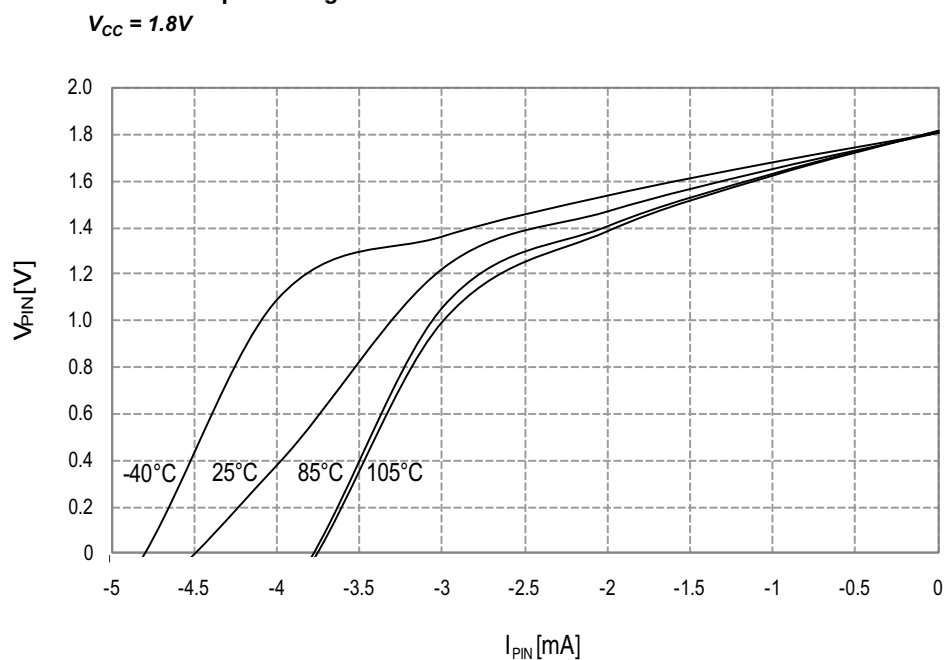
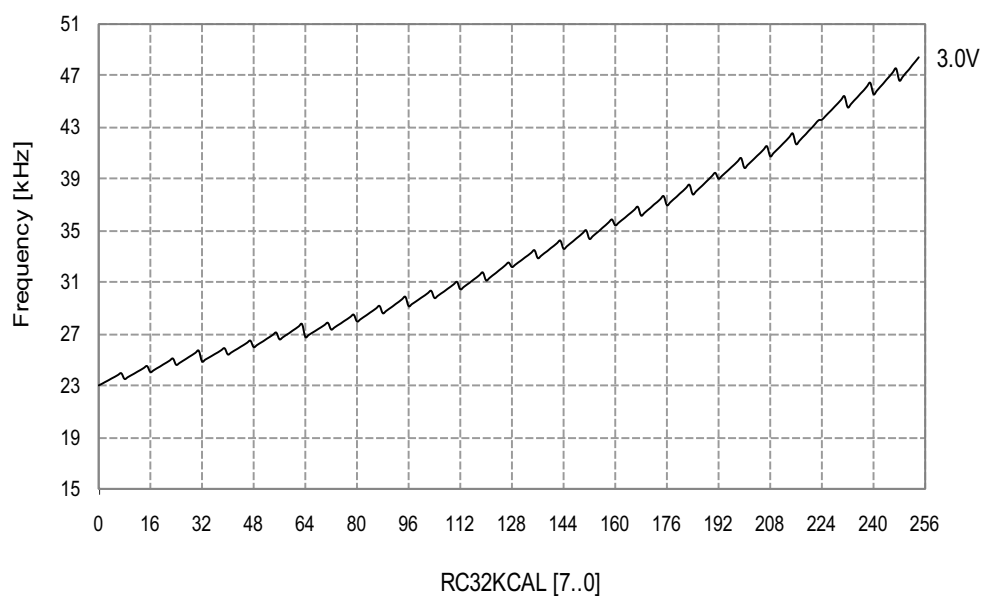


Figure 34-67. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

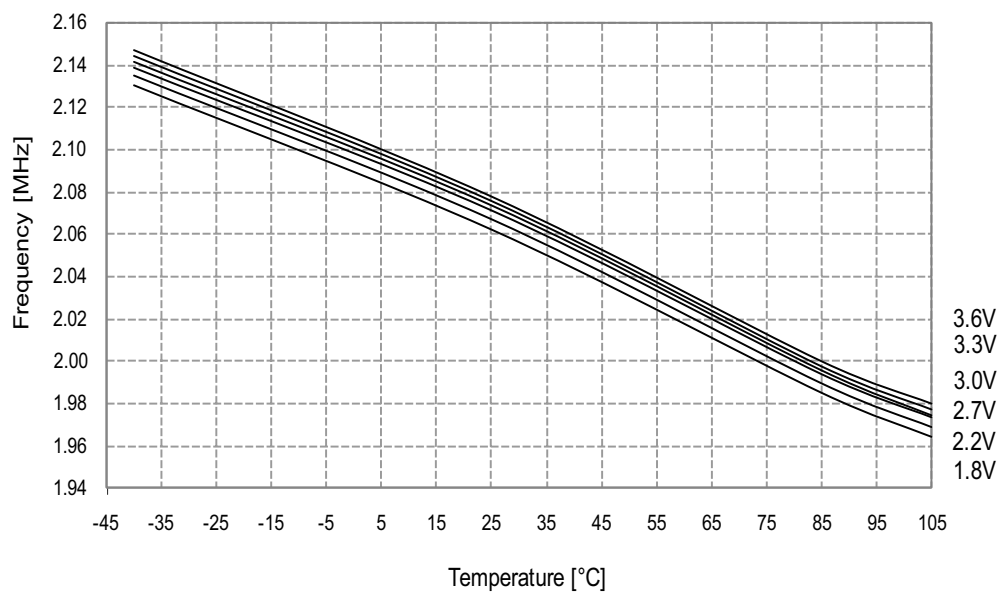
$V_{CC} = 3.0V$, $T = 25^{\circ}C$



34.1.9.3 2MHz Internal Oscillator

Figure 34-68. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



34.1.10 Two-Wire Interface Characteristics

Figure 34-77. SDA Hold Time vs. Temperature

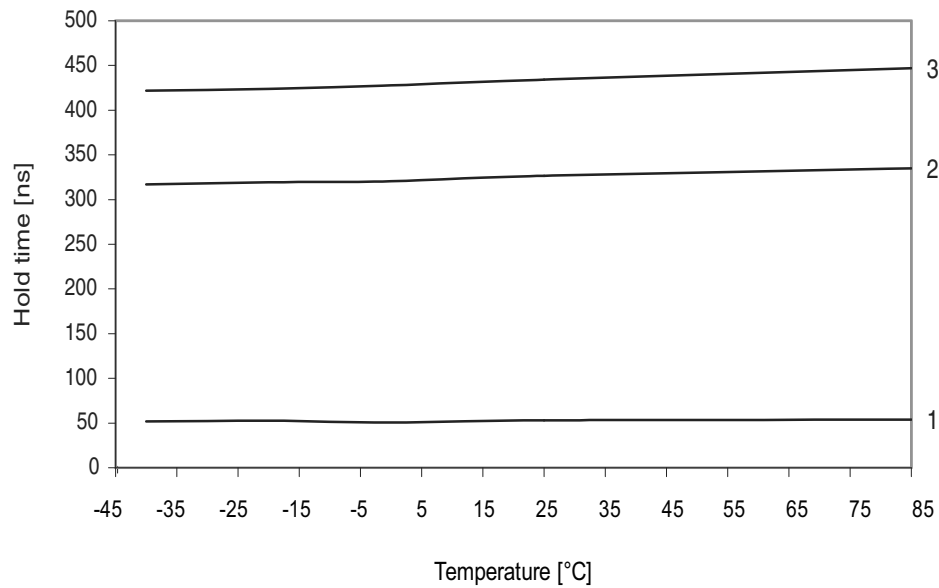
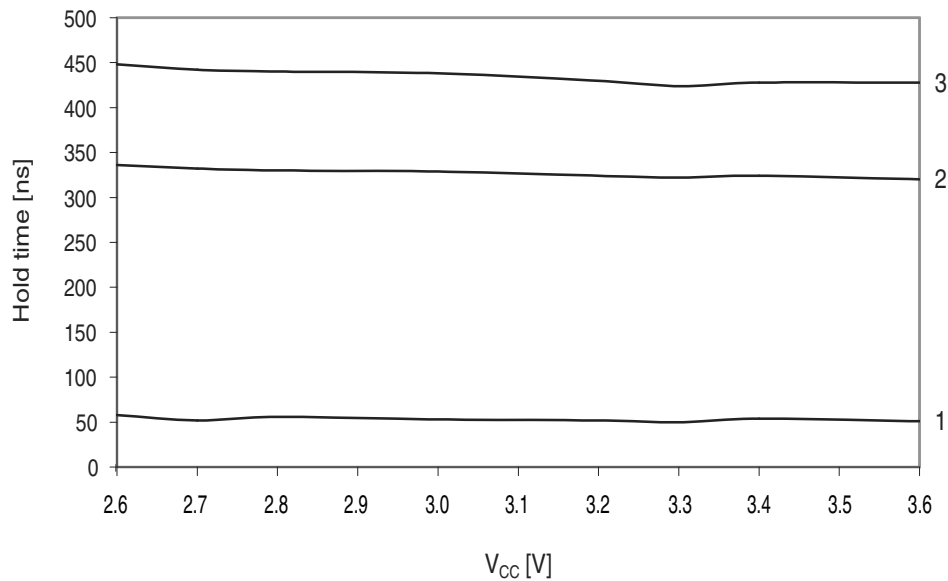


Figure 34-78. SDA Hold Time vs. Supply Voltage



34.2 Atmel ATxmega32C4

34.2.1 Current Consumption

34.2.1.1 Active Mode Supply Current

Figure 34-80. Active Supply Current vs. Frequency

$f_{\text{SYS}} = 0 - 1\text{MHz}$ external clock, $T = 25^\circ\text{C}$

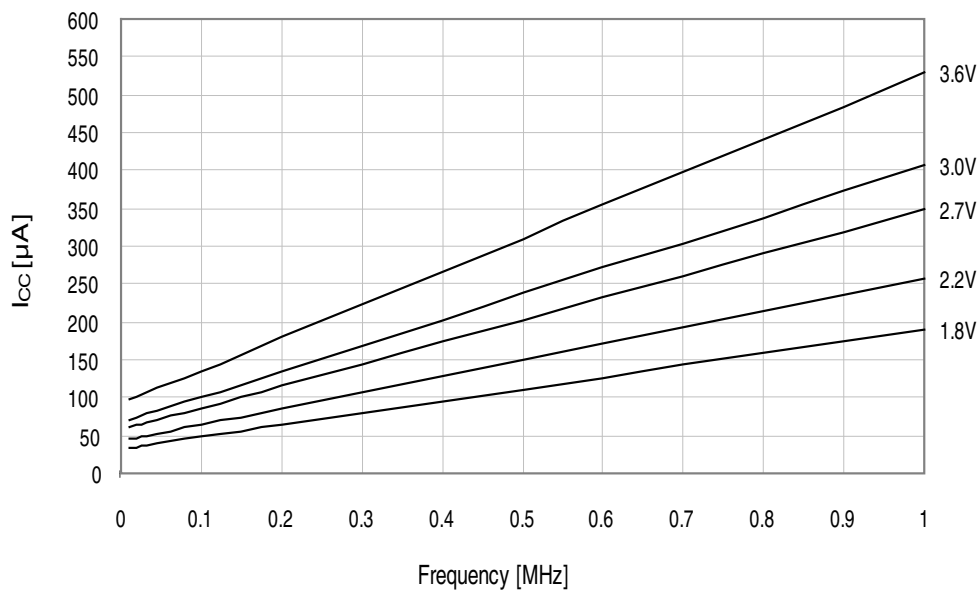


Figure 34-81. Active Supply Current vs. Frequency

$f_{\text{SYS}} = 1 - 32\text{MHz}$ external clock, $T = 25^\circ\text{C}$

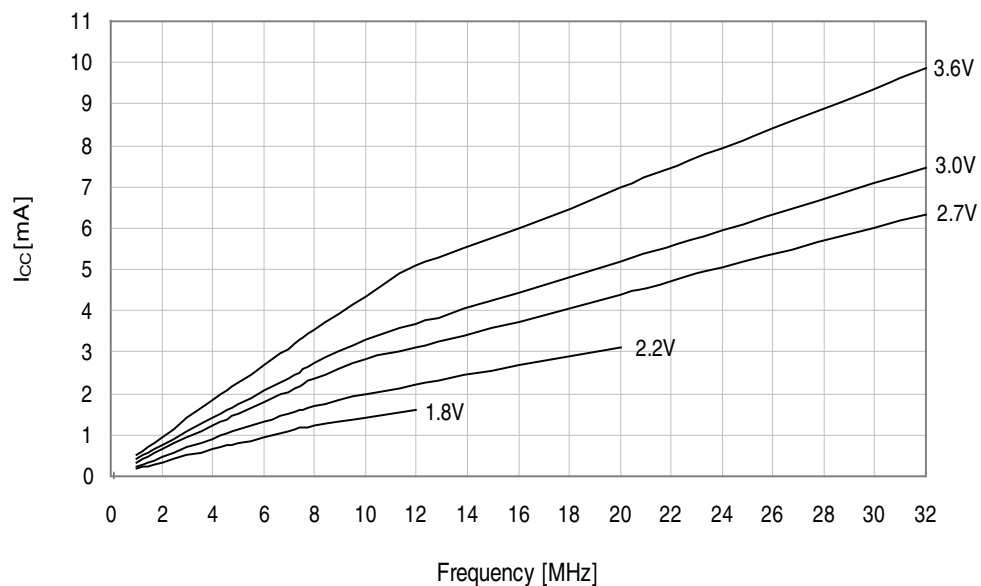
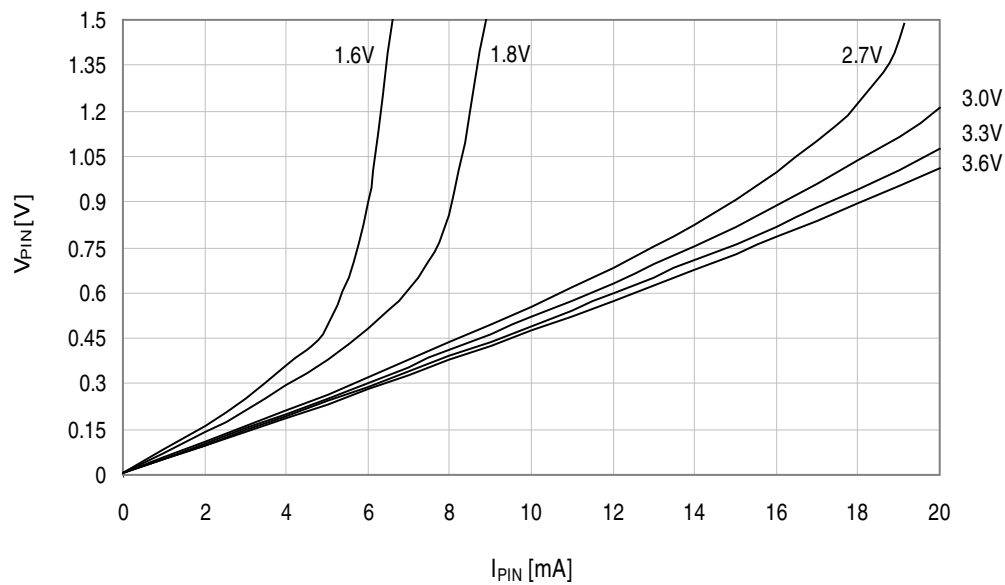


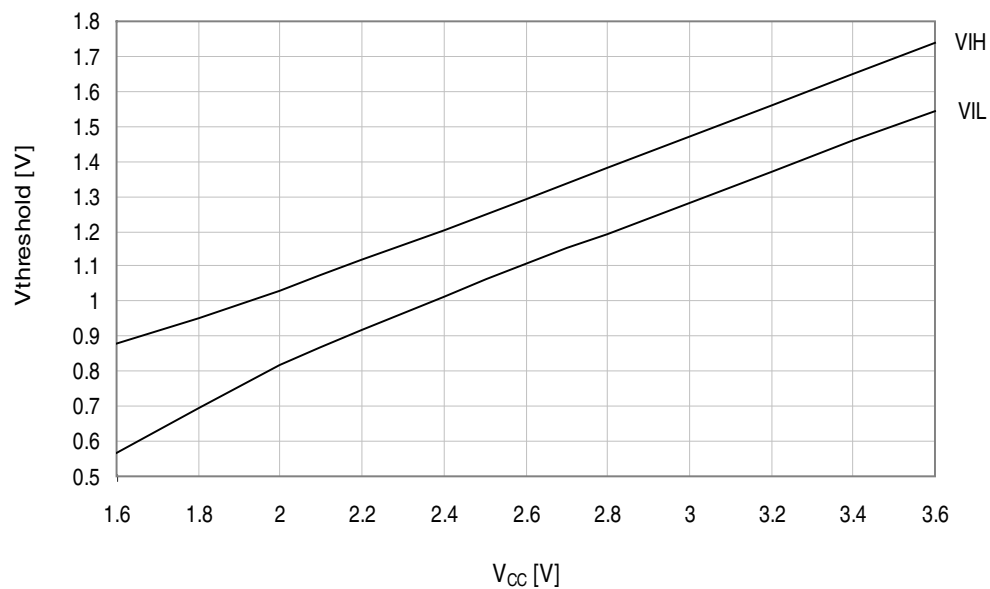
Figure 34-110. I/O Pin Output Voltage vs. Sink Current



34.2.2.3 Thresholds and Hysteresis

Figure 34-111. I/O Pin Input Threshold Voltage vs. V_{CC}

$T = 25^{\circ}\text{C}$



34.2.7 External Reset Characteristics

Figure 34-136. Minimum Reset Pin Pulse Width vs. V_{CC}

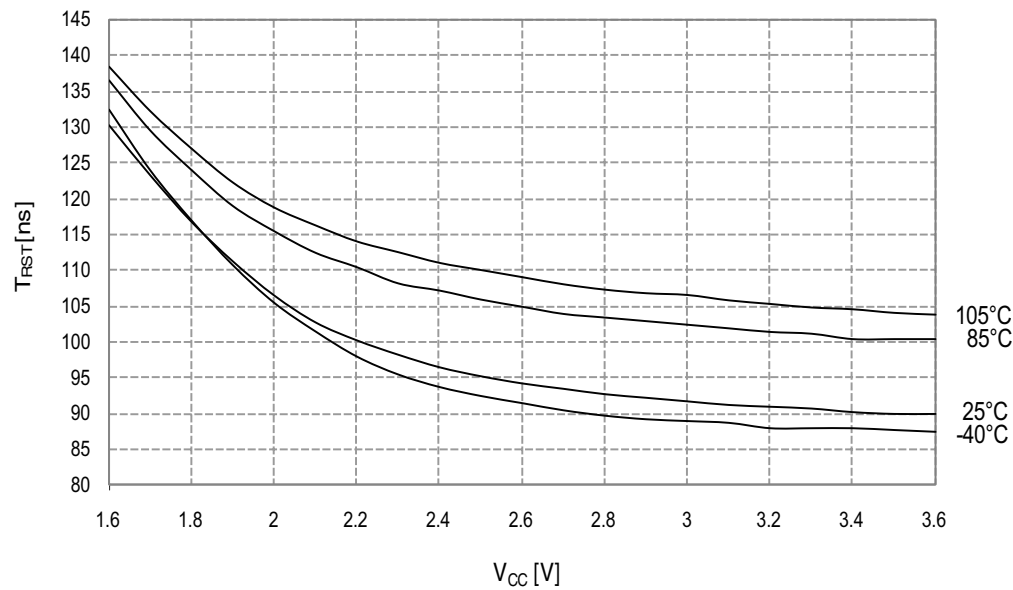
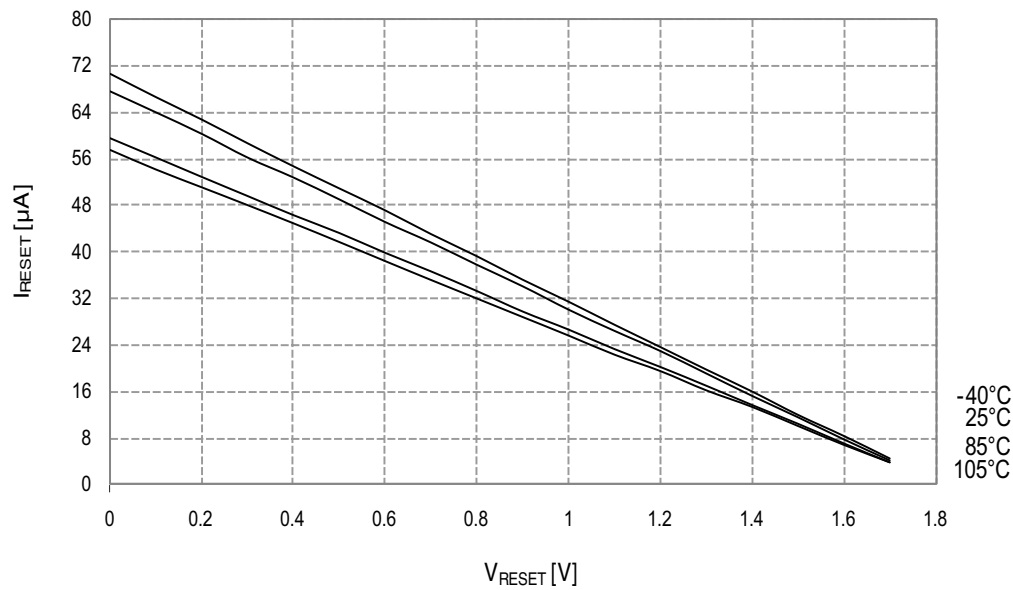


Figure 34-137. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage
 $V_{CC} = 1.8V$



34.2.9.4 32MHz Internal Oscillator

Figure 34-150. 32MHz Internal Oscillator Frequency vs. Temperature
DPLL disabled

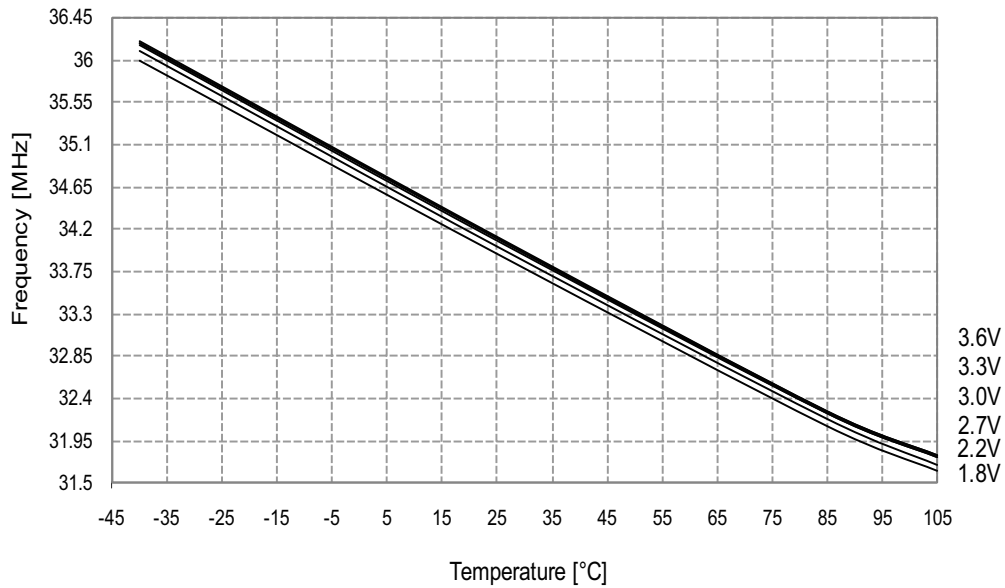


Figure 34-151. 32MHz Internal Oscillator Frequency vs. Temperature
DPLL enabled, from the 32.768kHz internal oscillator

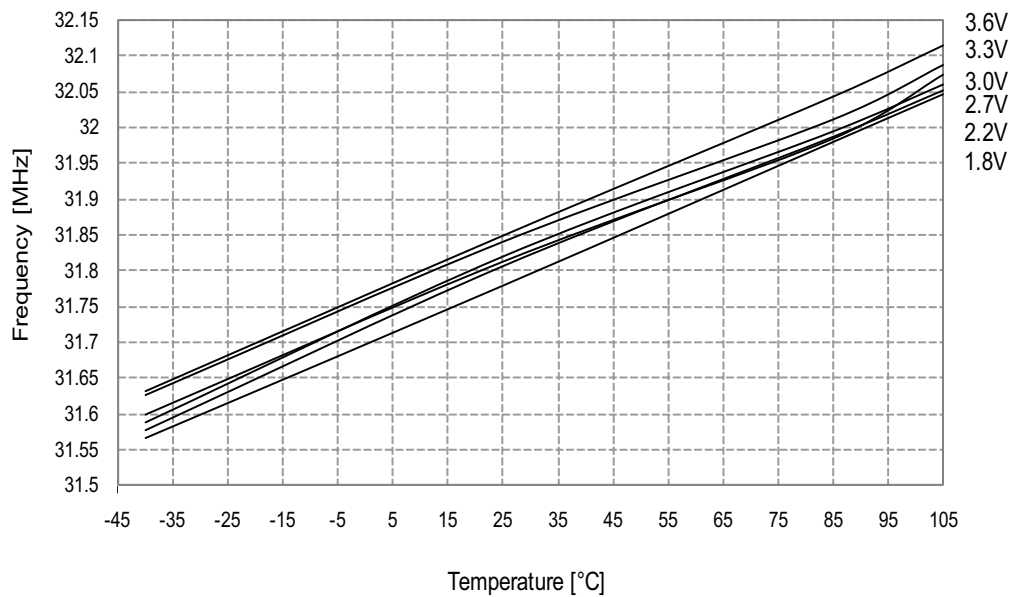


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