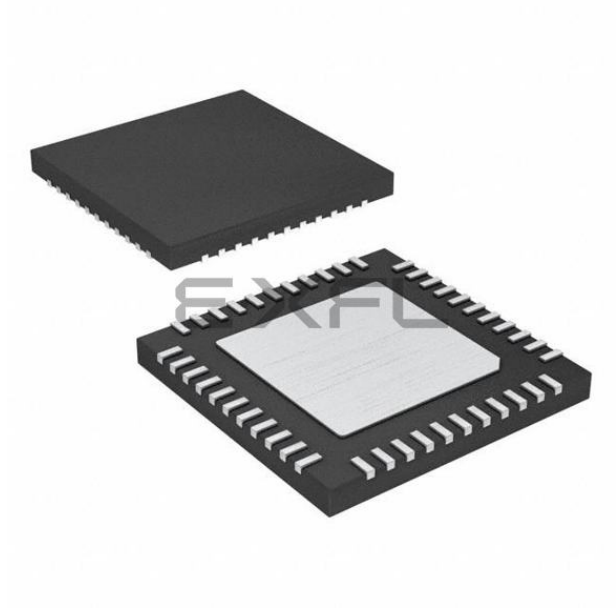

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16c4-mnr

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2. To simplify development, I/O Memory, EEPROM, and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Figure 7-2. Data Memory Map (hexadecimal address)

Byte Address	ATxmega32C4
0	I/O Registers (4K)
FFF	
1000	EEPROM (1K)
13FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte Address	ATxmega16C4
0	I/O Registers (4K)
FFF	
1000	EEPROM (1K)
13FF	
	RESERVED
2000	Internal SRAM (2K)
27FF	

7.6 EEPROM

All devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

7.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules is shown in the “Peripheral Module Address Map” on page 55.

7.7.1 General Purpose I/O Registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

7.8 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.9 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

13. Interrupts and Programmable Multilevel Interrupt Controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

13.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA C4 devices are shown in Table 13-1 on page 28. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA C manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1 on page 28. The program address is the word address.

21. TWI – Two-Wire Interface

21.1 Features

- Two Identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips I^2C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

21.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I^2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V_{CC} voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

32.2 PW

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Notes :

02/17/2012

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat	ZCP	PW	H

33. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

33.1 Atmel ATxmega16C4

33.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 33-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 33-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a GND pin				200	
V_{PIN}	Pin voltage with respect to GND and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

33.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 33-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 33-2. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 33-3. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

Table 33-5. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.8		µA
	32.768kHz int. oscillator				29		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			410		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			290		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				175		
	Temperature sensor				170		
	ADC	16ksps V_{REF} = Ext ref			1.2		mA
			CURRLIMIT = LOW		1.0		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext ref	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext ref			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			11		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.1.13 Clock and Oscillator Characteristics

33.1.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 33-19. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

33.1.13.2Calibrated 2MHz RC Internal Oscillator Characteristics

Table 33-20. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

33.1.13.3Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 33-21. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

33.1.13.432kHz Internal ULP Oscillator Characteristics

Table 33-22. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

33.2 Atmel ATxmega32C4

33.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 33-30 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 33-30. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a GND pin				200	
V_{PIN}	Pin voltage with respect to GND and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

33.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 33-31 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 33-31. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 33-32. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 33-8 on page 85 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Table 33-34. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.8		µA
	32.768kHz int. oscillator				29		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			410		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			290		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				175		
	Temperature sensor				170		
	ADC	16ksps V_{REF} = Ext. ref.			1.2		mA
			CURRLIMIT = LOW		1.0		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			11		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

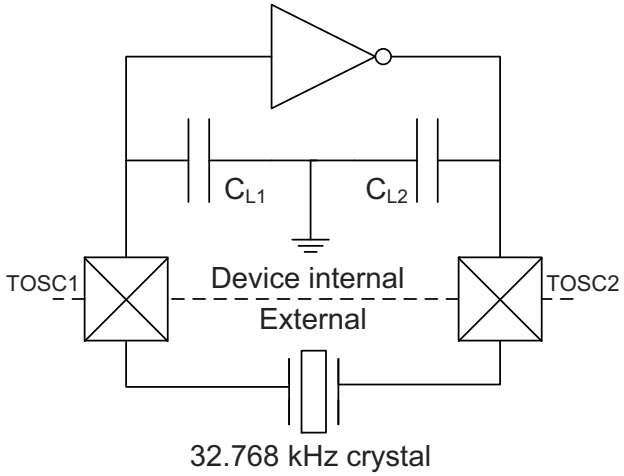
33.2.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 33-56. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 33-11 for definition.

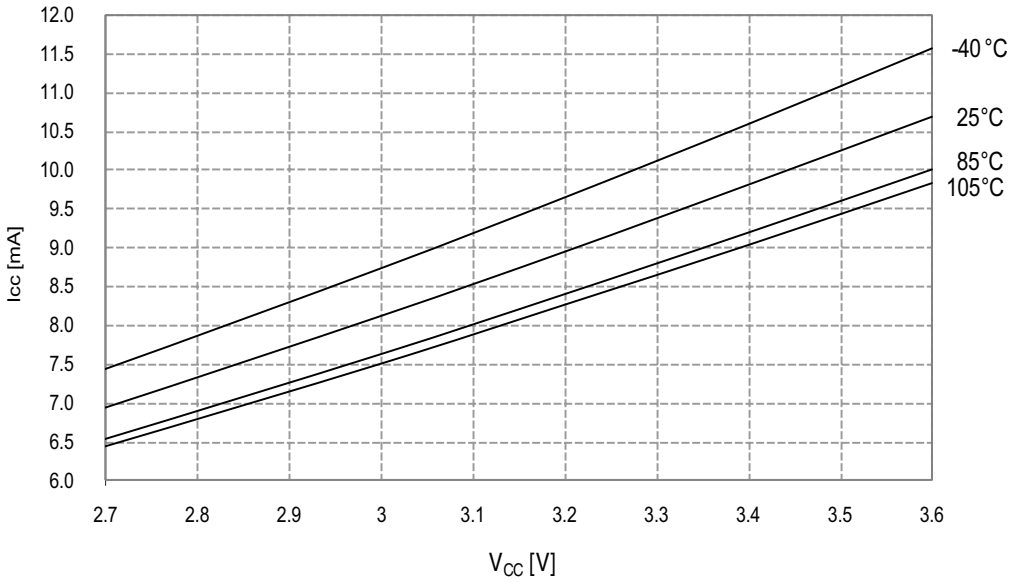
Figure 33-11.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

Figure 34-7. Active Mode Supply Current vs. V_{CC}

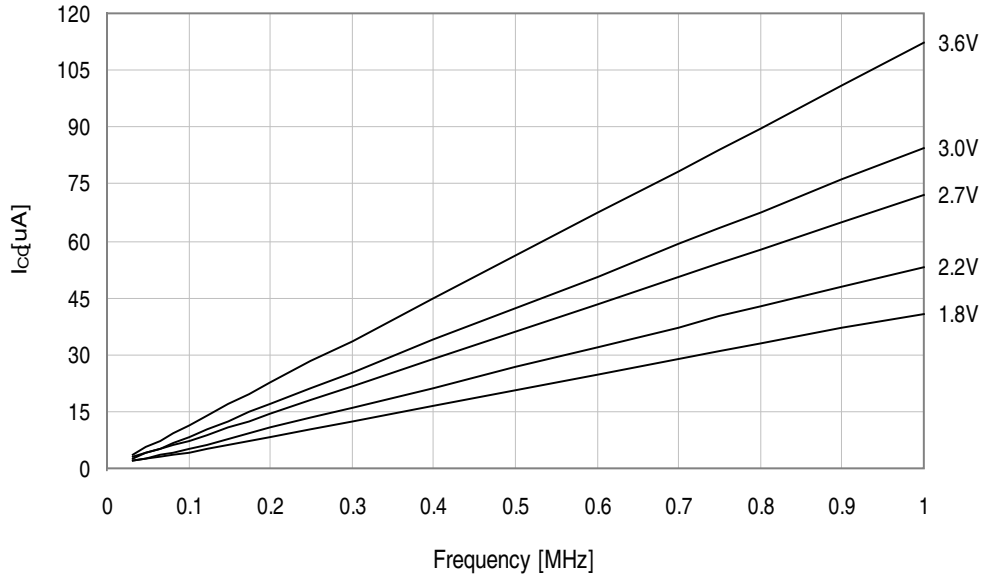
f_{SYS} = 32MHz internal oscillator



34.1.1.2 Idle Mode Supply Current

Figure 34-8. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C



34.1.1.3 Power-down Mode Supply Current

Figure 34-15.Power-down Mode Supply Current vs. V_{CC}

All functions disabled

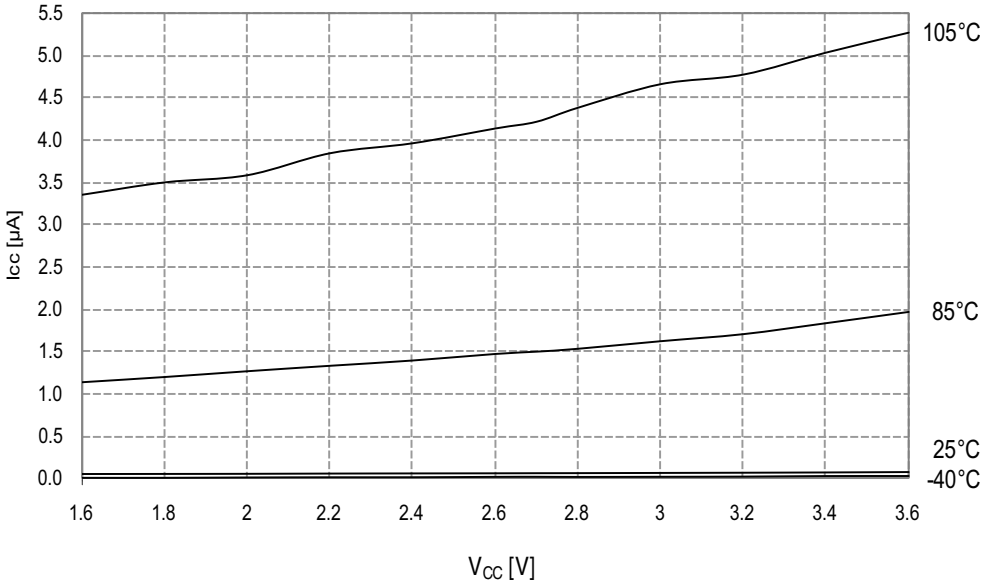


Figure 34-16.Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

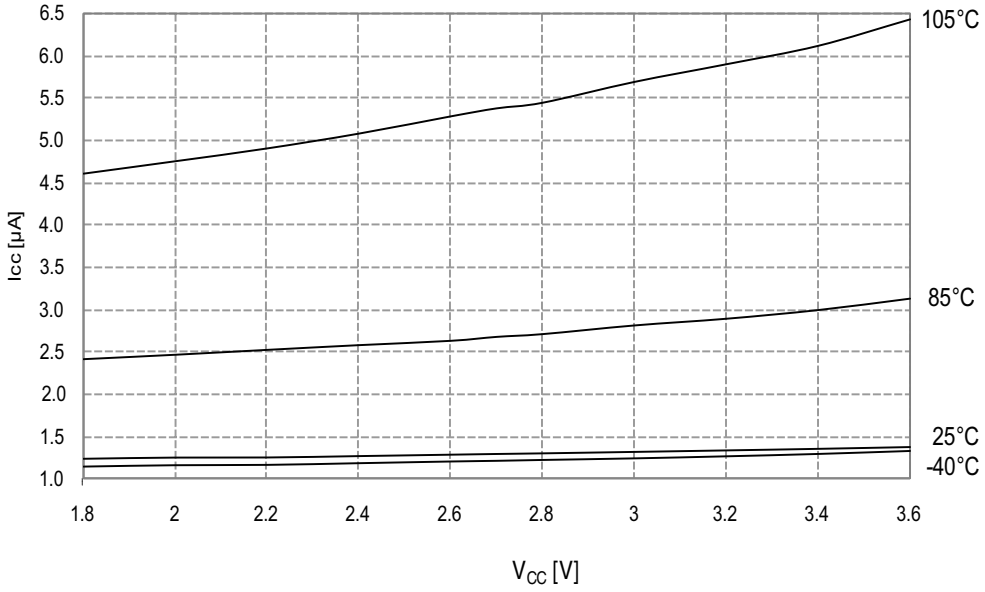


Figure 34-33. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

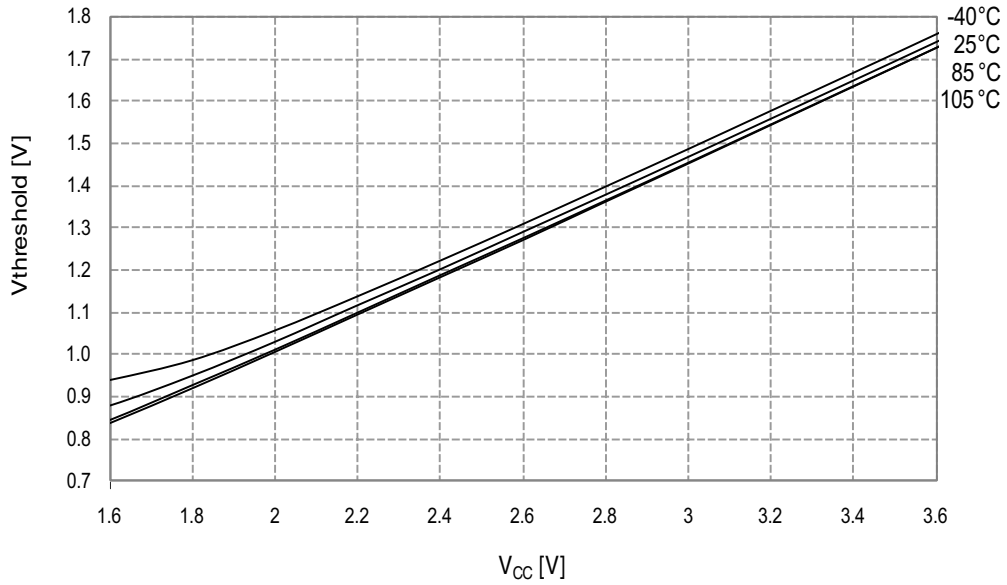
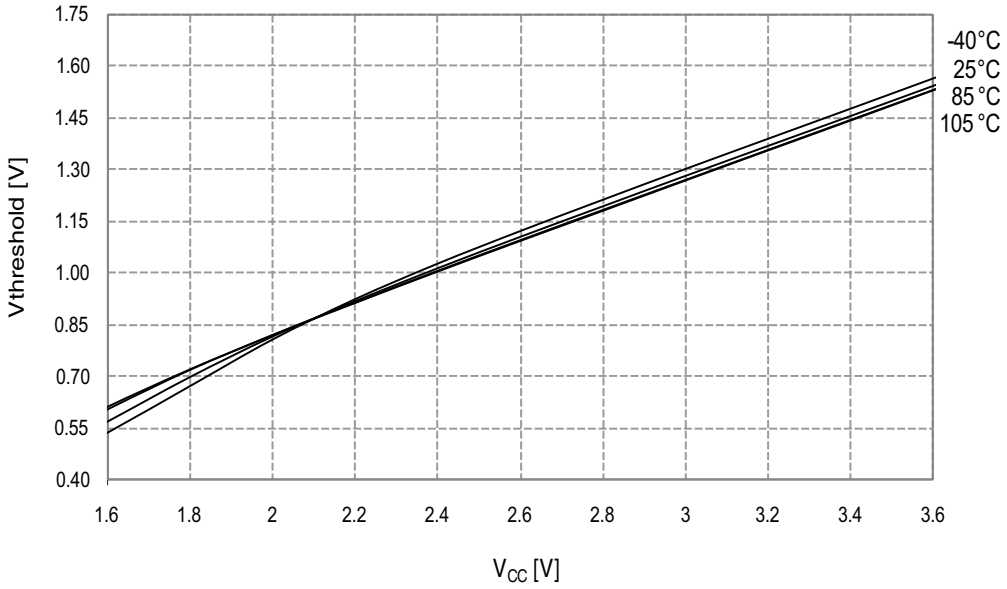


Figure 34-34. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"



34.1.8 Power-on Reset Characteristics

Figure 34-63. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode

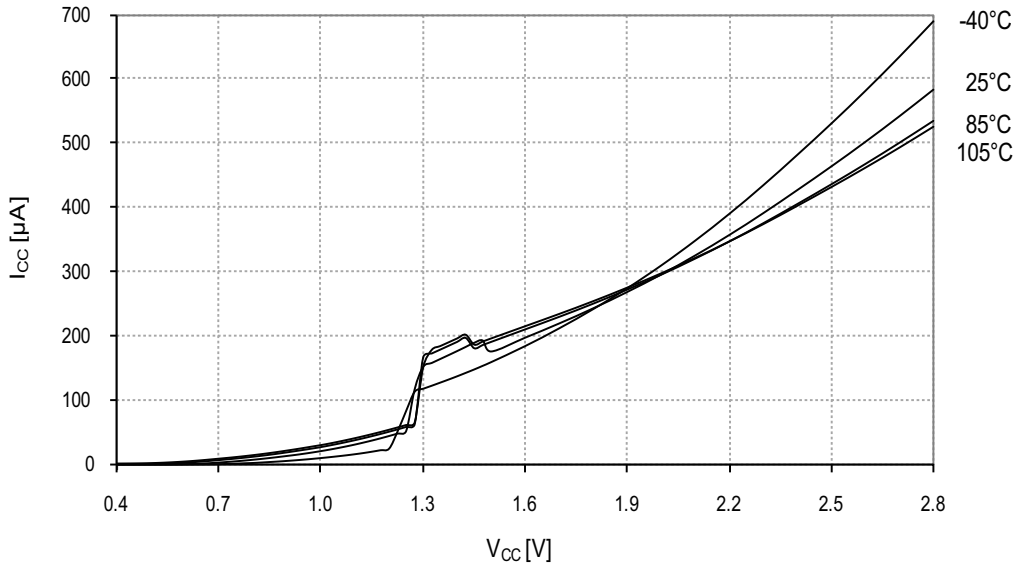


Figure 34-64. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode

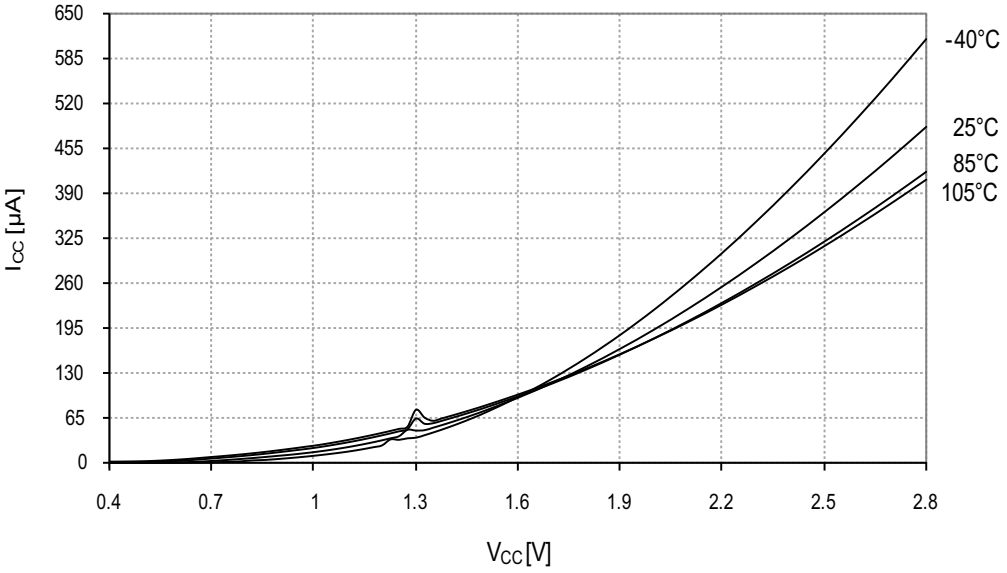


Figure 34-75. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

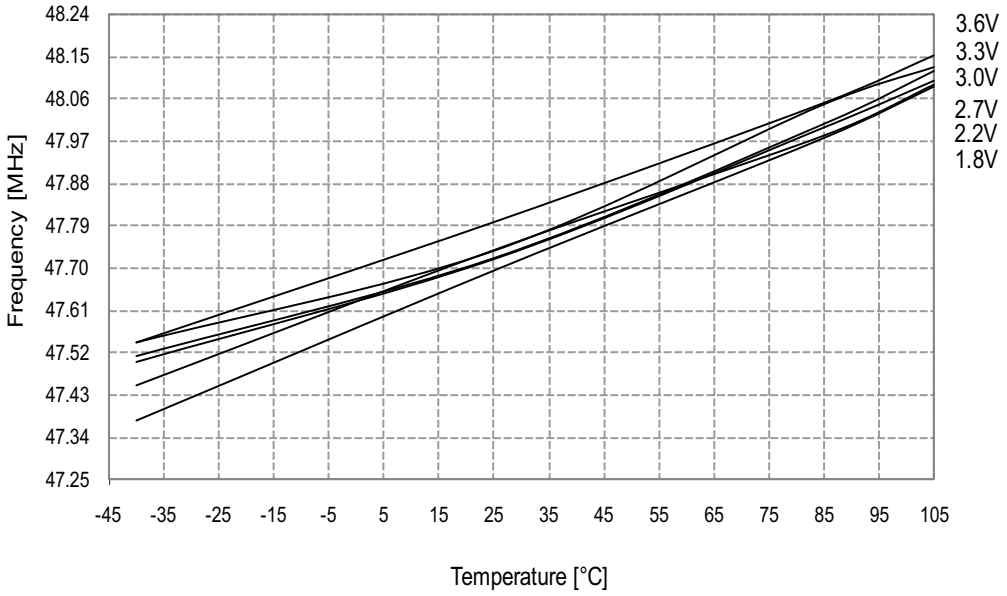


Figure 34-76. 48MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V

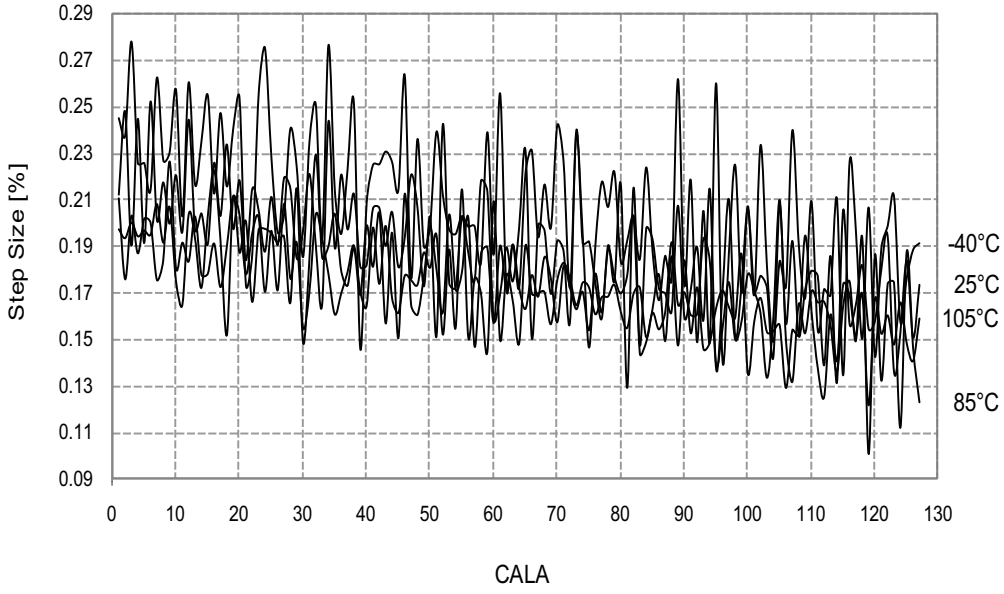


Figure 34-108. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

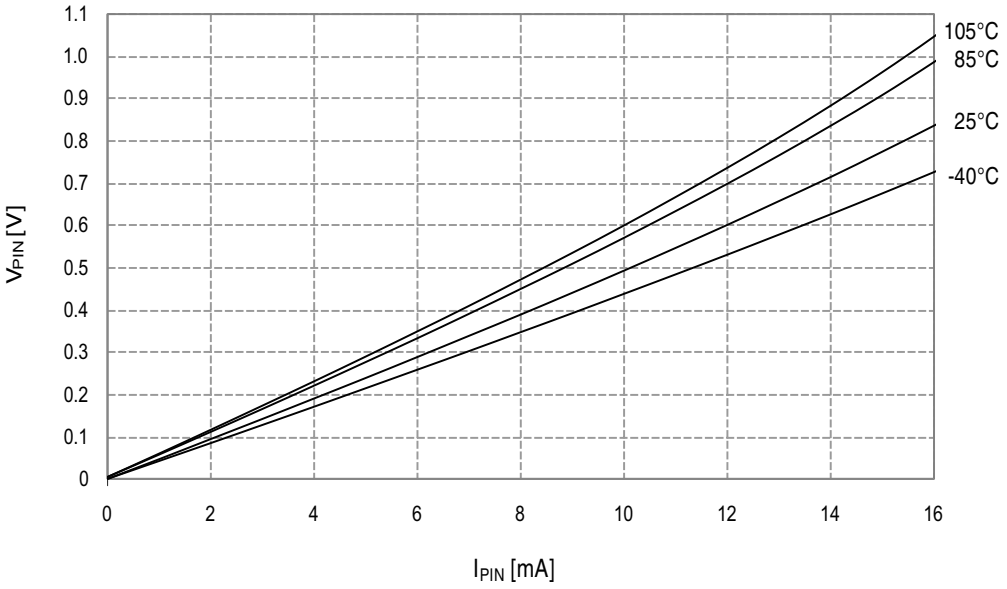


Figure 34-109. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

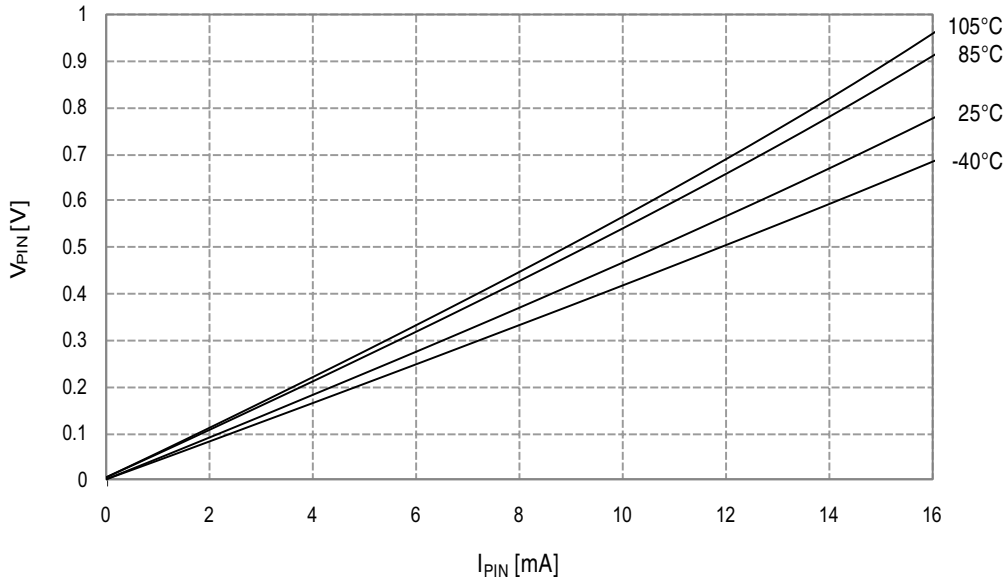


Figure 34-120. DNL Error vs. Input Code

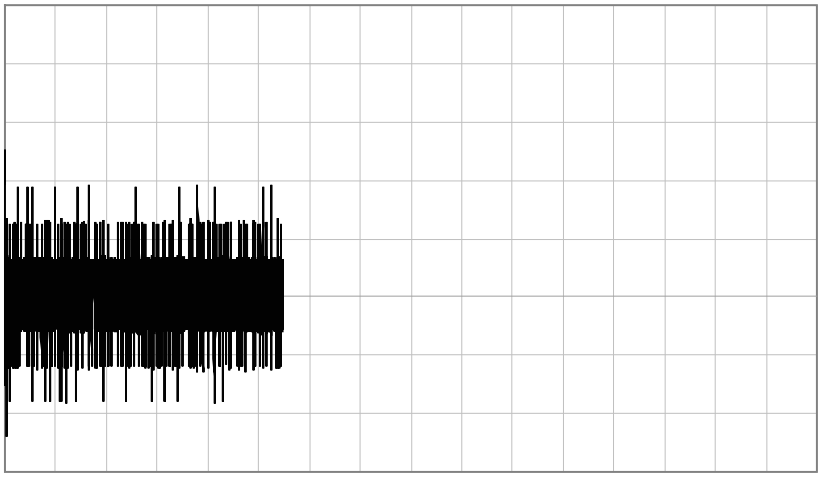


Figure 34-121. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

34.2.6 BOD Characteristics

Figure 34-134. BOD Thresholds vs. Temperature

BOD level = 1.6V

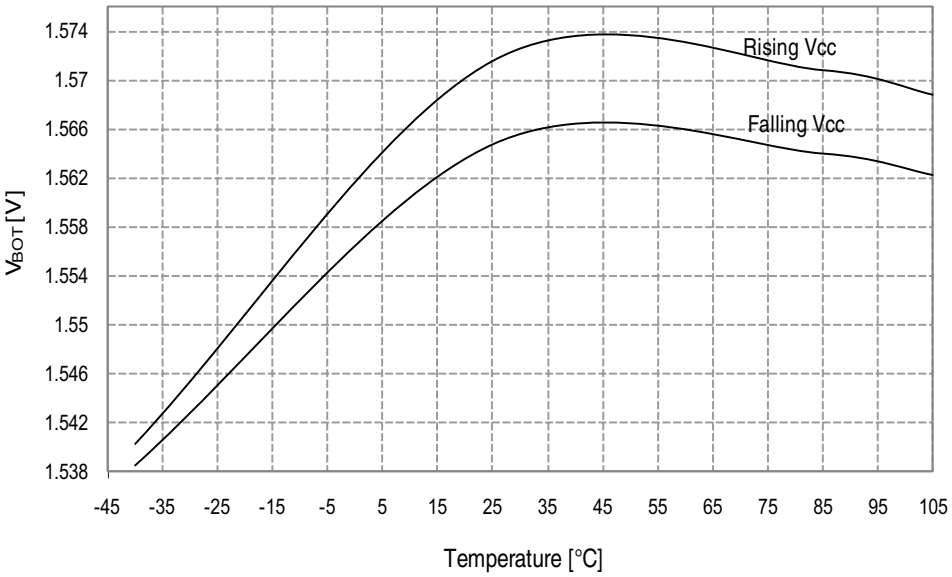
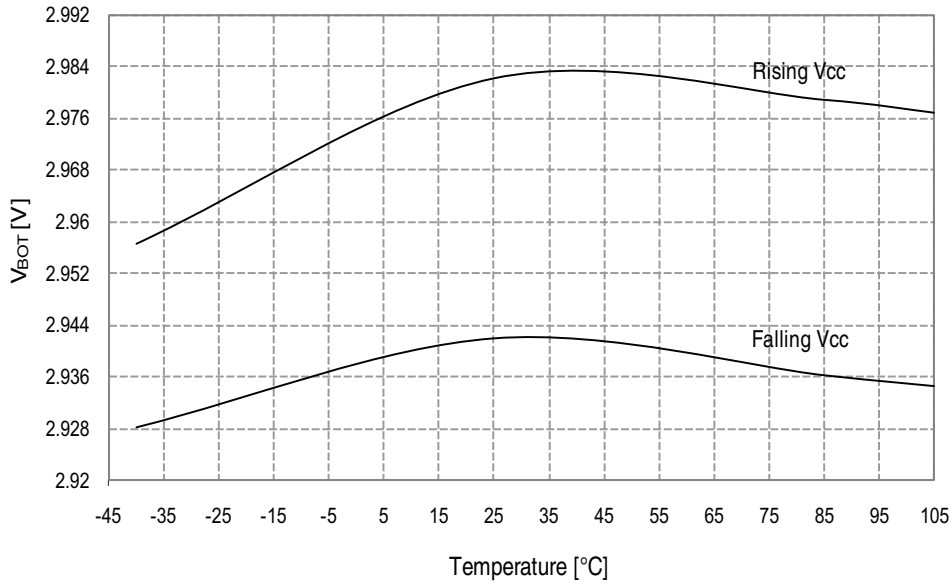


Figure 34-135. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.2.7 External Reset Characteristics

Figure 34-136. Minimum Reset Pin Pulse Width vs. V_{CC}

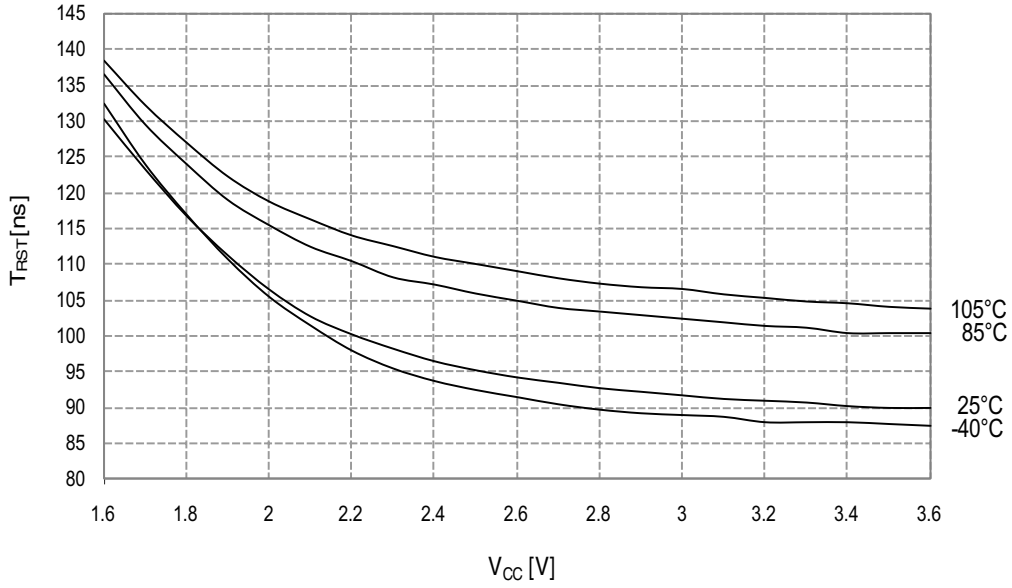
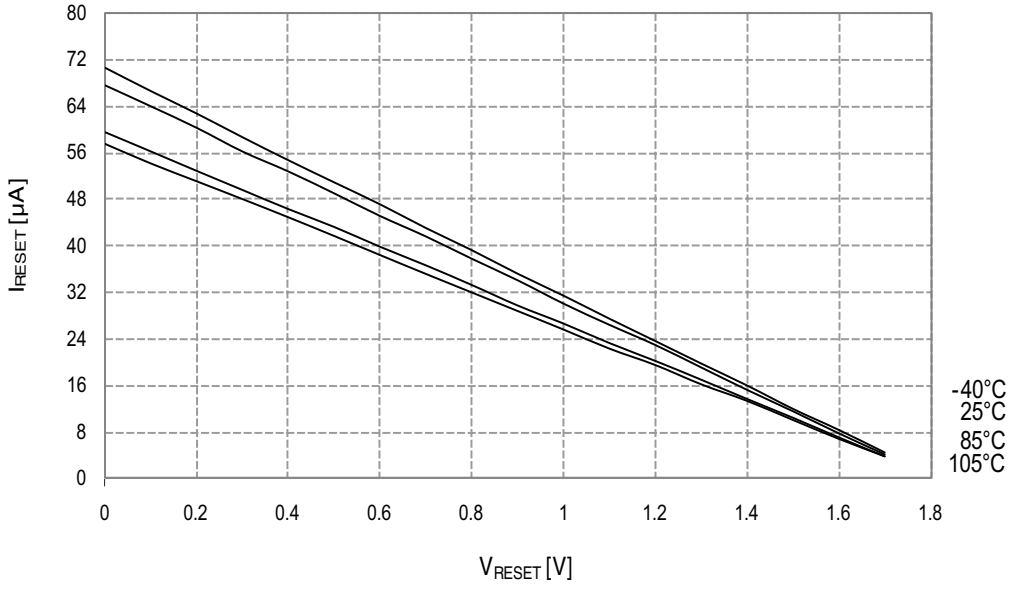


Figure 34-137. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V



34.2.9.4 32MHz Internal Oscillator

Figure 34-150. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

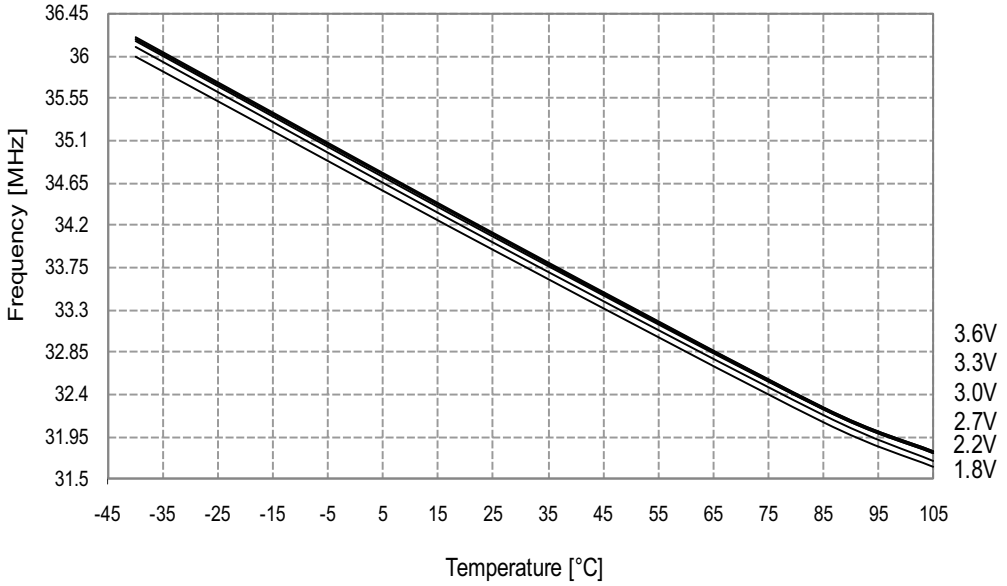


Figure 34-151. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator