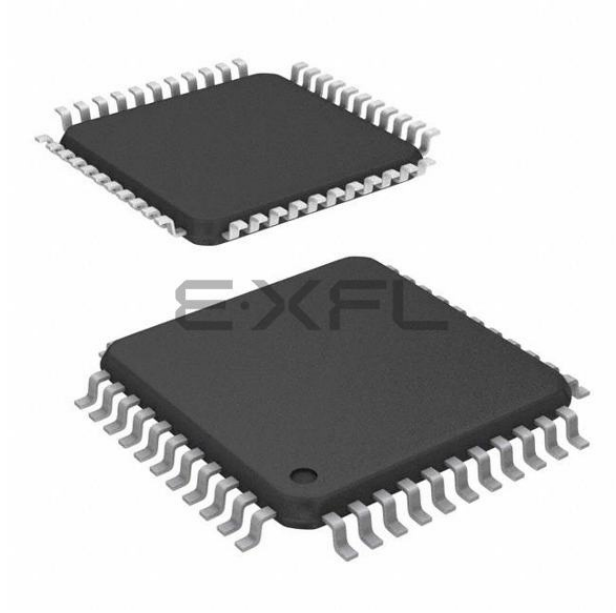

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c4-an

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

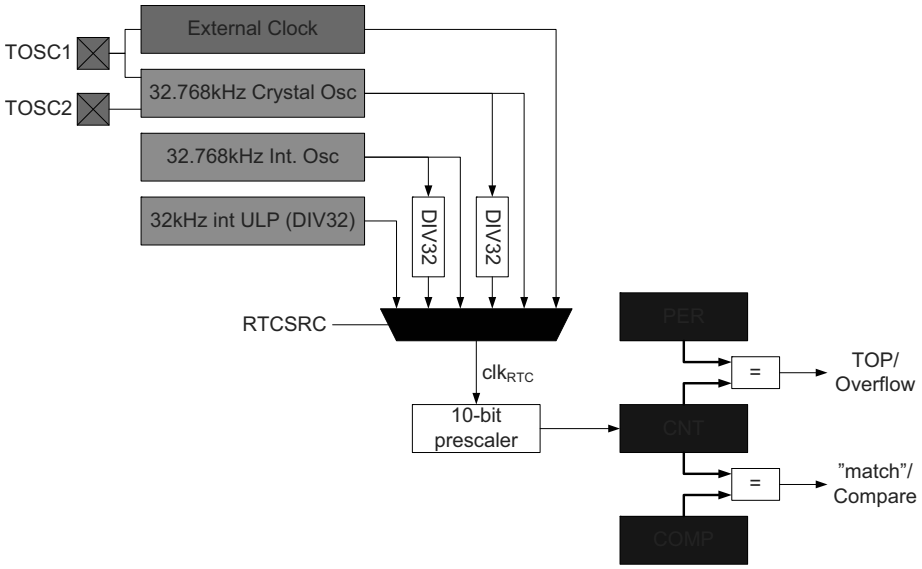
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview

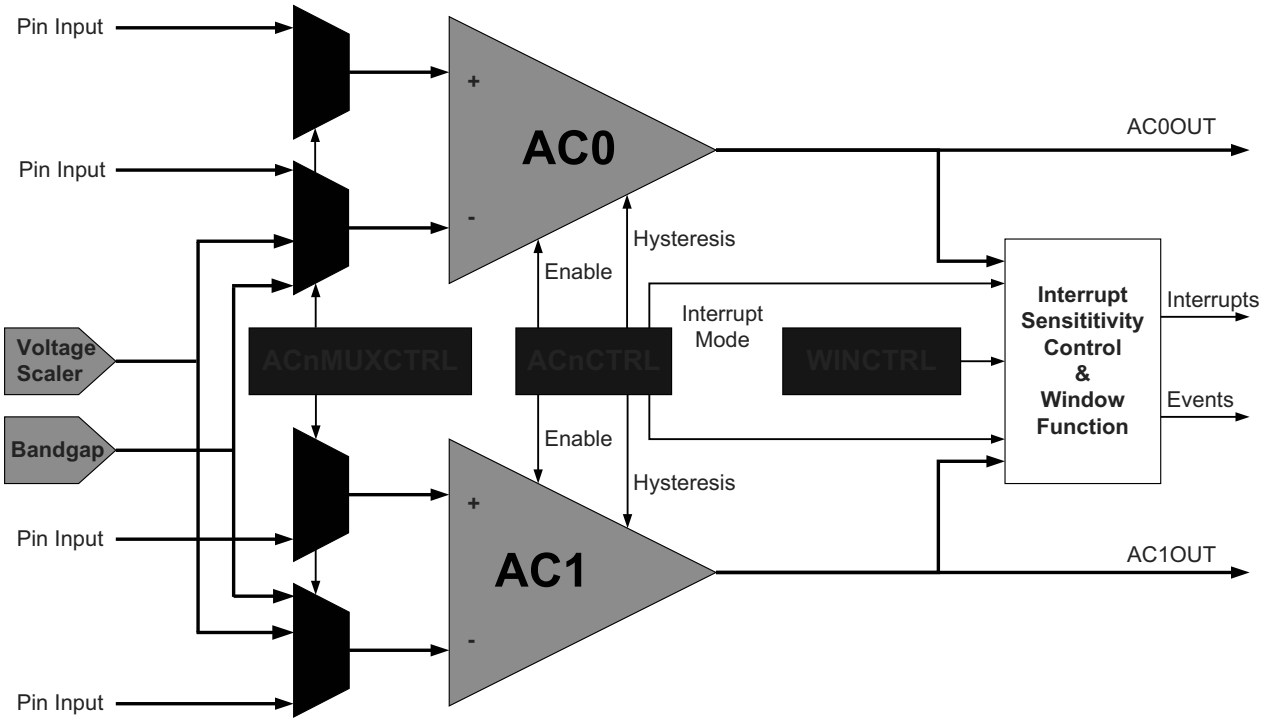


Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

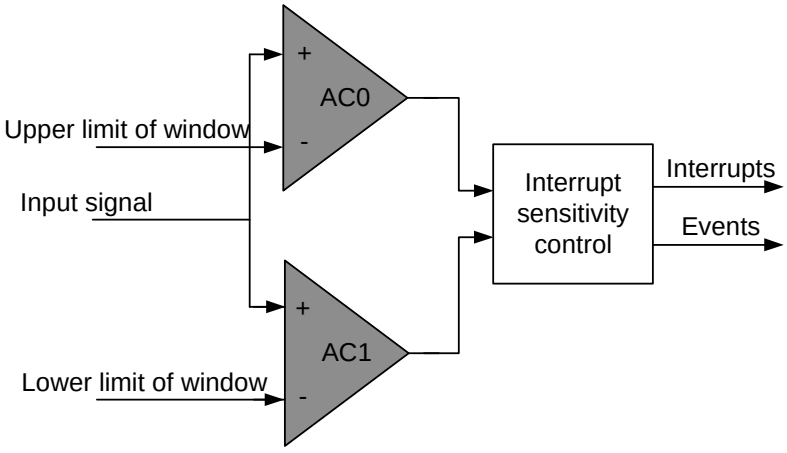
PORTD has one USB. Notation of this is USB.

Figure 27-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog Comparator Window Function



Mnemonics	Operands	Description	Operation	Flags	#Clocks
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1(1)
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2(1)
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	Temp ← Rd, Rd ← (Z), (Z) ← ($FFh – Rd) ● (Z)	None	2
LAT	Z, Rd	Load and Toggle RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp ⊕ (Z)	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1

33.2.3 Current Consumption

Table 33-33. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		200		
			V_{CC} = 3.0V		410		
		2MHz, Ext. Clk	V_{CC} = 1.8V		350	600	
			V_{CC} = 3.0V		0.75	1.4	mA
		32MHz, Ext. Clk			7.5	12	
	Idle power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.0		µA
			V_{CC} = 3.0V		2.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		42		
			V_{CC} = 3.0V		85		
		2MHz, Ext. Clk	V_{CC} = 1.8V		85	225	
			V_{CC} = 3.0V		170	350	
		32MHz, Ext. Clk			2.7	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.0	4.5	
		T = 105°C			0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	10	
	Power-save power consumption(2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.5		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

33.2.13 Clock and Oscillator Characteristics

33.2.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 33-48. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

33.2.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 33-49. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

33.2.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 33-50. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

33.2.13.4 32kHz Internal ULP Oscillator Characteristics

Table 33-51. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

34. Typical Characteristics

34.1 Atmel ATxmega16C4

34.1.1 Current Consumption

34.1.1.1 Active Mode Supply Current

Figure 34-1. Active Supply Current vs. Frequency
f_{SYS} = 0 - 1MHz external clock, T = 25°C

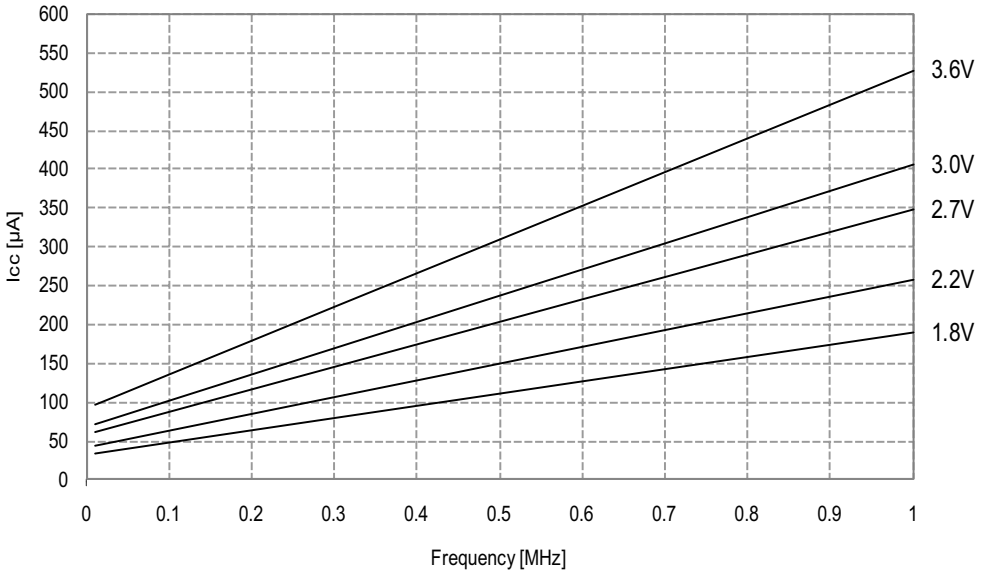


Figure 34-2. Active Supply Current vs. Frequency
f_{SYS} = 1 - 32MHz external clock, T = 25°C

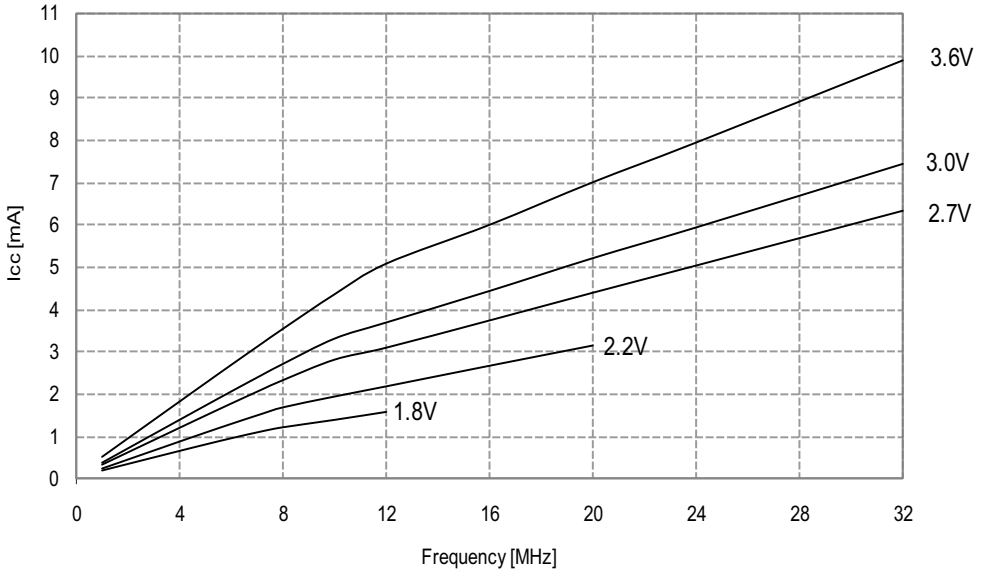


Figure 34-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

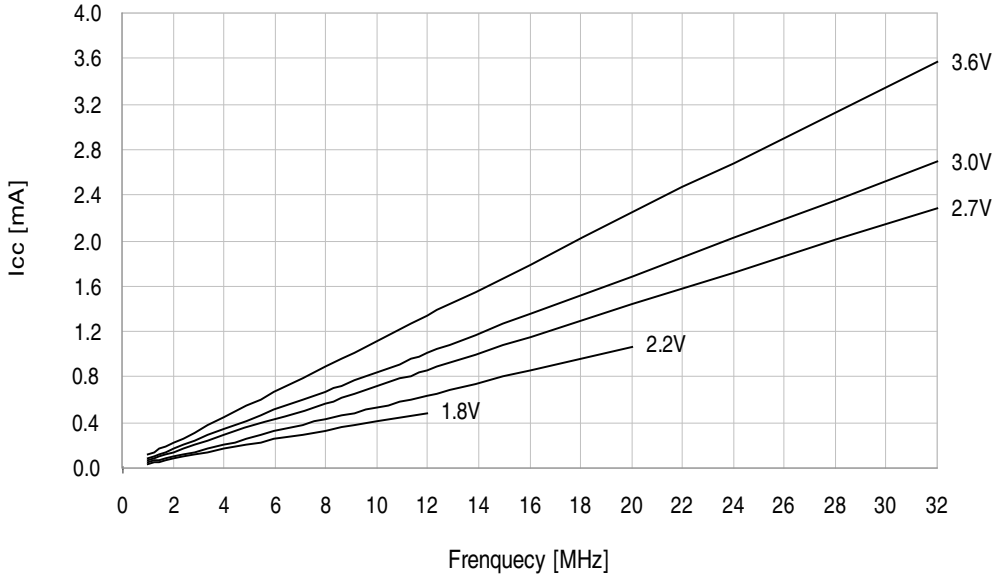


Figure 34-10.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

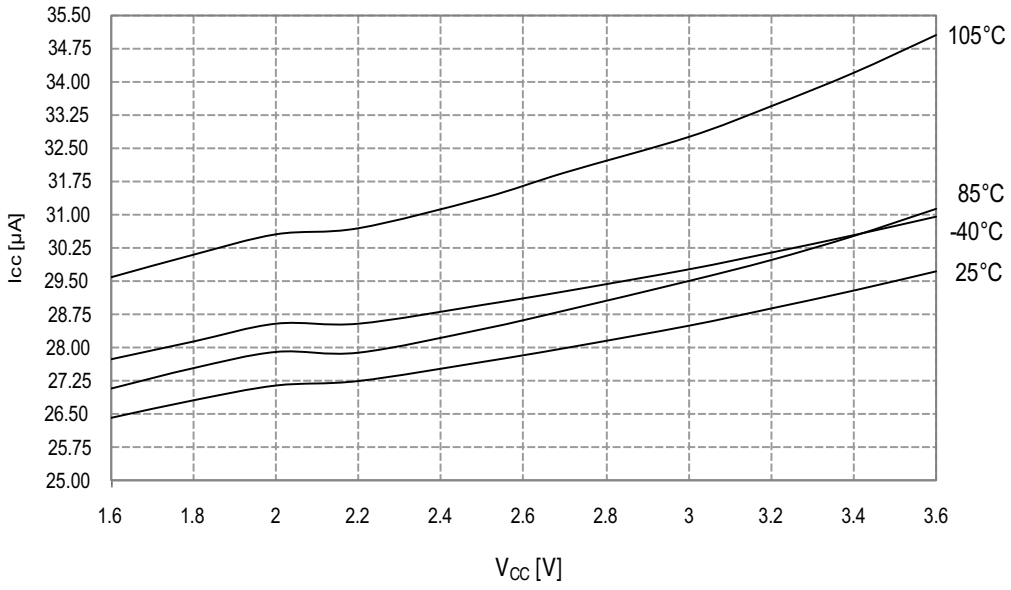


Figure 34-11.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = MHz external clock

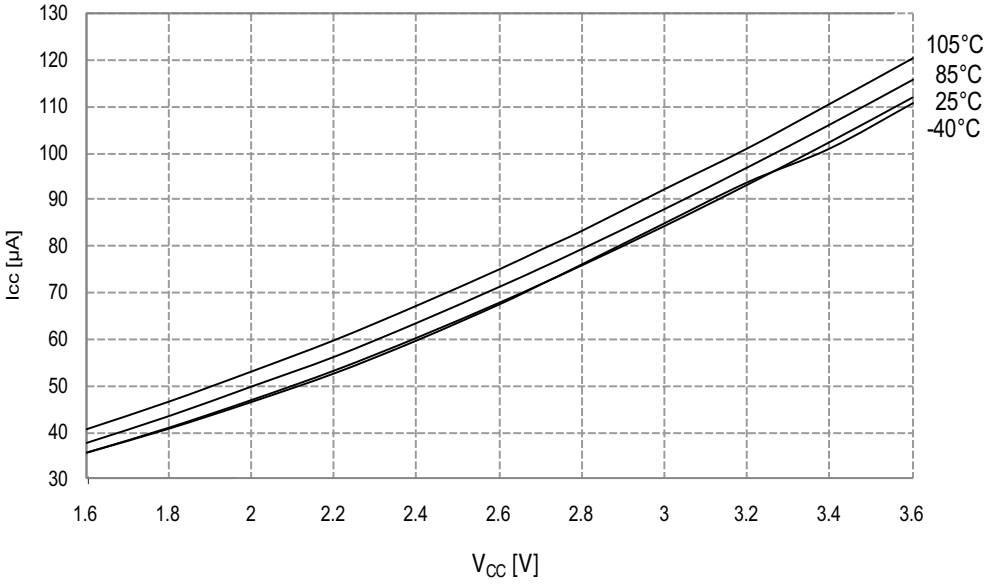


Figure 34-12.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

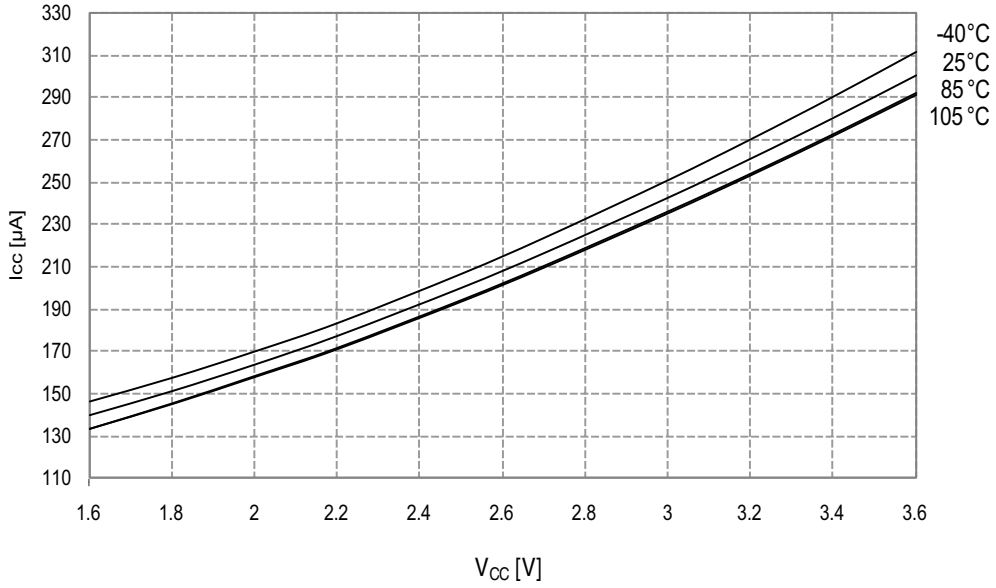


Figure 34-25. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

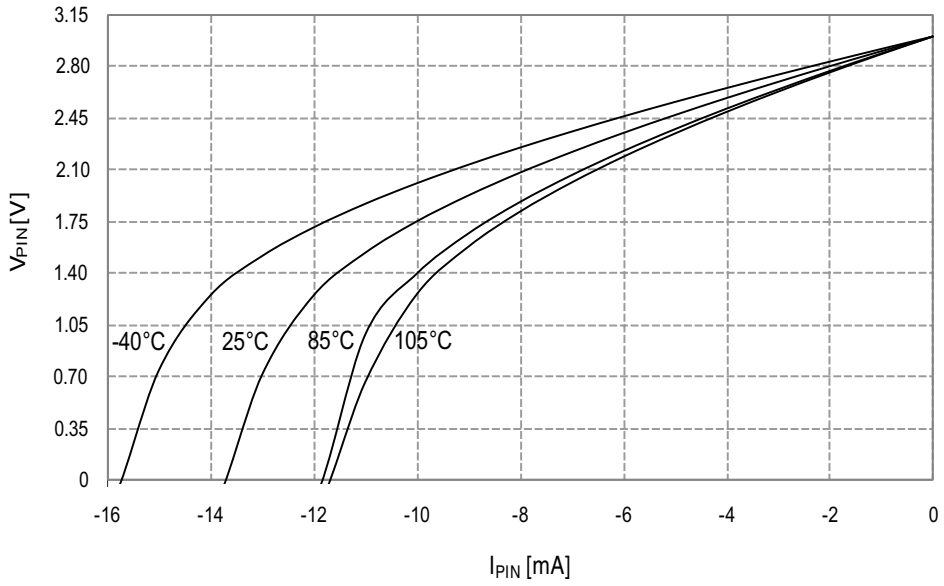


Figure 34-26. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

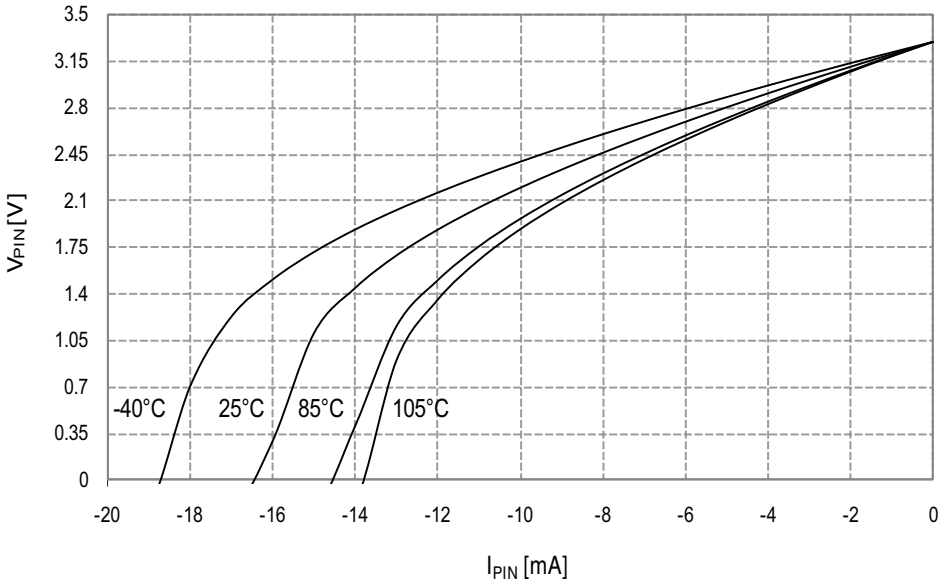


Figure 34-43. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

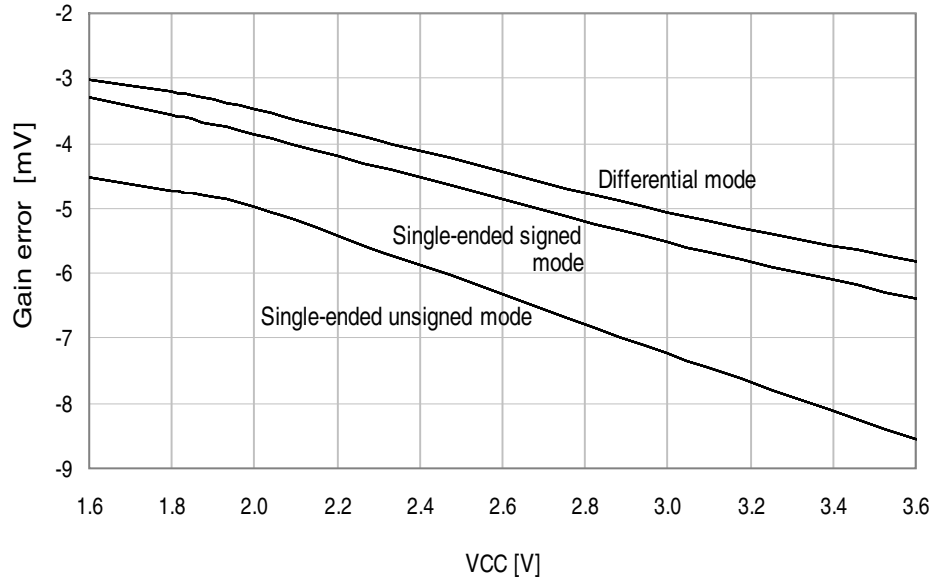
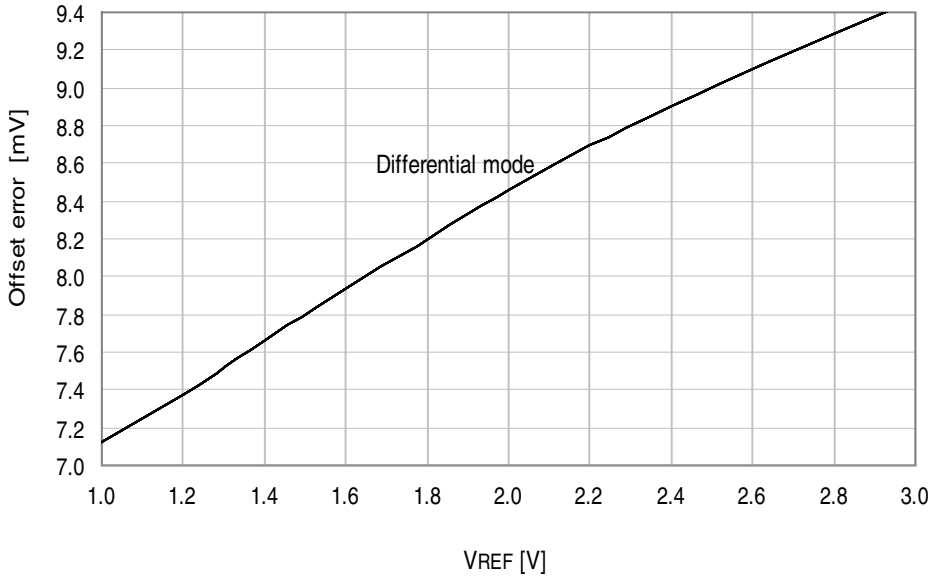


Figure 34-44. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps



34.1.7 External Reset Characteristics

Figure 34-57. Minimum Reset Pin Pulse Width vs. V_{CC}

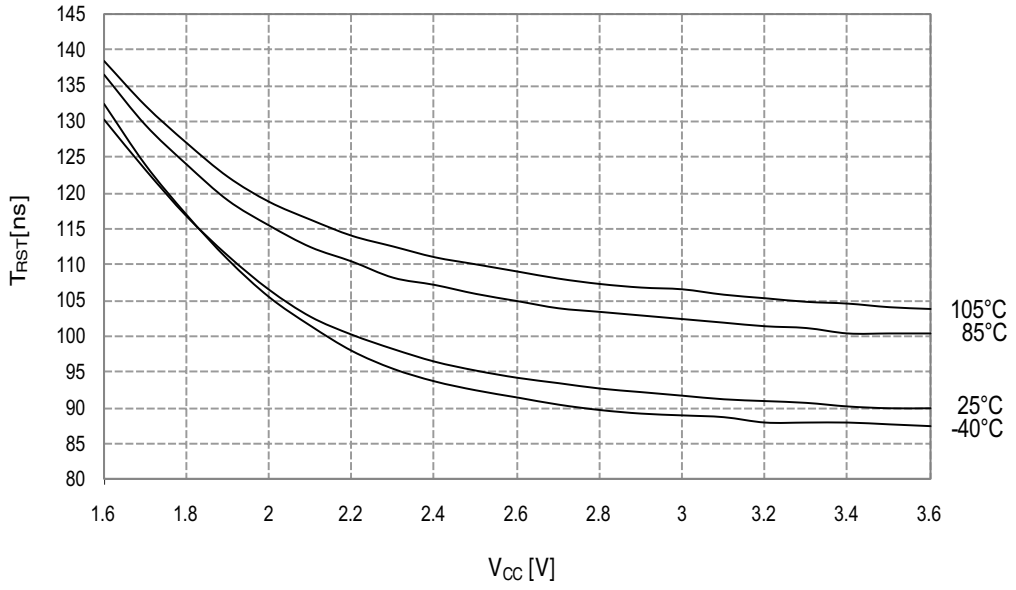
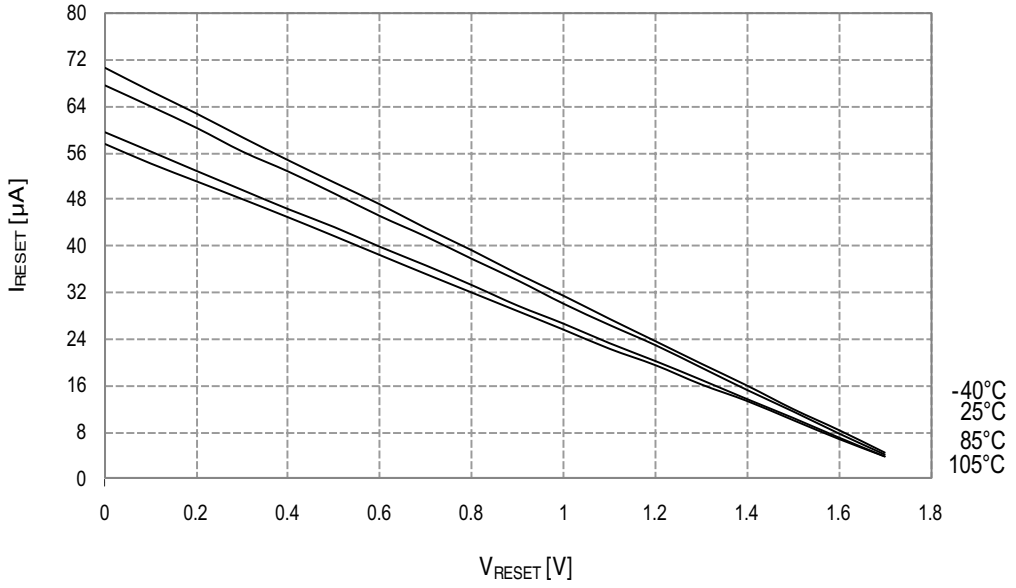


Figure 34-58. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

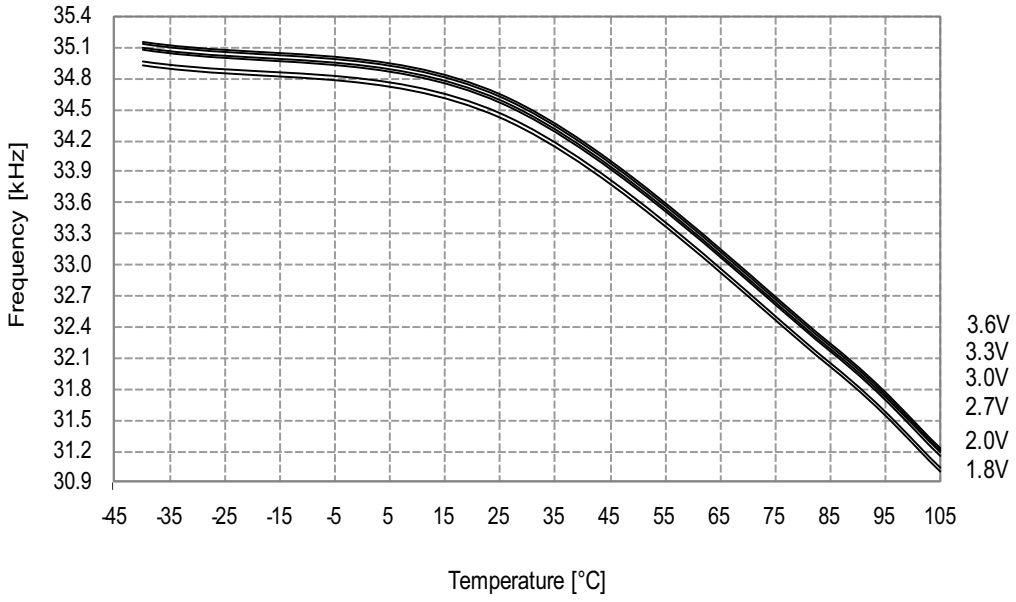
V_{CC} = 1.8V



34.1.9 Oscillator Characteristics

34.1.9.1 Ultra Low-Power Internal Oscillator

Figure 34-65.Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.1.9.2 32.768kHz Internal Oscillator

Figure 34-66. 32.768kHz Internal Oscillator Frequency vs. Temperature

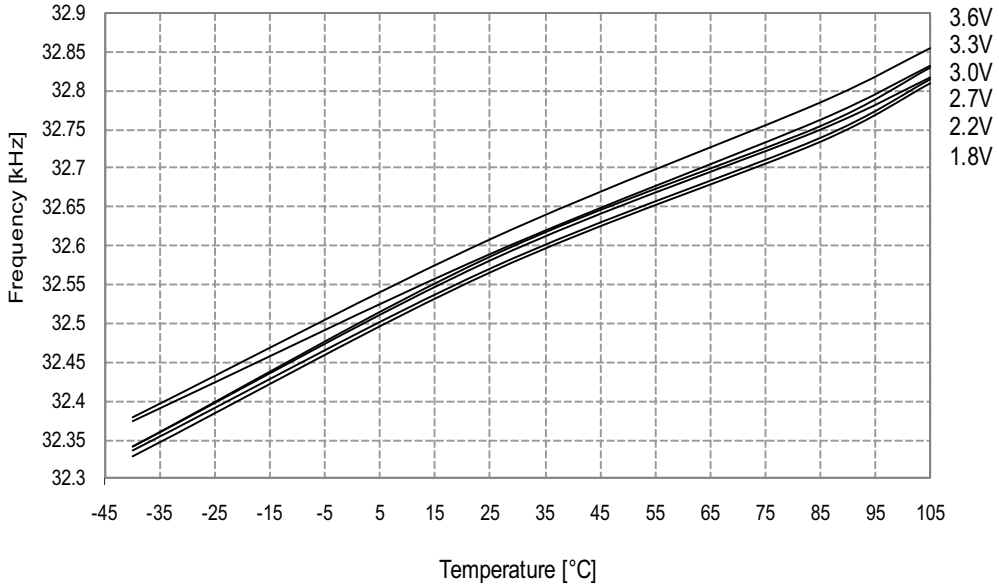


Figure 34-88. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

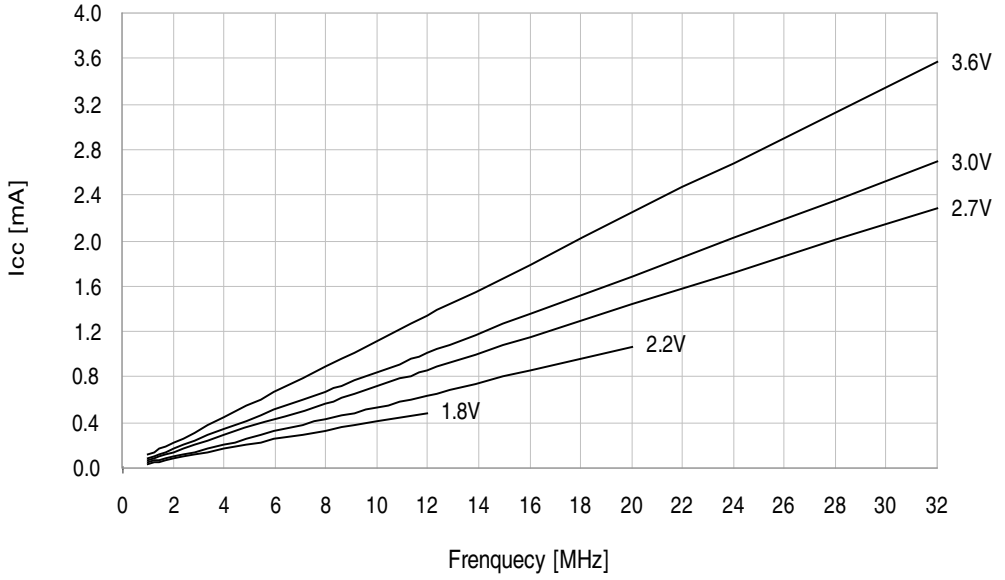


Figure 34-89. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

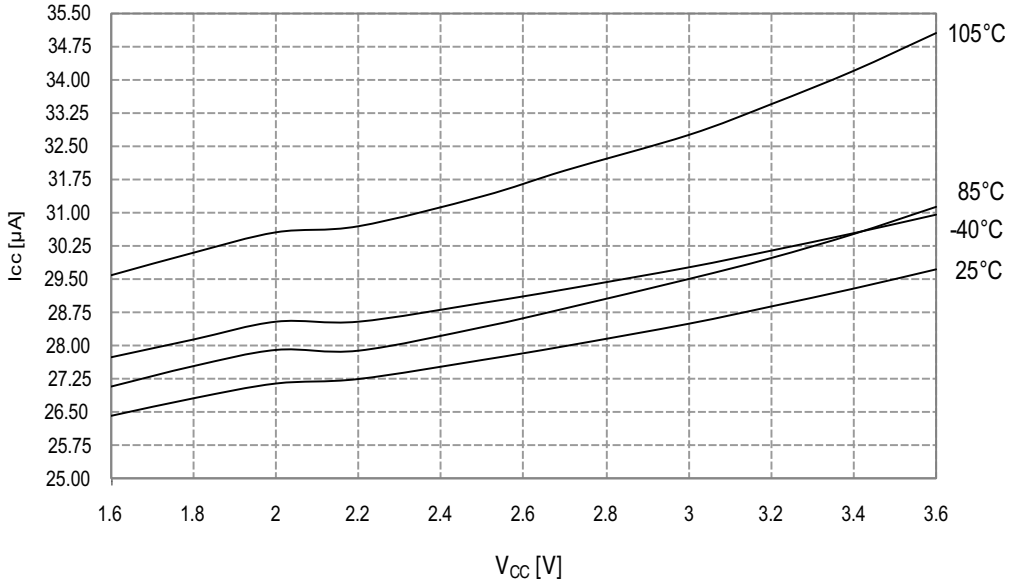


Figure 34-92. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

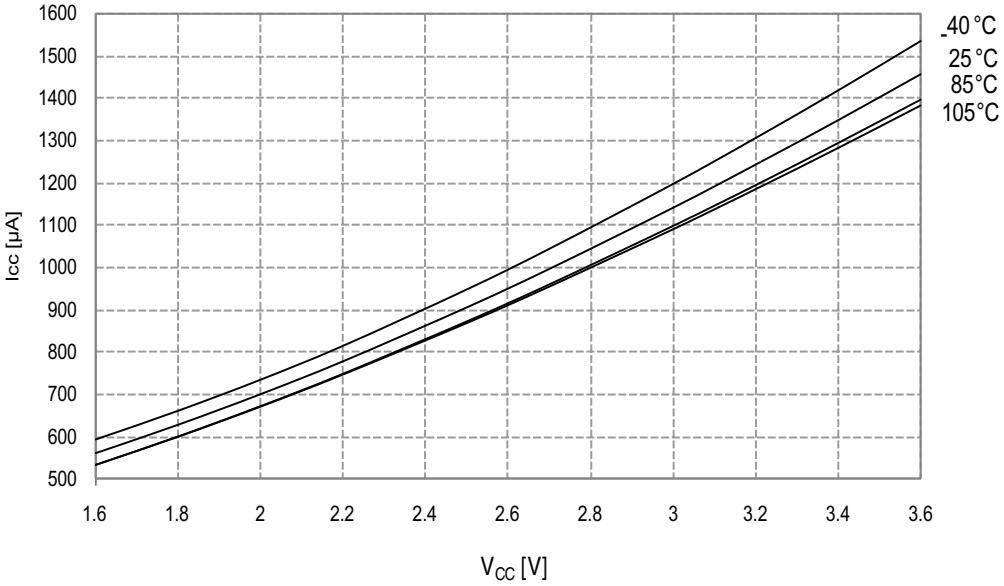
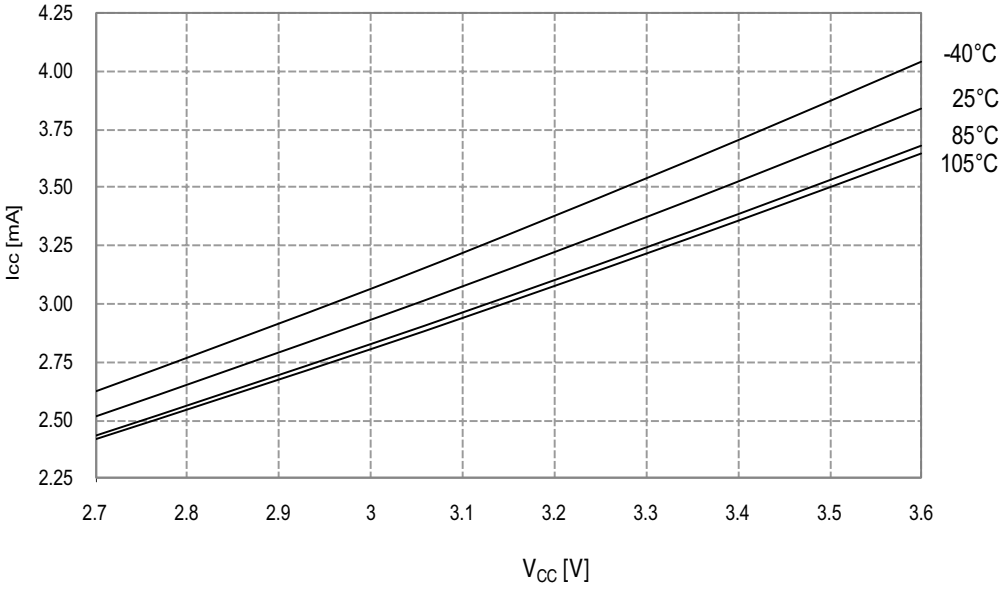


Figure 34-93. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



34.2.2 I/O Pin Characteristics

34.2.2.1 Pull-up

Figure 34-100. I/O Pin Pull-up Resistor Current vs. Input Voltage
V_{CC} = 1.8V

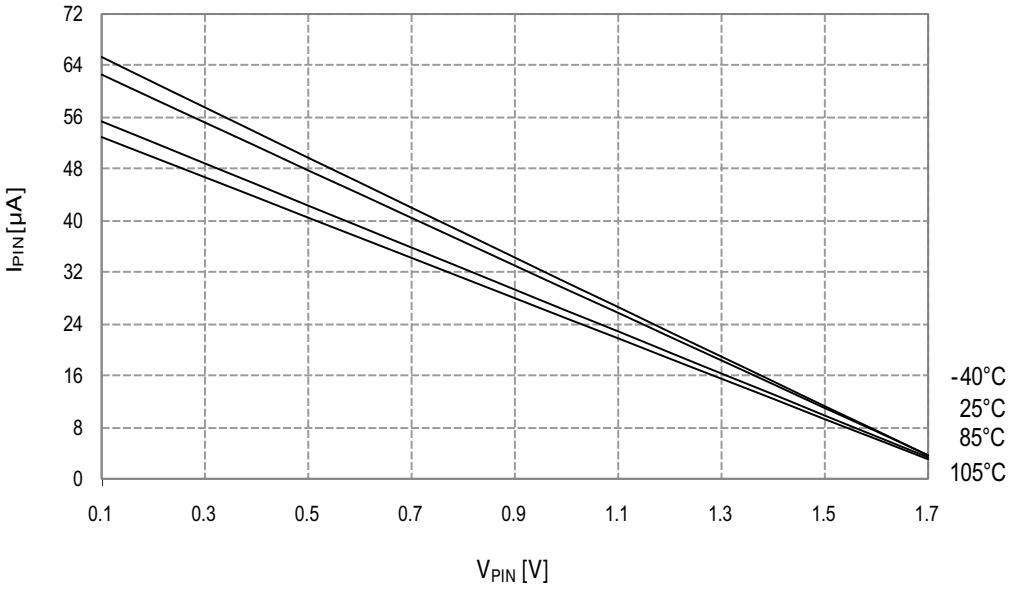


Figure 34-101. I/O Pin Pull-up Resistor Current vs. Input Voltage
V_{CC} = 3.0V

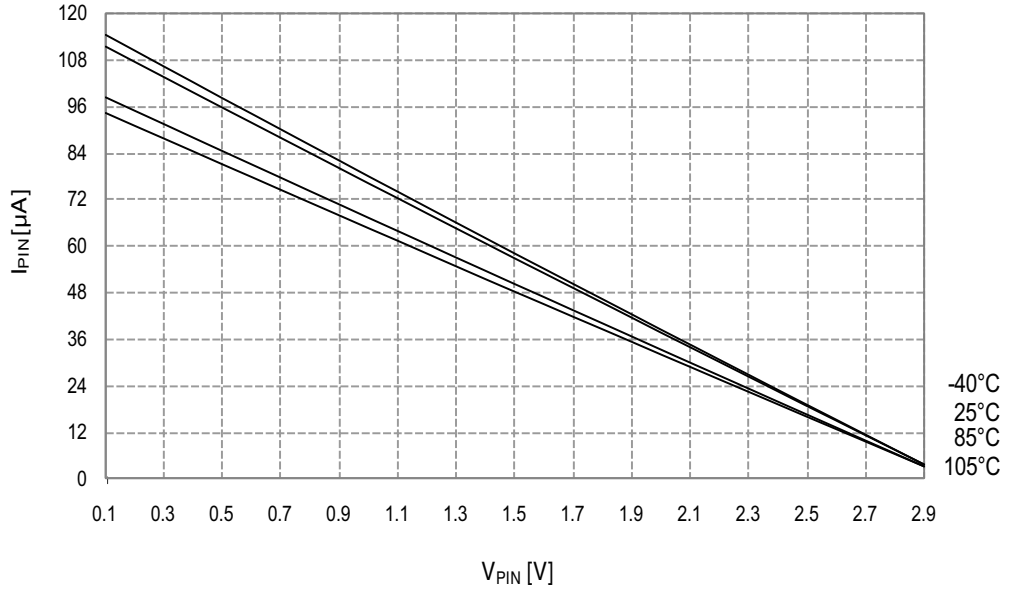


Figure 34-116. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

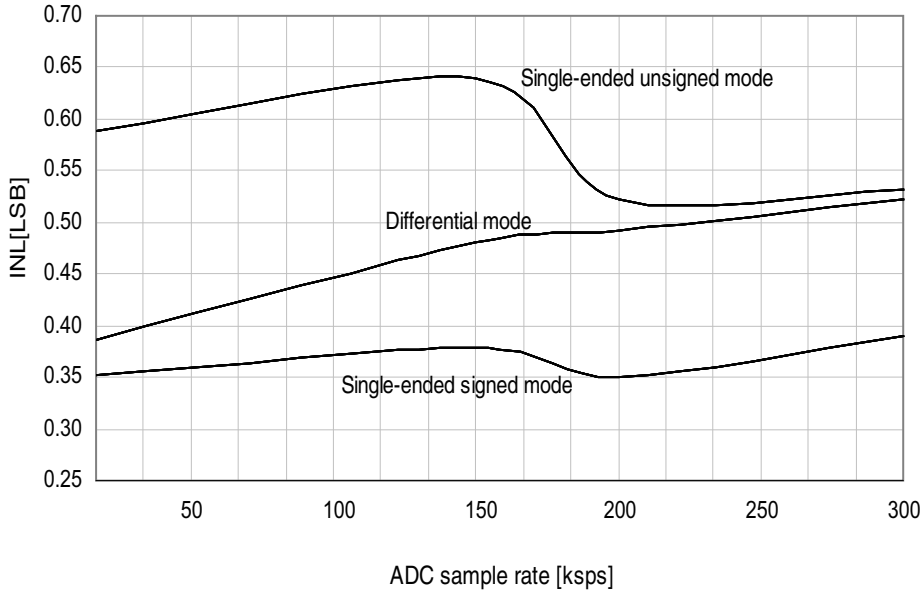
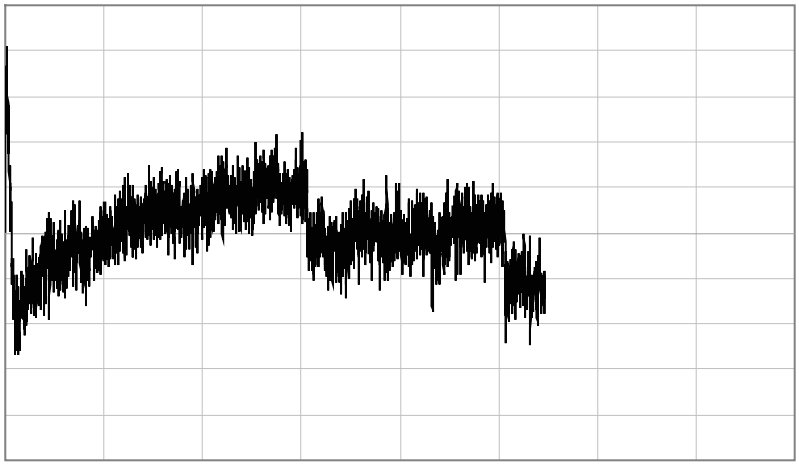
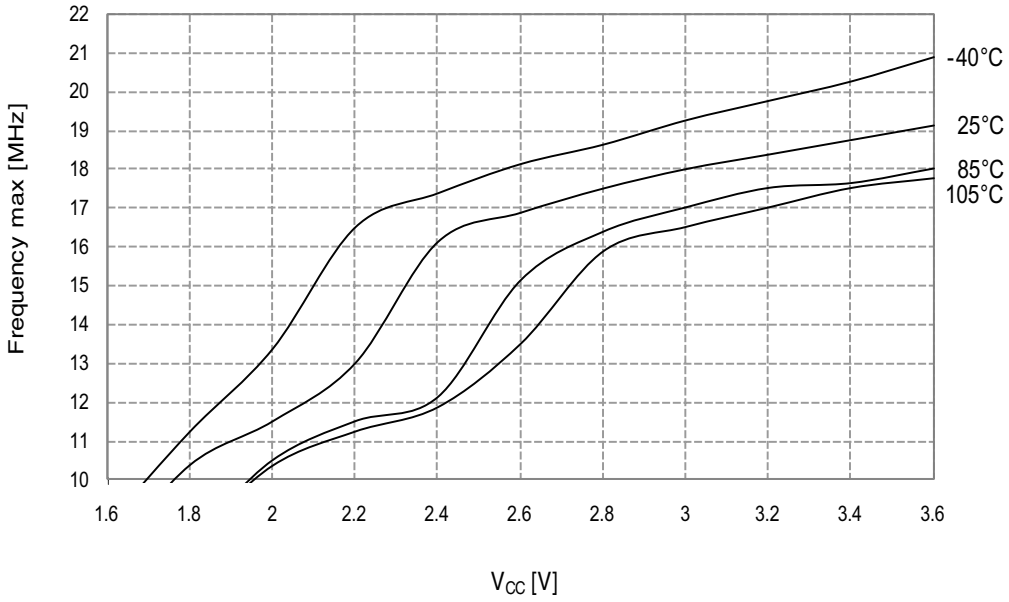


Figure 34-117. INL Error vs. Input Code



34.2.11 PDI Characteristics

Figure 34-158. Maximum PDI Frequency vs. V_{CC}



36. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 8493I – 12/2014

1.	Some minor corrections according to the template.
2.	Trademark corrections.
3.	Several cross-references have been corrected.

36.2 8493H – 07/2014

1.	Updated the “Ordering Information” on page 2. Added ordering codes for ATxmega16C4/32C4 @ 105°C.
2.	Updated Table 33-4 on page 67 and Table 33-33 on page 86. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
3.	Updated Table 33-17 on page 75 and Table 33-46 on page 94. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
4.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and in Section 27.1 “Features” on page 48.
5.	Updated the typical characteristics of “Atmel ATxmega16C4” and “Atmel ATxmega32C4” with characterizations @105°C
6.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 27. “AC – Analog Comparator” on page 48.
7.	Changed values for TCCO in Table 29-3 on page 53.

36.3 8493G – 01/2014

1.	Updated the typical characteristics with characterization at 105°C.

36.4 8493F – 10/2013

1.	Updated pin locations of TOSC1 and TOSC2 in Port E - Alternate functions in Table 29-5 on page 54.
2.	Updated pin locations of XTAL1, XTAL2, TOSC1, and TOSC2 in Port R - Alternate functions in Table 29-6 on page 54.

36.5 8493E – 10/2013

1.	Updated Port C - Alternate functions in Table 29-3 on page 53.