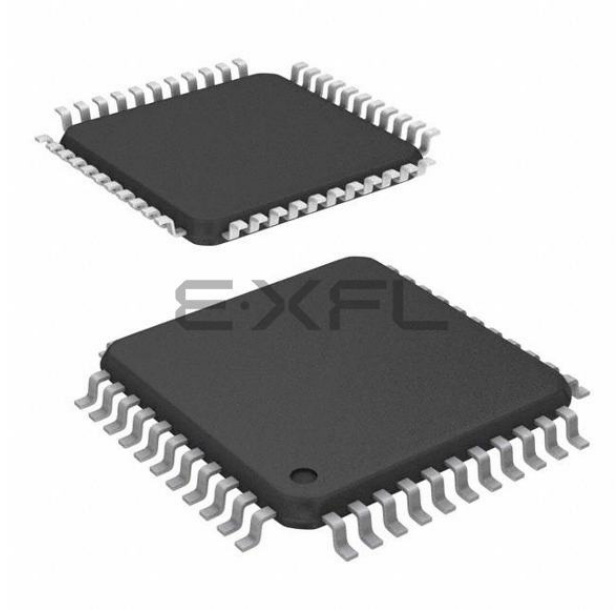

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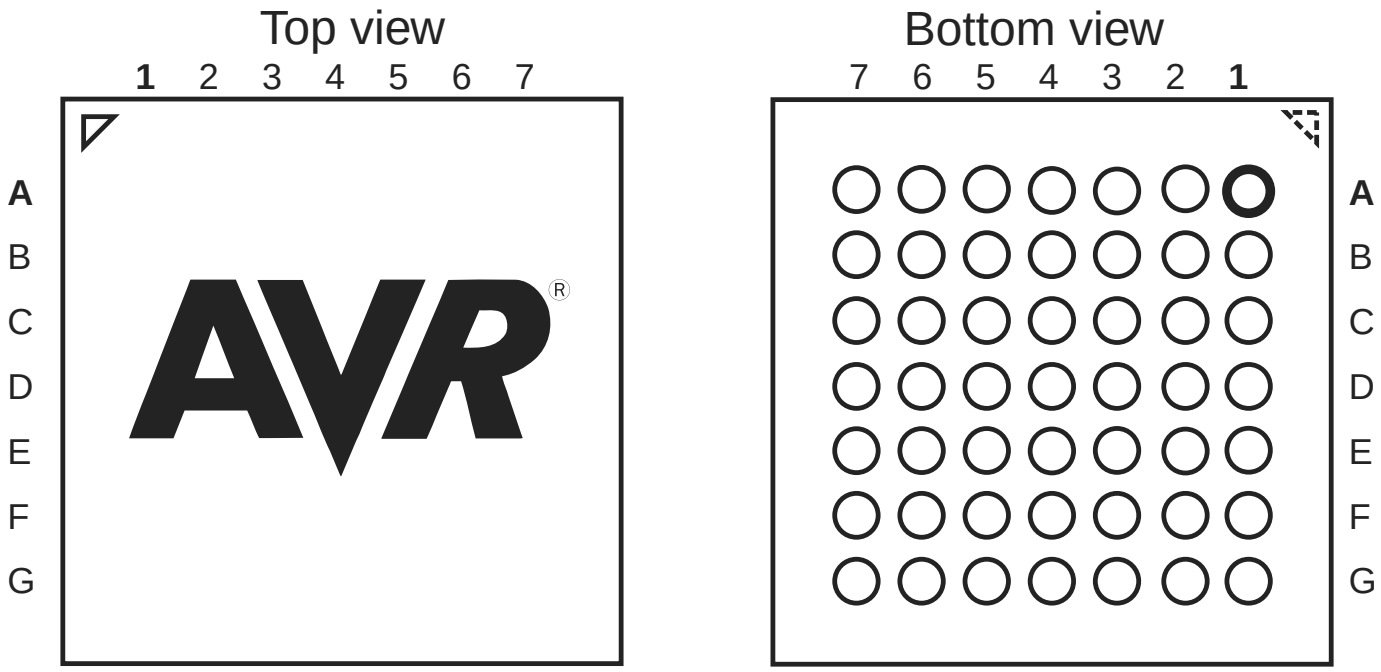
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c4-au

Figure 2-2. VFBGA Pinout



	1	2	3	4	5	6	7
A	PA3	AVCC	GND	PR1	PR0	PDI	PE3
B	PA4	PA1	PA0	GND	$\overline{\text{RESET}}$/PDI_CLK	PE2	VCC
C	PA5	PA2	PA6	PA7	GND	PE1	GND
D	PB1	PB2	PB3	PB0	GND	PD7	PE0
E	GND	GND	PC3	GND	PD4	PD5	PD6
F	VCC	PC0	PC4	PC6	PD0	PD1	PD3
G	PC1	PC2	PC5	PC7	GND	VCC	PD2

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA C4 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); four, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The XMEGA C4 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - Four bit-accessible general purpose registers for global variables or flags
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering Information” on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but

8. Event System

8.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- Four event channels for up to four different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoders
  - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

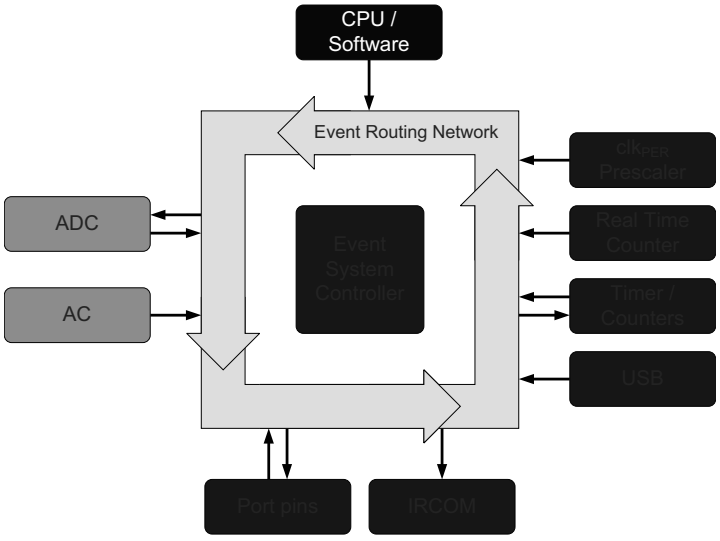
8.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, and CPU, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 8-1 shows a basic diagram of all connected peripherals. The event system can directly connect together analog to digital converter, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. Events can also be generated from software and the peripheral clock.

Figure 8-1. Event System Overview and Connected Peripherals



The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

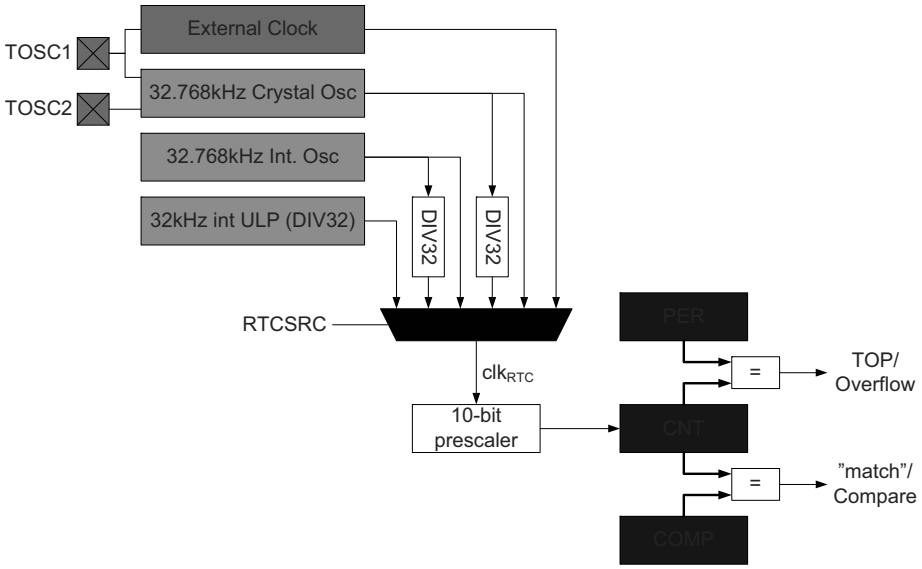
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview



25. CRC – Cyclic Redundancy Check Generator

25.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, and CPU
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

25.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

  Polynomial: $x^{16}+x^{12}+x^5+1$

  Hex value: 0x1021

- **CRC-32:**

  Polynomial: $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

  Hex value: 0x04C11DB7

29.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 29-1. Port A - Alternate Functions

PORT A	PIN #	INTERRUPT	ADCA POS/ GAIN POS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREFA
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 29-2. Port B - Alternate Functions

PORT B	PIN #	INTERRUPT	ADCA POS	REFB
PB0	4	SYNC	ADC8	AREFB
PB1	5	SYNC	ADC9	
PB2	6	SYNC/ASYNC	ADC10	
PB3	7	SYNC	ADC11	

Table 29-3. Port C - Alternate Functions

PORT C	PIN#	INTERRUPT	TCC0[1][2]	AWEXC	TCC1	USART C0[3]	USART C1	SPIC[4]	TWIC	CLOCKOUT[5]	EVENTOUT[6]
GND	8										
VCC	9										
PC0	10	SYNC	OC0A	$\overline{\text{OC0ALS}}$					SDA		
PC1	11	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	12	SYNC/ASYNC	OC0C	$\overline{\text{OC0BLS}}$		RXD0					
PC3	13	SYNC	OC0D	OC0BHS		TXD0					
PC4	14	SYNC		$\overline{\text{OC0CLS}}$	OC1A			$\overline{\text{SS}}$		RTCOUT	

Table 33-10. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL[1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL[1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset Error	Differential mode			8		mV
			Temperature drift		0.01		mV/K
			Operating voltage drift		0.25		mV/V
	Gain Error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain Error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

33.1.13 Clock and Oscillator Characteristics

33.1.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 33-19. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

33.1.13.2Calibrated 2MHz RC Internal Oscillator Characteristics

Table 33-20. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

33.1.13.3Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 33-21. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

33.1.13.432kHz Internal ULP Oscillator Characteristics

Table 33-22. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

Figure 34-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

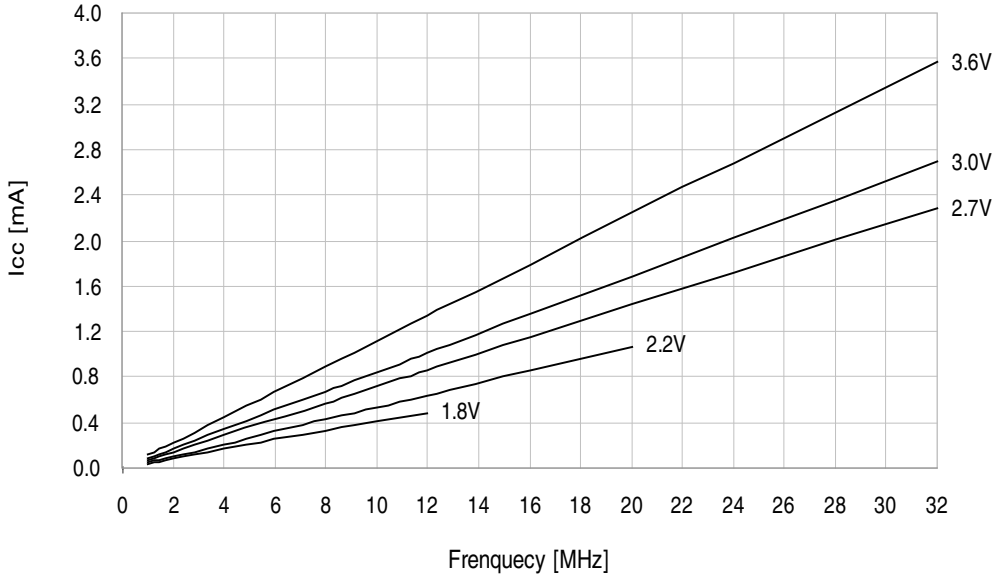


Figure 34-10.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

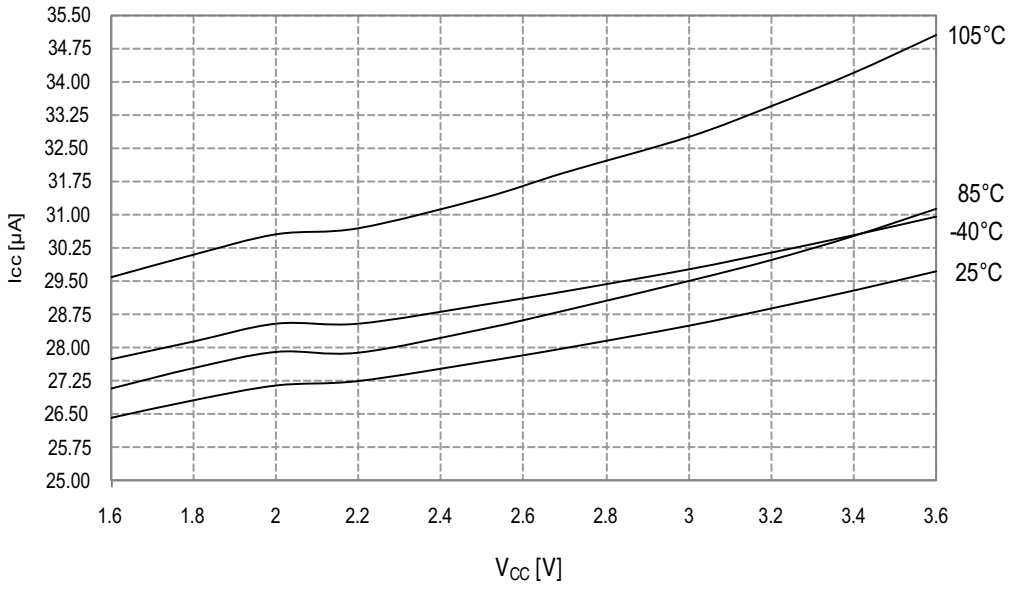


Figure 34-51. Analog Comparator Current Source vs. Calibration Value

T = 25°C

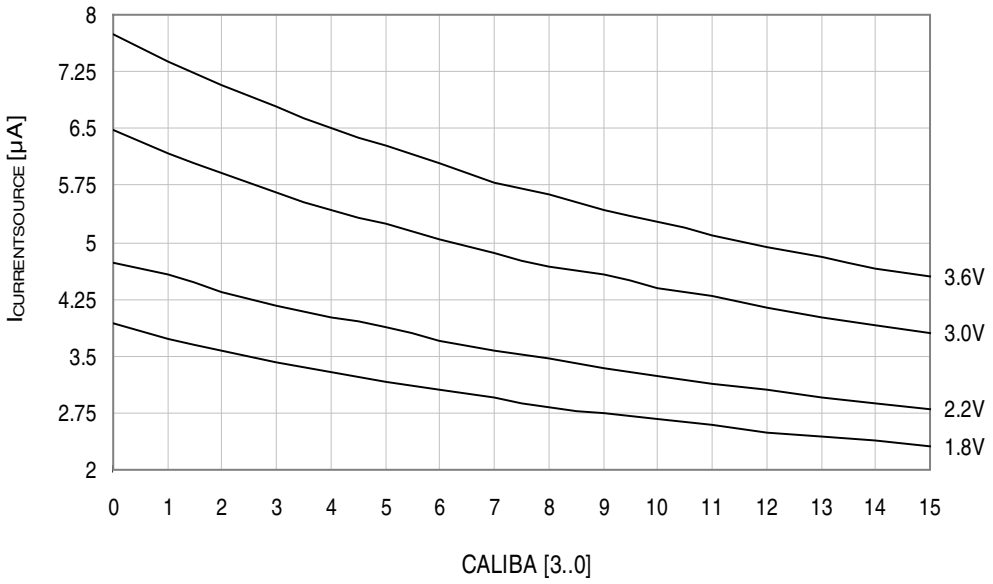


Figure 34-52. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

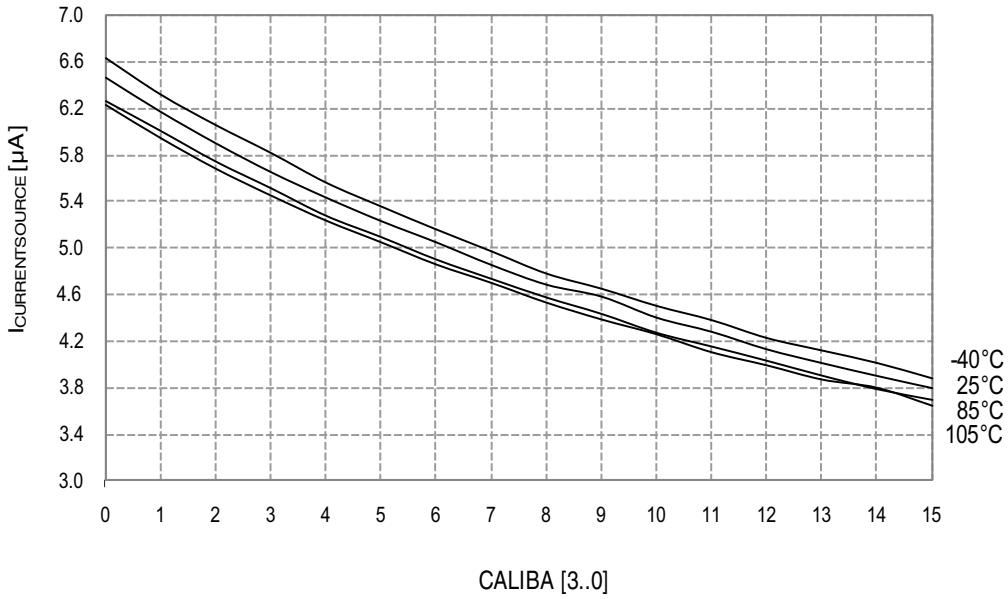


Figure 34-69. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

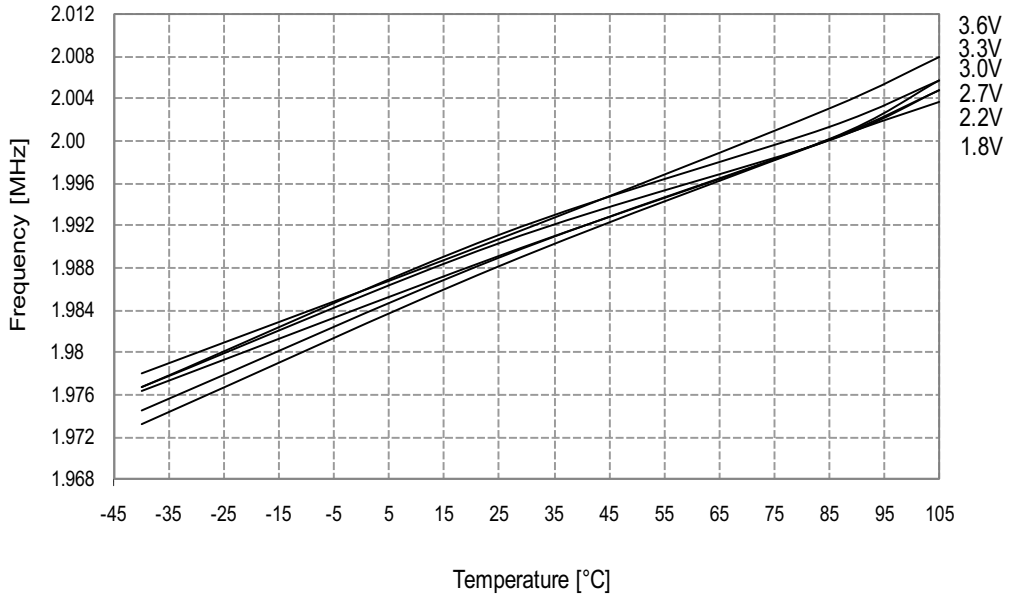
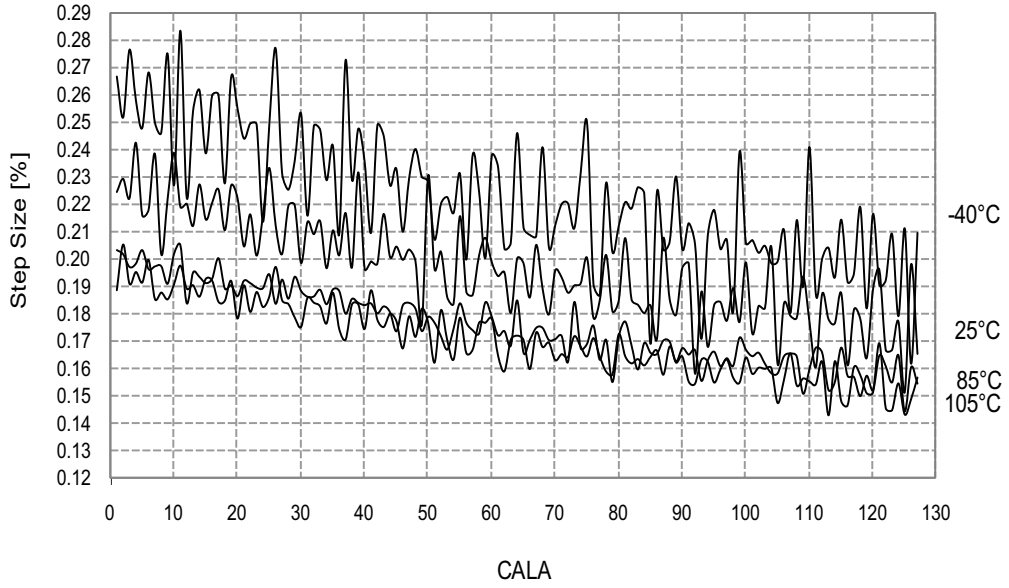


Figure 34-70. 2MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3V



34.1.11 PDI Characteristics

Figure 34-79. Maximum PDI Frequency vs. V_{CC}

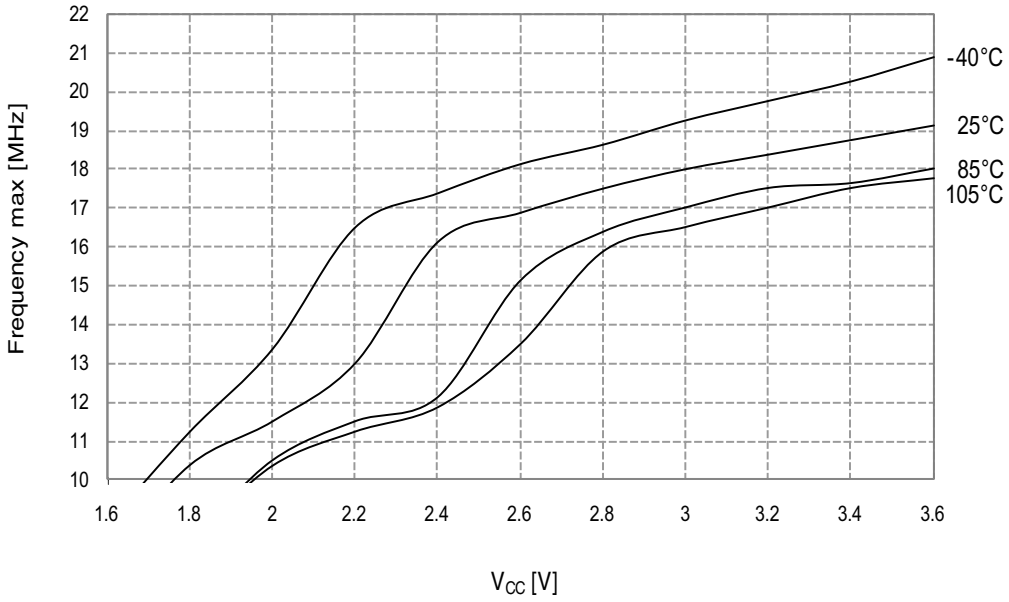
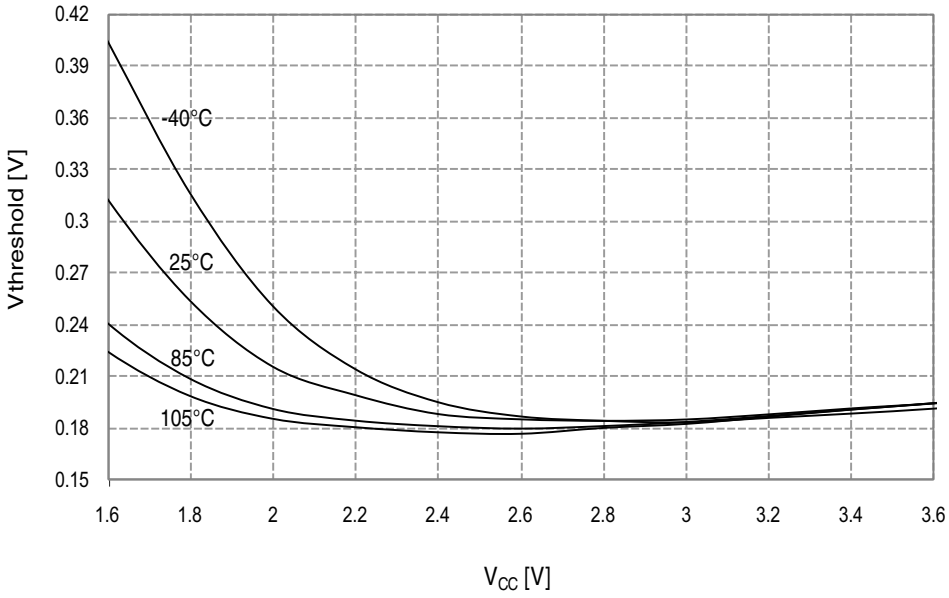


Figure 34-114. I/O Pin Input Hysteresis vs. V_{CC}



34.2.3 ADC Characteristics

Figure 34-115. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

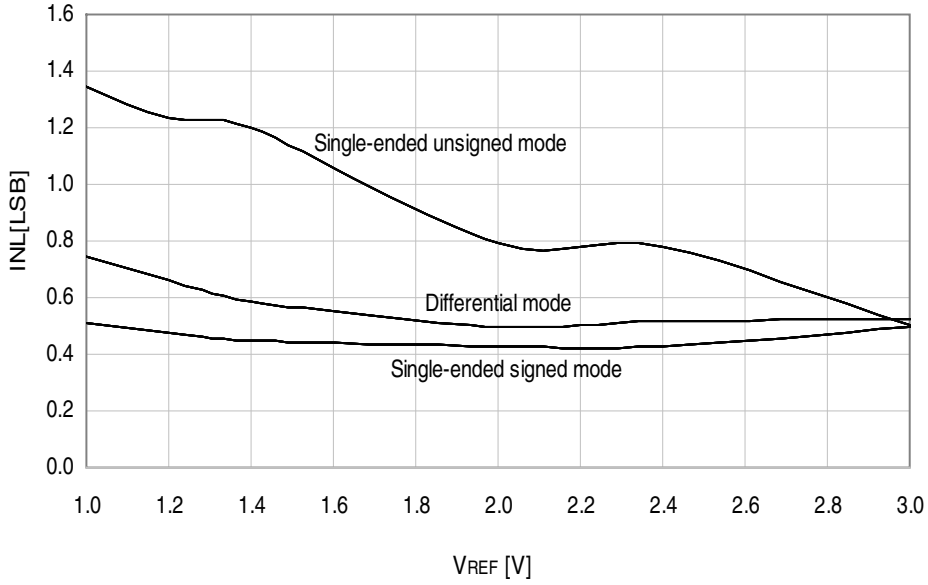
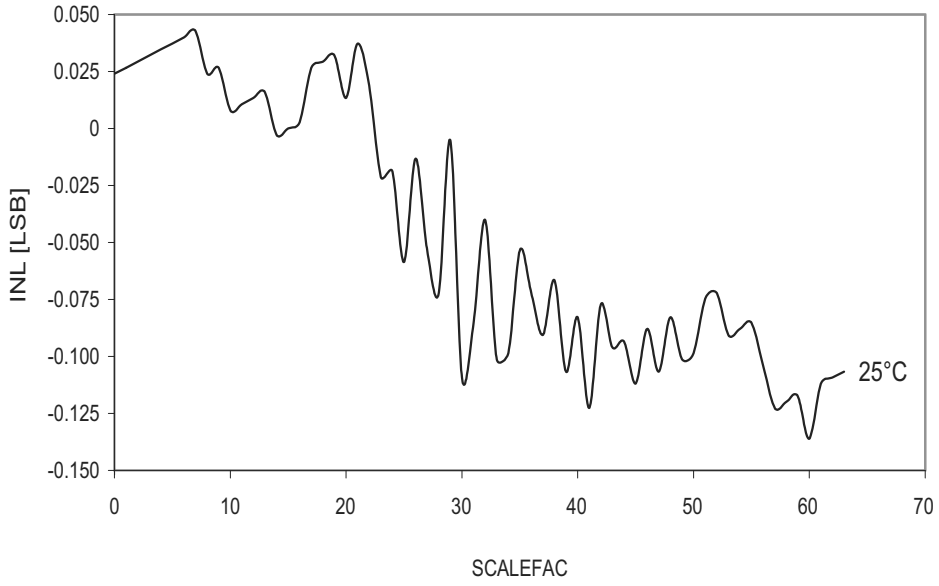


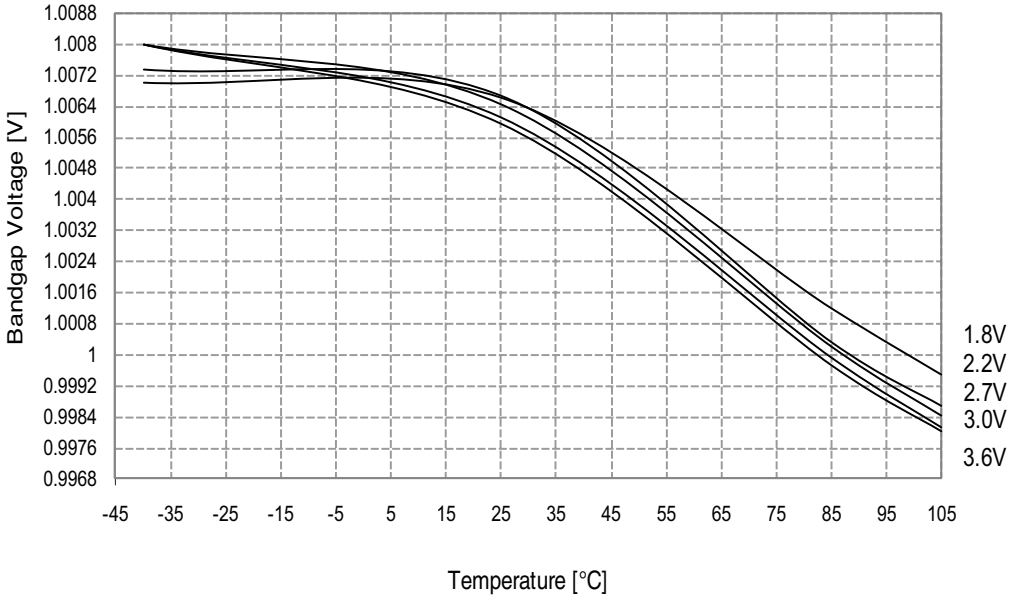
Figure 34-132. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V



34.2.5 Internal 1.0V Reference Characteristics

Figure 34-133. ADC Internal 1.0V Reference vs. Temperature



34.2.6 BOD Characteristics

Figure 34-134. BOD Thresholds vs. Temperature

BOD level = 1.6V

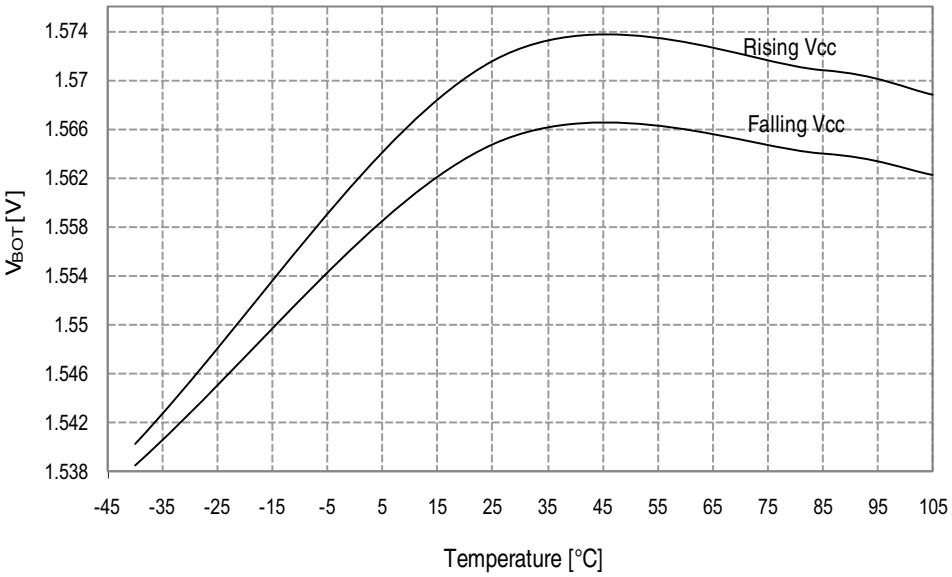
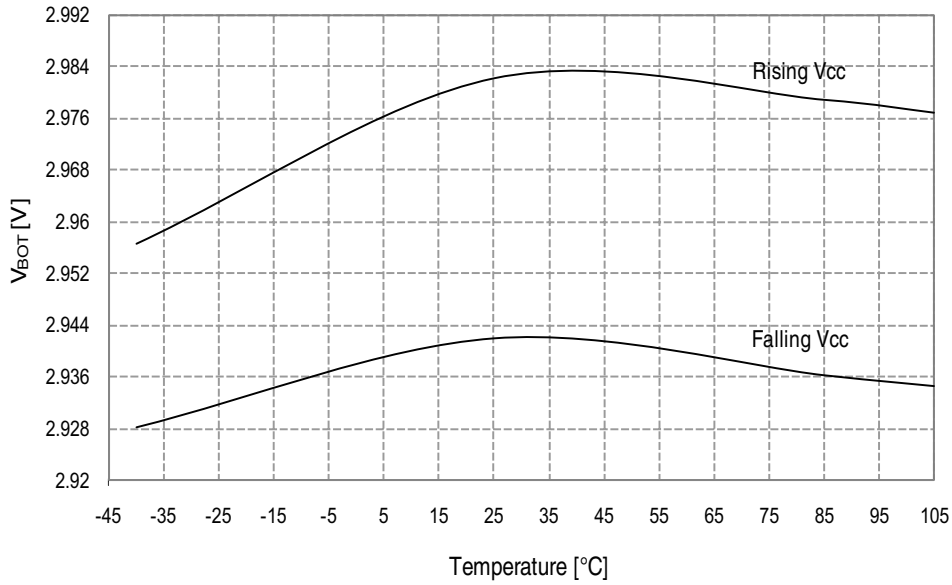


Figure 34-135. BOD Thresholds vs. Temperature

BOD level = 3.0V



34.2.8 Power-on Reset Characteristics

Figure 34-142. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode

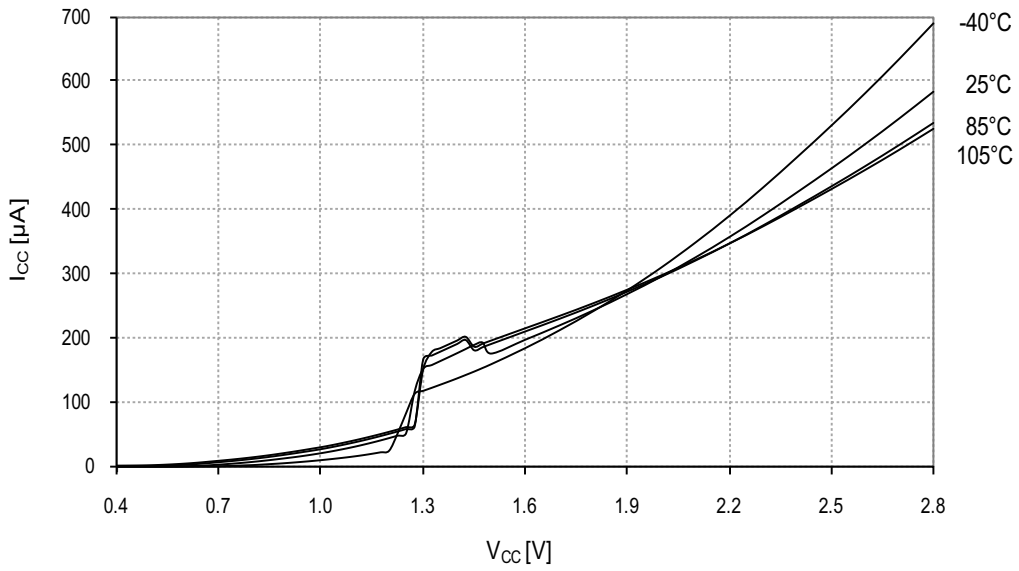
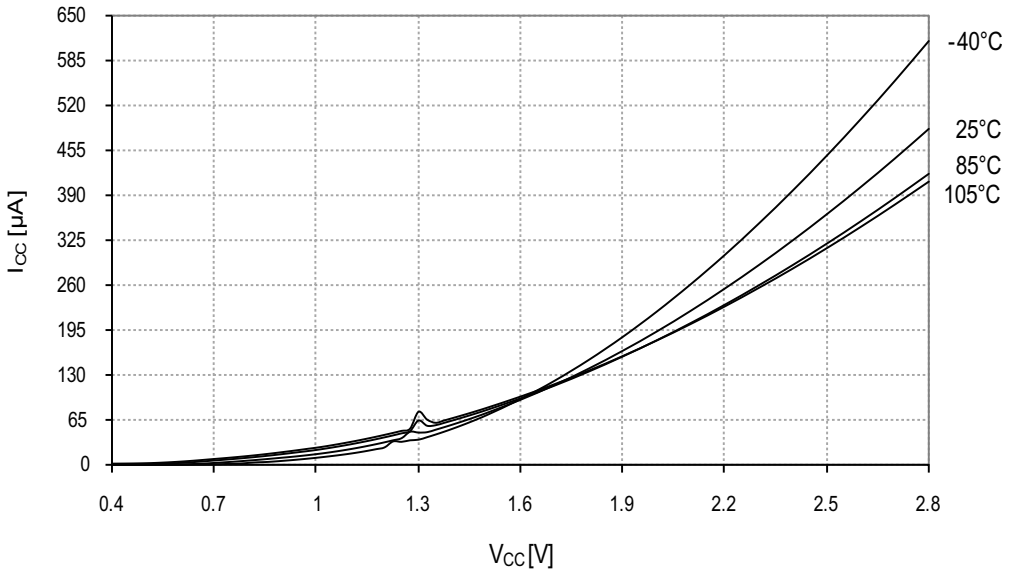


Figure 34-143. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode



36. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 8493I – 12/2014

1.	Some minor corrections according to the template.
2.	Trademark corrections.
3.	Several cross-references have been corrected.

36.2 8493H – 07/2014

1.	Updated the “Ordering Information” on page 2. Added ordering codes for ATxmega16C4/32C4 @ 105°C.
2.	Updated Table 33-4 on page 67 and Table 33-33 on page 86. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
3.	Updated Table 33-17 on page 75 and Table 33-46 on page 94. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
4.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and in Section 27.1 “Features” on page 48.
5.	Updated the typical characteristics of “Atmel ATxmega16C4” and “Atmel ATxmega32C4” with characterizations @105°C
6.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 27. “AC – Analog Comparator” on page 48.
7.	Changed values for TCCO in Table 29-3 on page 53.

36.3 8493G – 01/2014

1.	Updated the typical characteristics with characterization at 105°C.

36.4 8493F – 10/2013

1.	Updated pin locations of TOSC1 and TOSC2 in Port E - Alternate functions in Table 29-5 on page 54.
2.	Updated pin locations of XTAL1, XTAL2, TOSC1, and TOSC2 in Port R - Alternate functions in Table 29-6 on page 54.

36.5 8493E – 10/2013

1.	Updated Port C - Alternate functions in Table 29-3 on page 53.

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