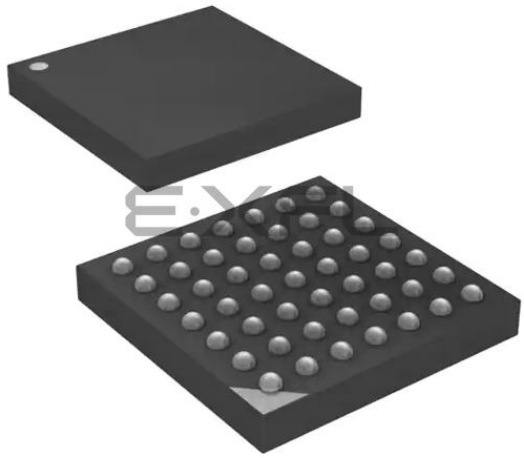

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What is "Embedded - Microcontrollers"?

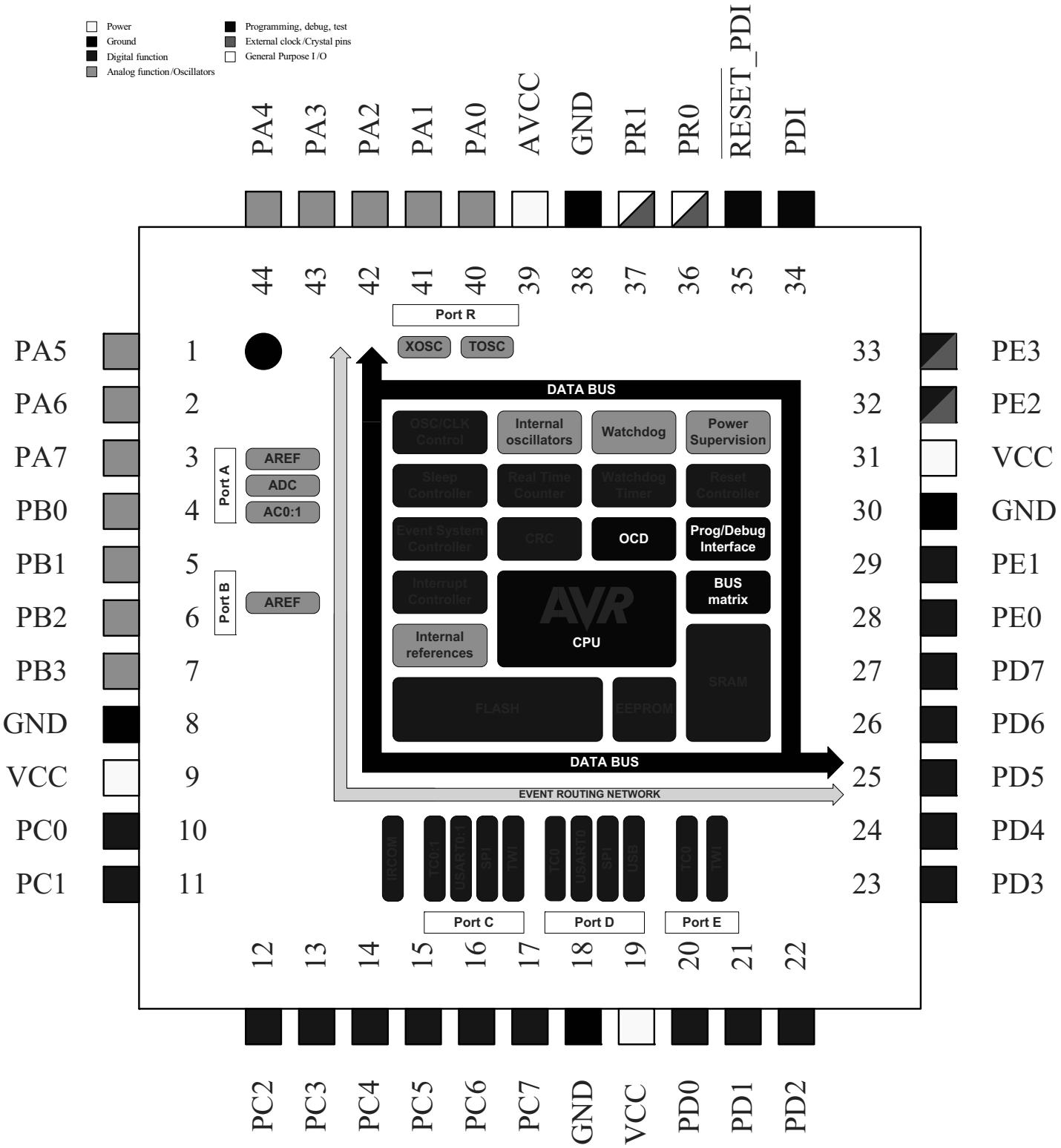
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c4-cu

2. Pinout/Block Diagram

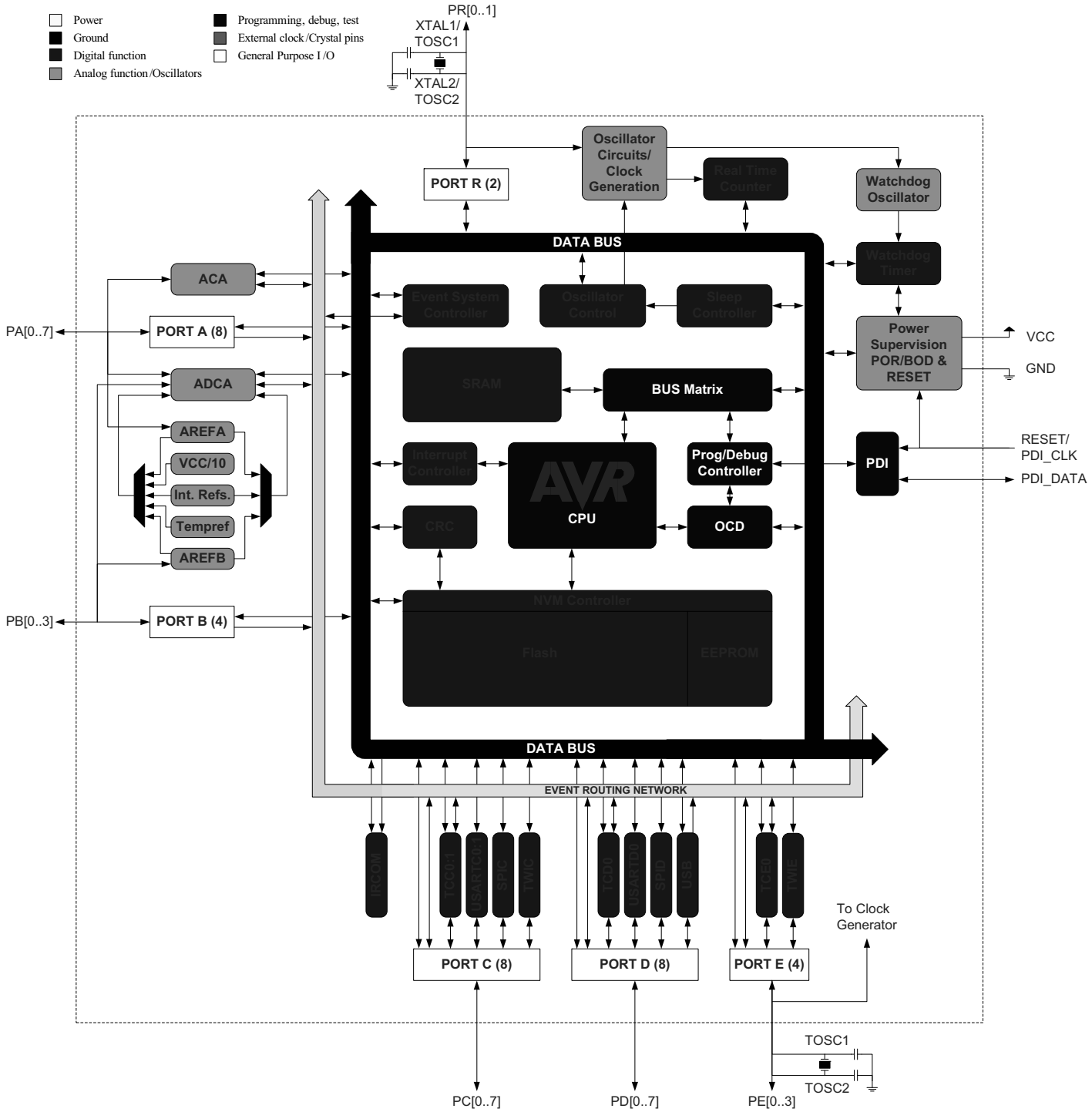
Figure 2-1. Block Diagram and Pinout



Notes: 1. For full details on pinout and alternate pin functions refer to “Pinout and Pin Functions” on page 51.
2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

3.1 Block Diagram

Figure 3-1. XMEGA C4 Block Diagram



8. Event System

8.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- Four event channels for up to four different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoders
  - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

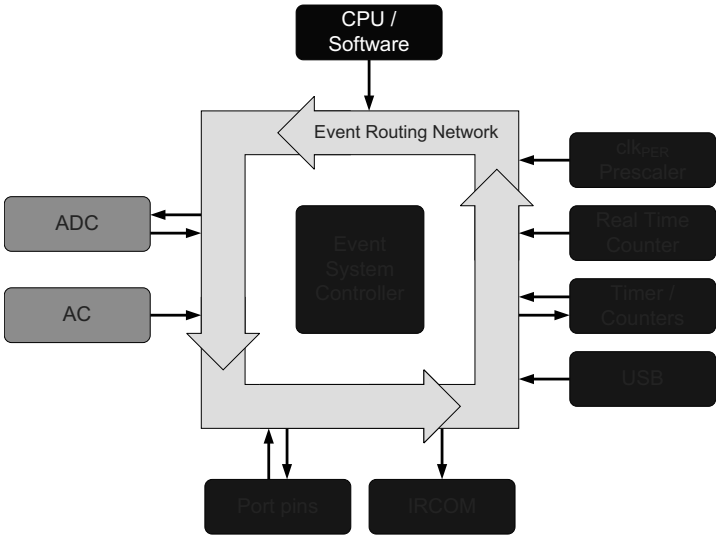
8.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, and CPU, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 8-1 shows a basic diagram of all connected peripherals. The event system can directly connect together analog to digital converter, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. Events can also be generated from software and the peripheral clock.

Figure 8-1. Event System Overview and Connected Peripherals

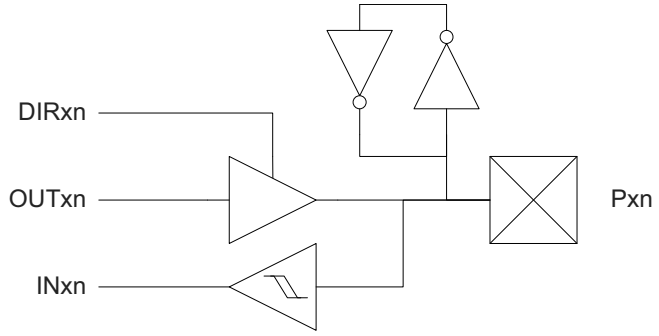


The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

14.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 14-4. I/O Configuration - Totem-pole with Bus-keeper



14.3.5 Others

Figure 14-5. Output Configuration - Wired-OR with Optional Pull-down

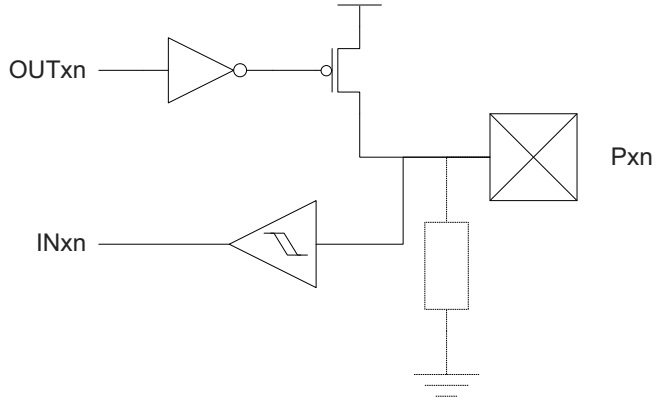
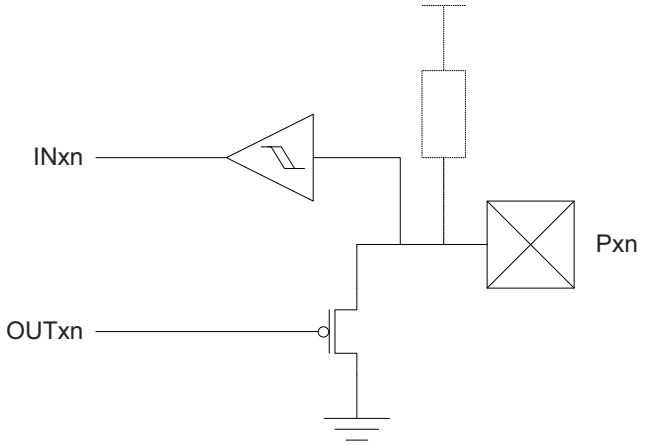


Figure 14-6. I/O Configuration - Wired-AND with Optional Pull-up



23. USART

23.1 Features

- Three identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits, and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multidevice bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

23.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC has two USARTs and PORTD has one USART. Notation of these peripherals are USARTC0, USARTC1, and USARTD0 respectively.

Base address	Name	Description
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/counter 0 on port C
0x0840	TCC1	Timer/counter 1 on port C
0x0880	AWEXC	Advanced waveform extension on port C
0x0890	HIRESC	High resolution extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial peripheral interface on port C
0x08F8	IRCOM	Infrared communication module
0x0900	TCD0	Timer/counter 0 on port D
0x09A0	USARTD0	USART 0 on port D
0x09C0	SPID	Serial peripheral interface on port D
0x0A00	TCE0	Timer/counter 0 on port E

32.2 PW

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Notes :

02/17/2012

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat	ZCP	PW	H

32.3 7P

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

A			
A1			
E/D	5.00 / 5.00		
E1/D1	3.90 / 3.90		
b			
eD/eE	Ball pitch : 0.5		
S			
bbb			
ddd			
ball diam			

12/07/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**		CBD		

33.1.3 Current Consumption

Table 33-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		200		
			V_{CC} = 3.0V		410		
		2MHz, Ext. Clk	V_{CC} = 1.8V		350	600	
			V_{CC} = 3.0V		0.75	1.4	mA
		32MHz, Ext. Clk			7.5	12	
	Idle power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.0		µA
			V_{CC} = 3.0V		2.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		42		
			V_{CC} = 3.0V		85		
		2MHz, Ext. Clk	V_{CC} = 1.8V		85	225	
			V_{CC} = 3.0V		170	350	
		32MHz, Ext. Clk			2.7	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.0	4.5	
		T = 105°C			0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	10	
	Power-save power consumption(2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.5		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC,T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 33-11. Gain Stage Characteristics

R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain Error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		10		
	Offset Error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-150		

33.1.7 Analog Comparator Characteristics

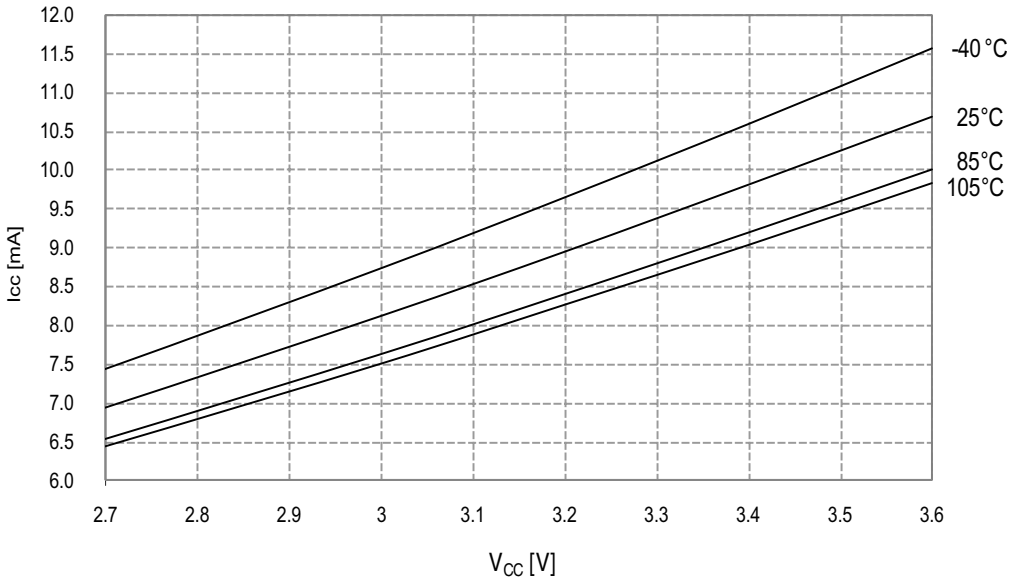
Table 33-12. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage	V_{CC}=1.6V - 3.6V		<±10		mV
I_{lk}	Input leakage current	V_{CC}=1.6V - 3.6V		<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none	V_{CC}=1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC}=1.6V - 3.6V		11		
V_{hys3}	Hysteresis, large	V_{CC}=1.6V - 3.6V		26		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		16	90	ns
		V_{CC}=1.6V - 3.6V		16		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, C_L=20pF		67k		
			2MHz crystal, C_L=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, C_L=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, C_L=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, C_L=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, C_L=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
R_Q	Negative impedance	XOSCPWR=1, FRQRANGE=1, C_L=20pF	9MHz crystal		1500		Ω
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, C_L=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, C_L=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, C_L=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, C_L=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, C_L=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, C_L=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, C_L=20pF		1.4		

Figure 34-7. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



34.1.1.2 Idle Mode Supply Current

Figure 34-8. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

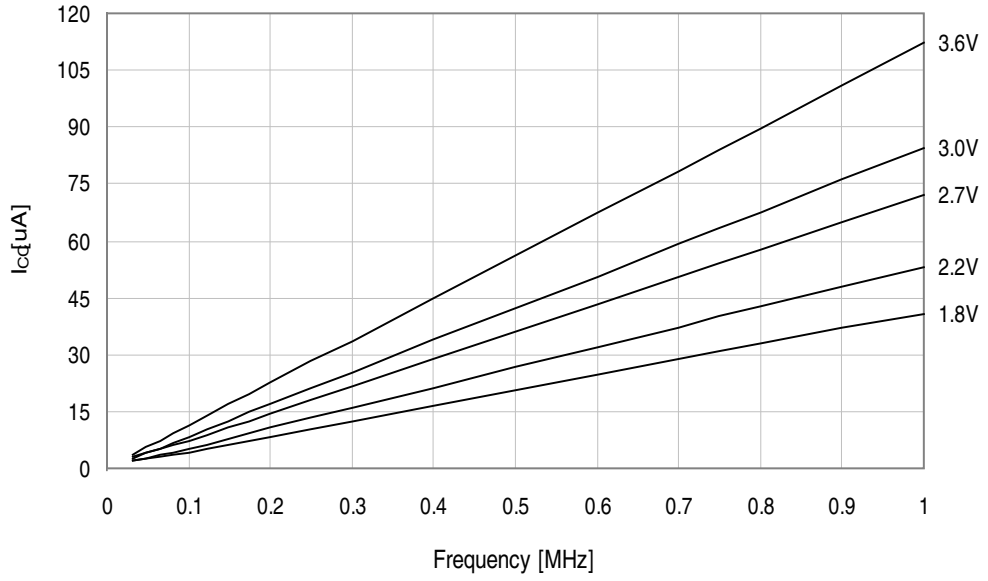
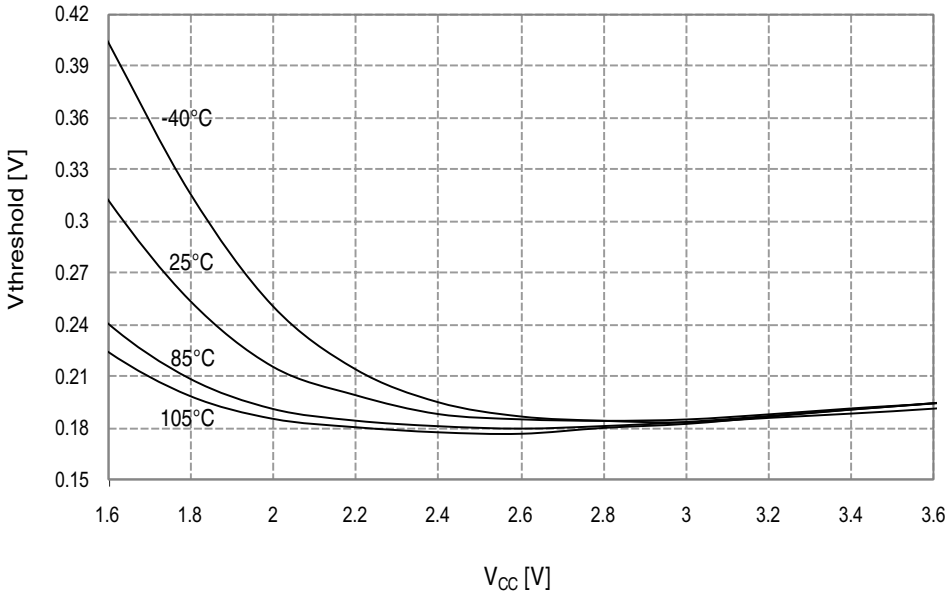


Figure 34-35. I/O Pin Input Hysteresis vs. V_{CC}



34.1.3 ADC Characteristics

Figure 34-36. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

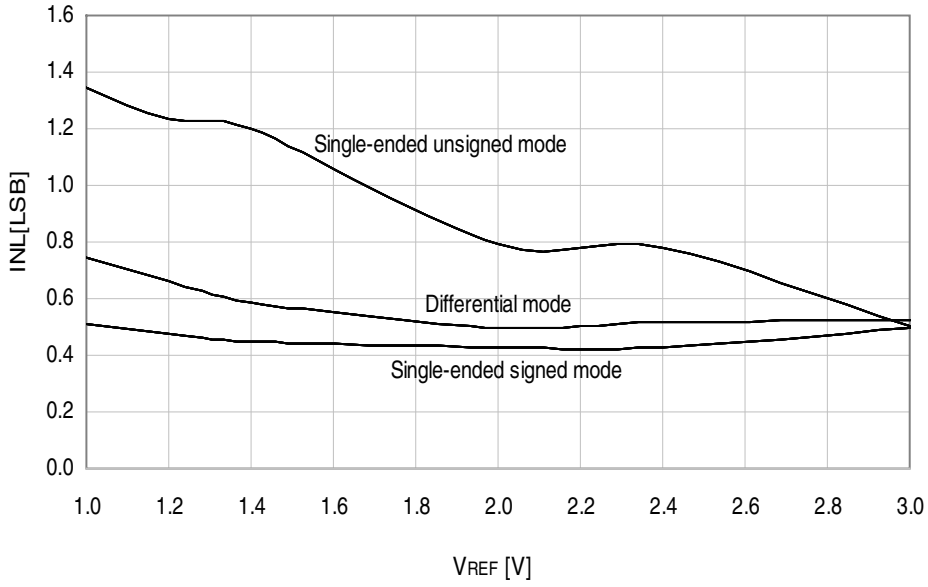


Figure 34-49. Analog Comparator Hysteresis vs. V_{CC}

Low power, small hysteresis

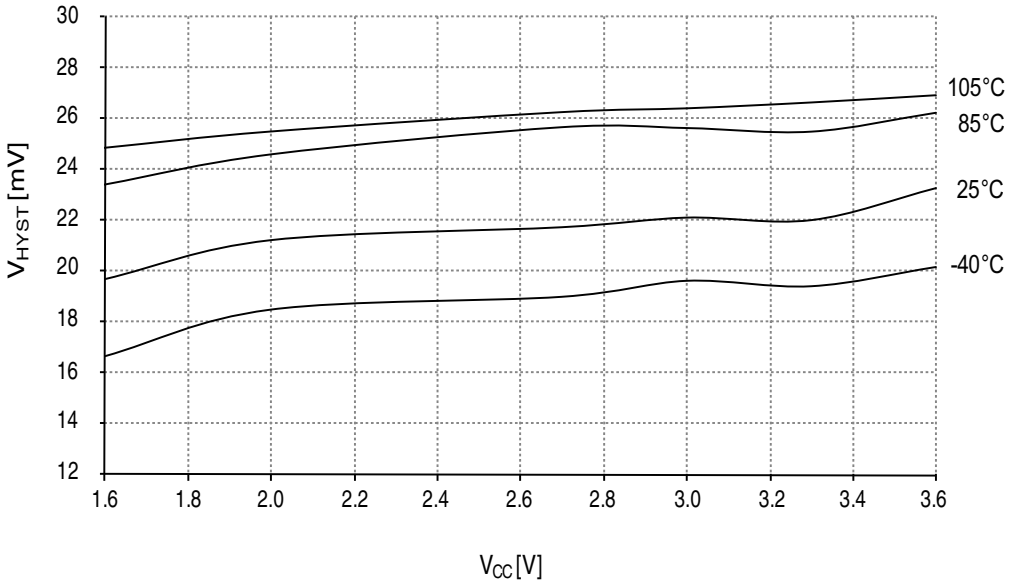
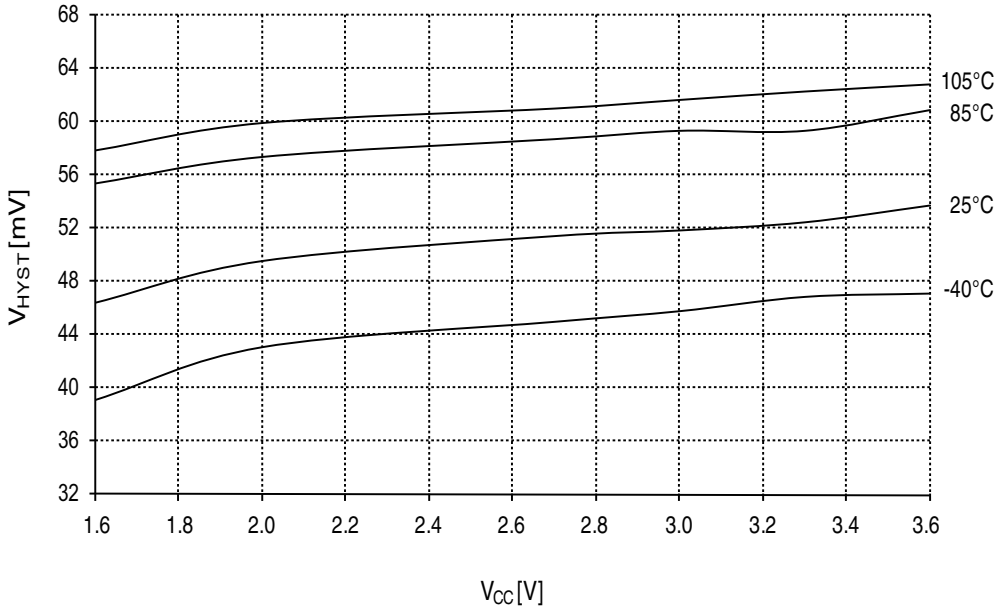


Figure 34-50. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis



34.2.1.3 Power-down Mode Supply Current

Figure 34-94. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

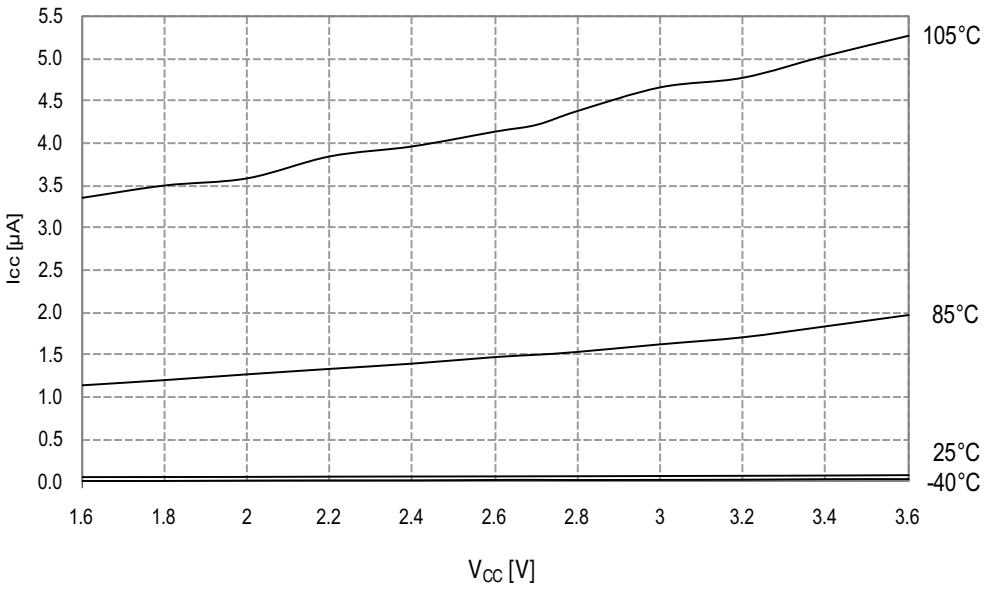


Figure 34-95. Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

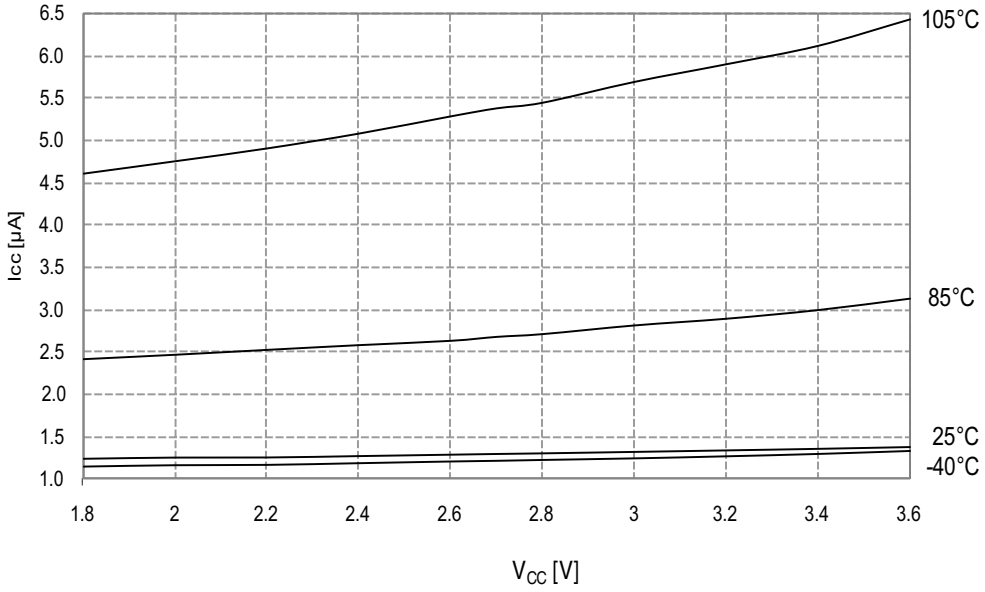
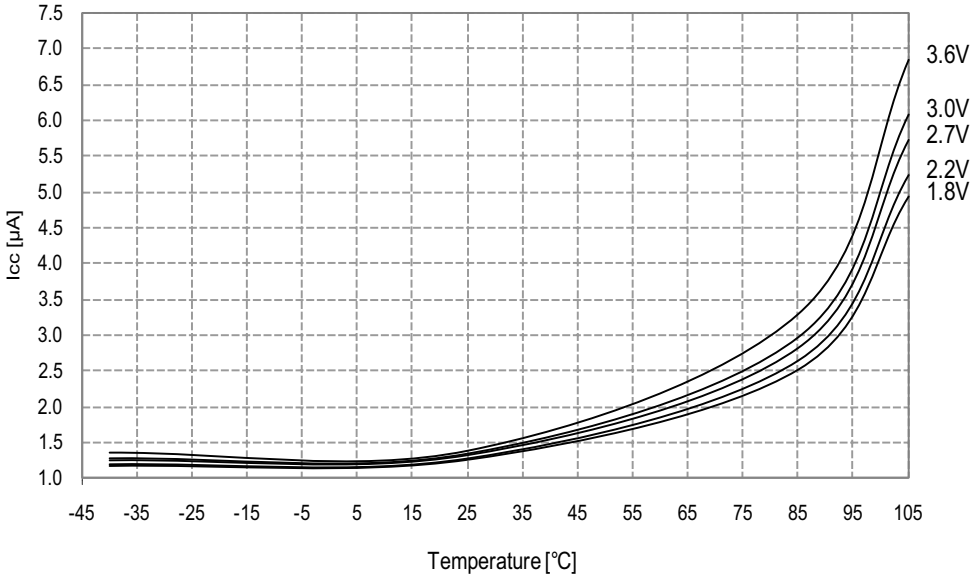


Figure 34-96. Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator



34.2.1.4 Power-save Mode Supply Current

Figure 34-97.Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC

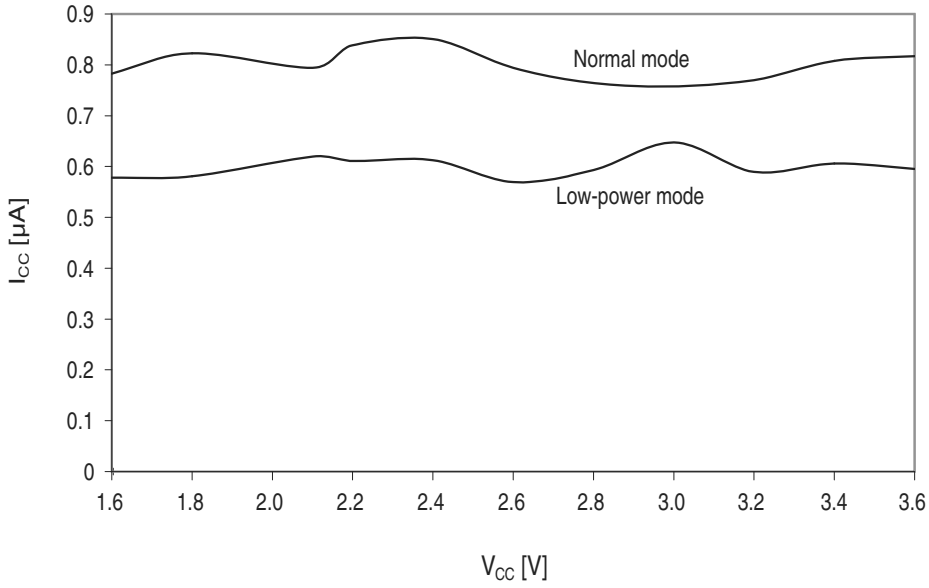


Figure 34-116. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

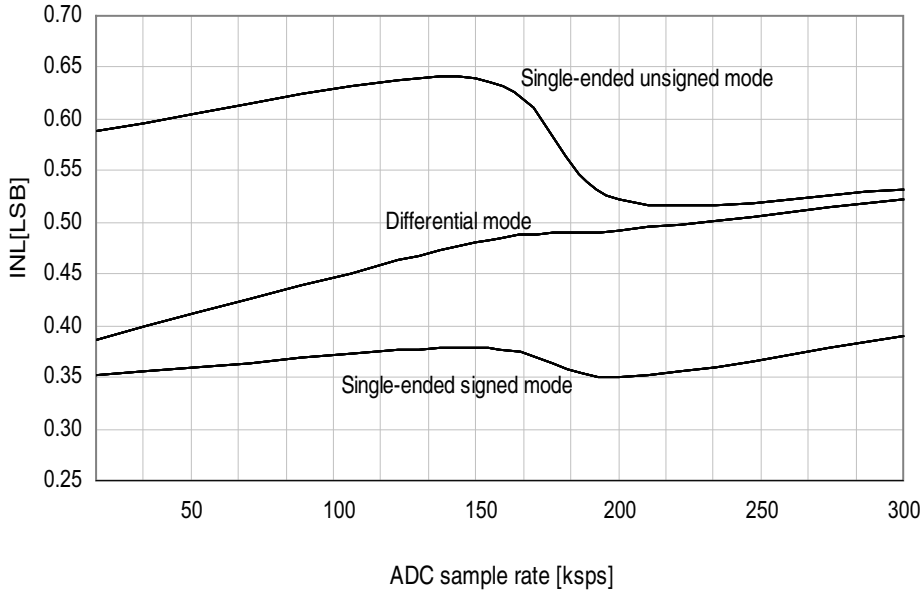


Figure 34-117. INL Error vs. Input Code

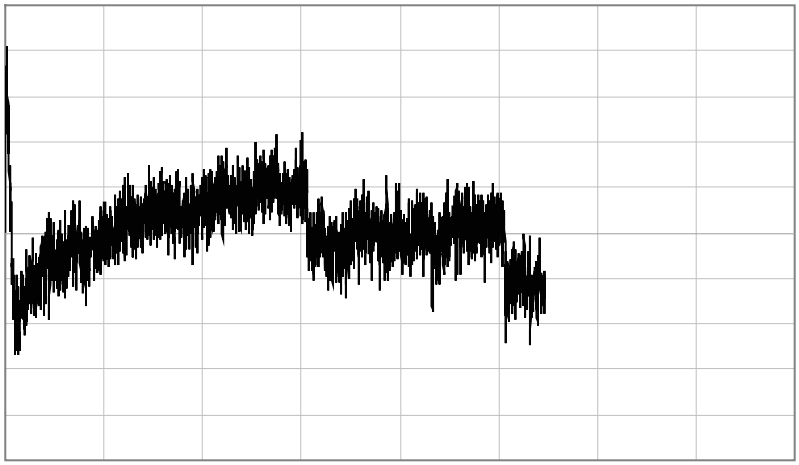
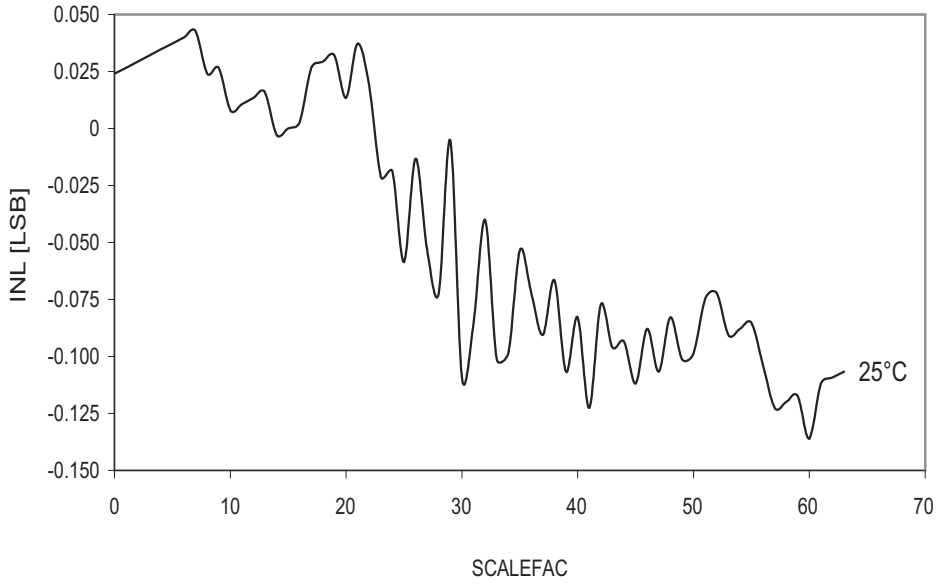


Figure 34-132. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V



34.2.5 Internal 1.0V Reference Characteristics

Figure 34-133. ADC Internal 1.0V Reference vs. Temperature

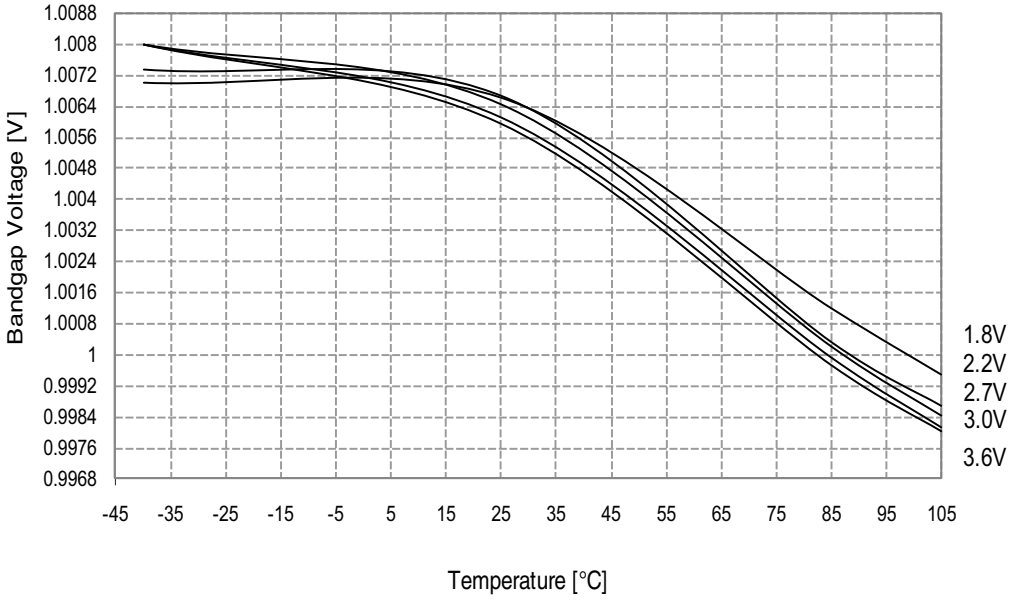
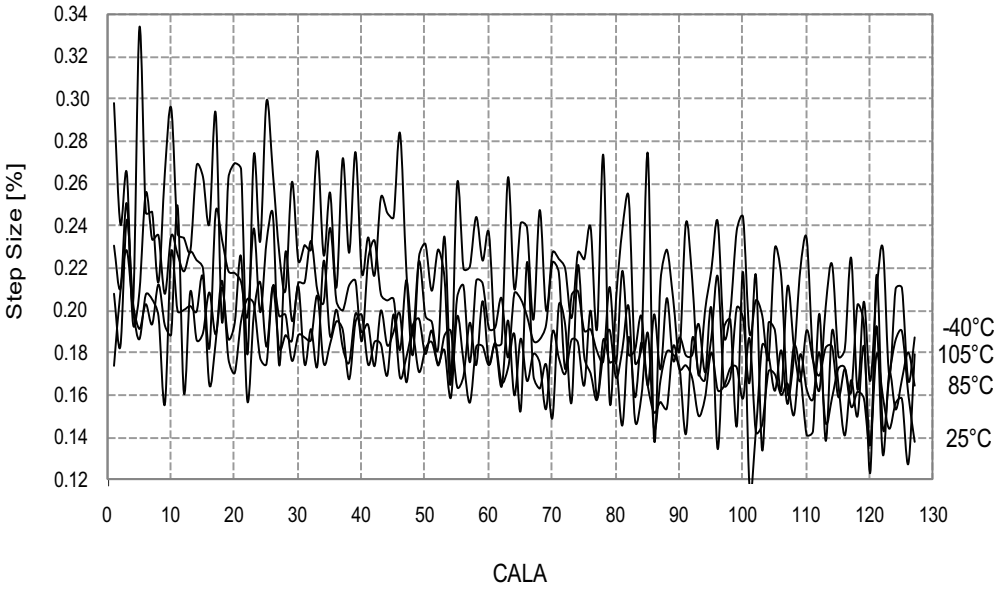


Figure 34-152. 32MHz Internal Oscillator CALA Calibration Step Size

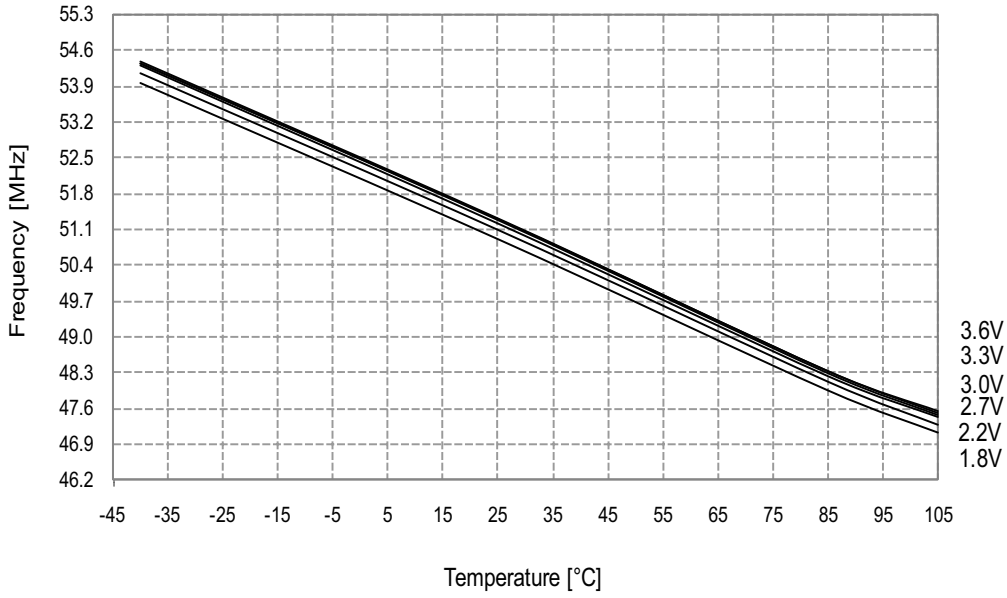
V_{CC} = 3.0V



34.2.9.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 34-153. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



36.6 8493D – 07/2013.

1.	Errata **Temperature sensor not calibrated** added to: ● ATxmega32C4 “Rev. H” on page 183 ● ATxmega16C4 “Rev. H” on page 183

36.7 8493C – 02/2013

1.	Updated the datasheet with Atmel new blue logo.
2.	Updated Figure 2-1 on page 4. PE2/PE3 are now half gray.
3.	Updated Figure 2-1 on page 4. Pin 19 is V_{CC} and not V_{DD}.
4.	Added Figure 2-2 on page 5.
5.	Updated Table 7-1 on page 15. Device ID for ATxmega32C4 is 44; 95; 1E. Device ID for ATxmega16 is 43; 94; 1E
6.	Updated “I/O Ports” on page 29. Removed “Optional slew rate control”. The feature doesn't exist in XMEGA C and XMEGA D devices.
7.	Updated Figure 27-1 on page 49, “Analog Comparator Overview”
8.	Updated “Pinout and Pin Functions” on page 51, to take into account the “Pinout/Block Diagram” on page 4.
9.	Updated “External Clock Characteristics” on page 77 and “ External Clock Characteristics” on page 96. Added Table 33-24 on page 77, Table 33-25 on page 78, Table 33-53 on page 96, and Table 33-54 on page 97.
10.	Updated Table 33-26 on page 78, and Table 33-55 on page 97. Added ESR parameter.
11.	Updated Table 33-29 on page 83 and Table 33-58 on page 102. Input low voltage V_{IL} min for I^2C is -0.5V.
12.	Added “Electrical Characteristics” for “Atmel ATxmega16C4” on page 65.
13.	Added “Typical Characteristics” for “Atmel ATxmega16C4” on page 103.
15.	Updated “Errata” on page 183. Added Errata to all rev H: AC system status flags are only valid if AC-system is enabled.

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1.	Updated “Packaging Information” on page 62. Added “7P” on page 64.
2.	Added “Electrical Characteristics” on page 65.
3.	Added “Typical Characteristics” on page 103.

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1.	Initial revision.