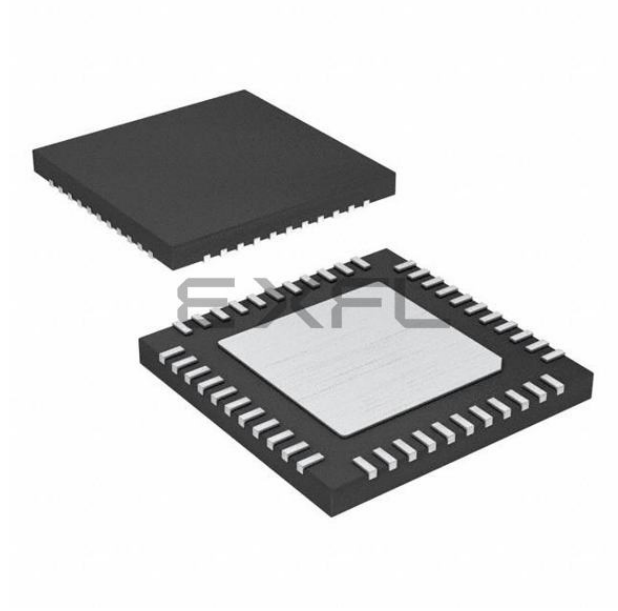

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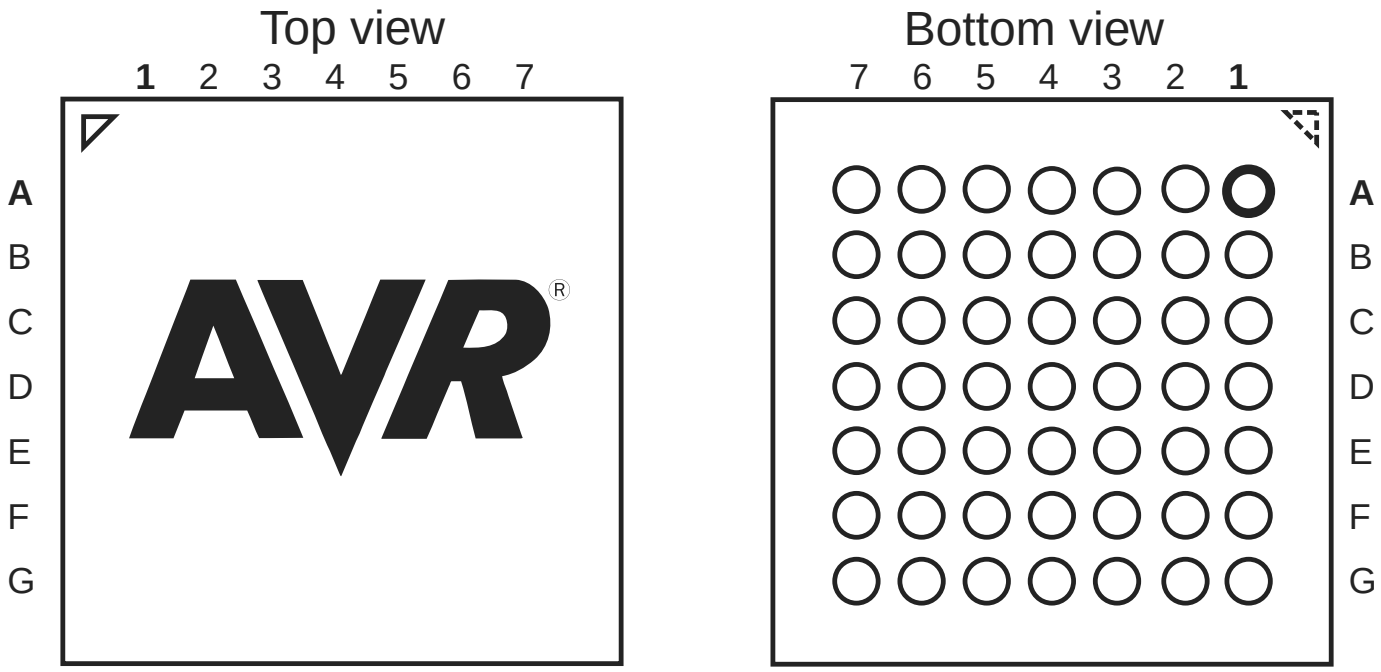
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c4-mh

Figure 2-2. VFBGA Pinout



	1	2	3	4	5	6	7
A	PA3	AVCC	GND	PR1	PR0	PDI	PE3
B	PA4	PA1	PA0	GND	$\overline{\text{RESET}}$/PDI_CLK	PE2	VCC
C	PA5	PA2	PA6	PA7	GND	PE1	GND
D	PB1	PB2	PB3	PB0	GND	PD7	PE0
E	GND	GND	PC3	GND	PD4	PD5	PD6
F	VCC	PC0	PC4	PC6	PD0	PD1	PD3
G	PC1	PC2	PC5	PC7	GND	VCC	PD2

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA C4 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); four, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The XMEGA C4 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

30. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA C4. For complete register description and summary for each peripheral module, refer to the XMEGA C manual.

Table 30-1. Peripheral Module Address Map

Base address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock control
0x0048	SLEEP	Sleep controller
0x0050	OSC	Oscillator control
0x0060	DFLLRC32M	DFLL for the 32 MHz internal RC oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC oscillator
0x0070	PR	Power reduction
0x0078	RST	Reset controller
0x0080	WDT	Watch-dog timer
0x0090	MCU	MCU control
0x00A0	PMIC	Programmable multilevel interrupt controller
0x00B0	PORTCFG	Port configuration
0x0180	EVSYS	Event system
0x00D0	CRC	CRC module
0x01C0	NVM	Nonvolatile memory (NVM) controller
0x0200	ADCA	Analog to digital converter on port A
0x0380	ACA	Analog comparator pair on port A
0x0400	RTC	Real time counter
0x0480	TWIC	Two wire interface on port C
0x04C0	USB	Universal serial Bus interface
0x04A0	TWIE	Two wire interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C

Table 33-5. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.8		µA
	32.768kHz int. oscillator				29		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			410		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			290		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				175		
	Temperature sensor				170		
	ADC	16ksps V_{REF} = Ext ref			1.2		mA
			CURRLIMIT = LOW		1.0		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext ref	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext ref			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			11		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.2.3 Current Consumption

Table 33-33. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		200		
			V_{CC} = 3.0V		410		
		2MHz, Ext. Clk	V_{CC} = 1.8V		350	600	
			V_{CC} = 3.0V		0.75	1.4	mA
		32MHz, Ext. Clk			7.5	12	
	Idle power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.0		µA
			V_{CC} = 3.0V		2.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		42		
			V_{CC} = 3.0V		85		
		2MHz, Ext. Clk	V_{CC} = 1.8V		85	225	
			V_{CC} = 3.0V		170	350	
		32MHz, Ext. Clk			2.7	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.0	4.5	
		T = 105°C			0.1	7.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	10	
	Power-save power consumption(2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.5		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

33.2.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 33-36. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-20		20	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4- 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.7		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

Table 33-40. Gain Stage Characteristics

R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain Error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		10		
	Offset Error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-150		

33.2.7 Analog Comparator Characteristics

Table 33-41. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage	V_{CC}=1.6V - 3.6V		<±10		mV
I_{lk}	Input leakage current	V_{CC}=1.6V - 3.6V		<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none	V_{CC}=1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC}=1.6V - 3.6V		11		
V_{hys3}	Hysteresis, large	V_{CC}=1.6V - 3.6V		26		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		16	90	ns
		V_{CC}=1.6V - 3.6V		16		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

33.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 33-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency(1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

33.2.13.6 External Clock Characteristics

Figure 33-10.External Clock Drive Waveform

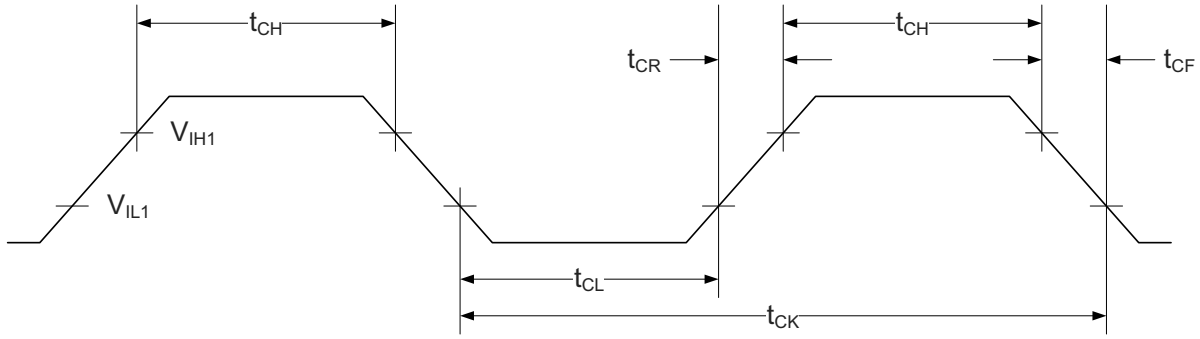


Table 33-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency(1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock high time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock low time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

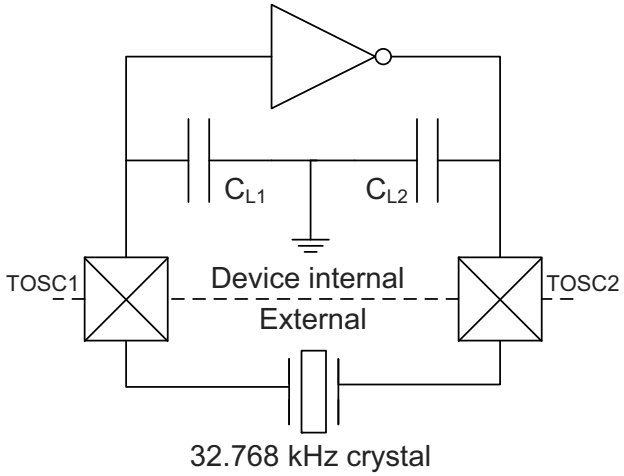
33.2.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 33-56. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 33-11 for definition.

Figure 33-11.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

33.2.14 SPI Characteristics

Figure 33-12. SPI Timing Requirements in Master Mode

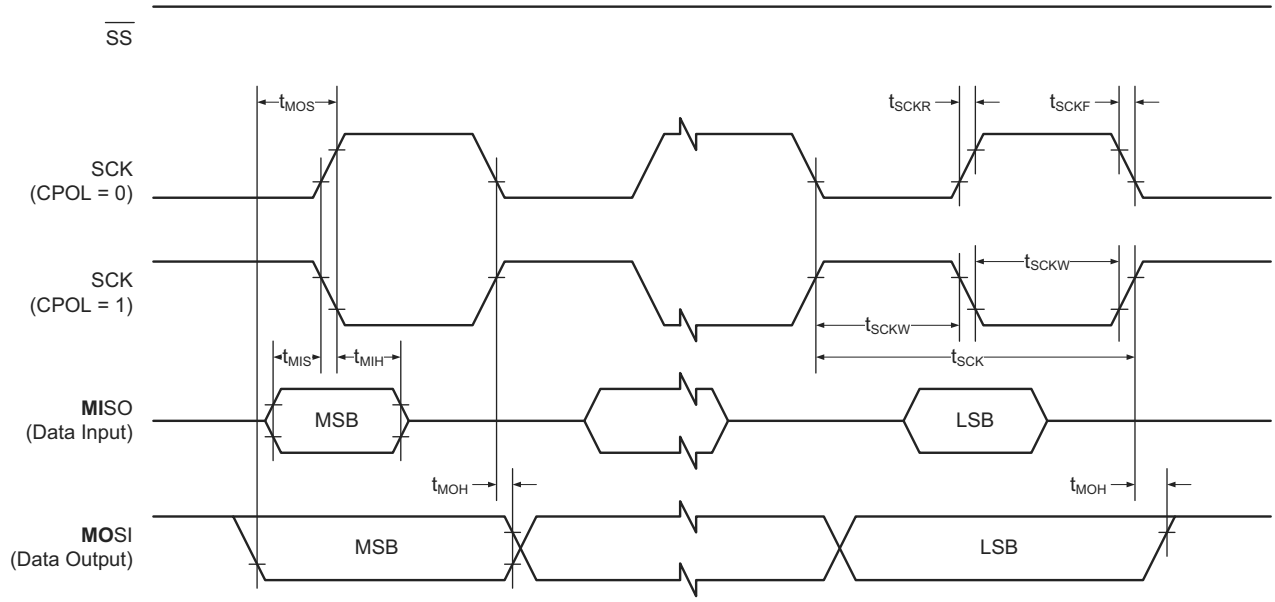


Figure 33-13. SPI Timing Requirements in Slave Mode

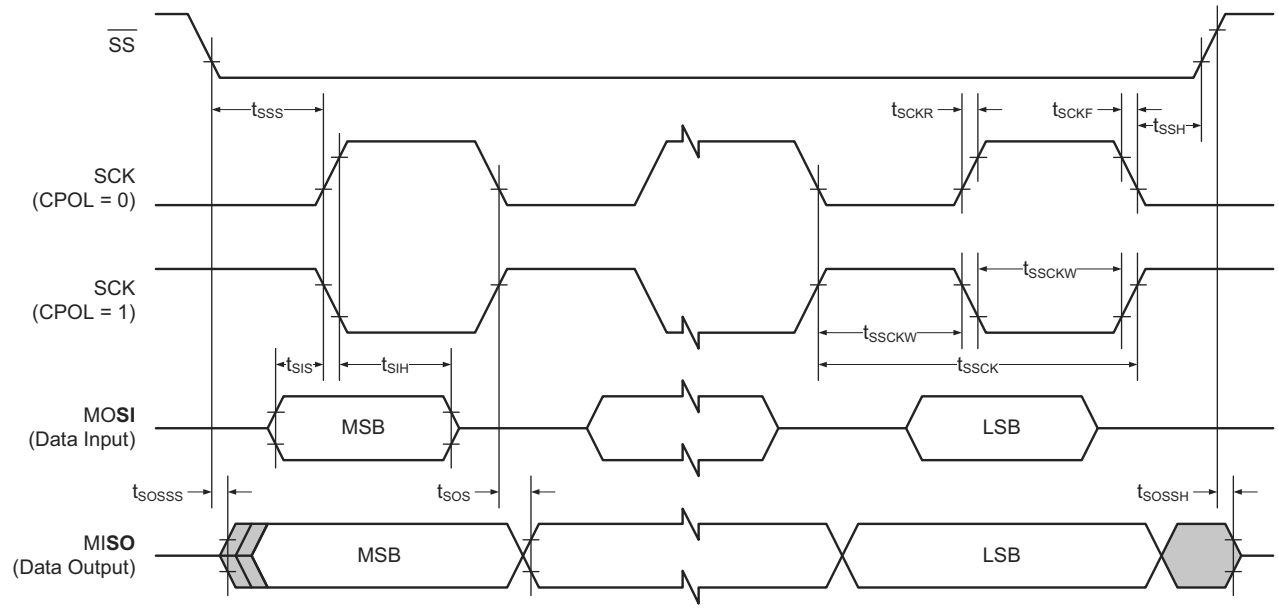
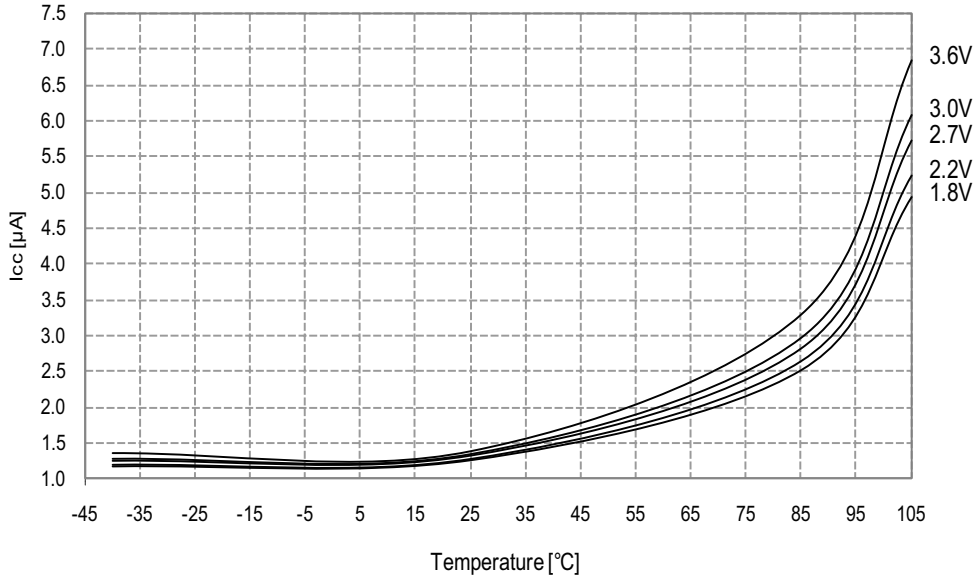


Figure 34-17.Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator



34.1.1.4 Power-save Mode Supply Current

Figure 34-18.Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC

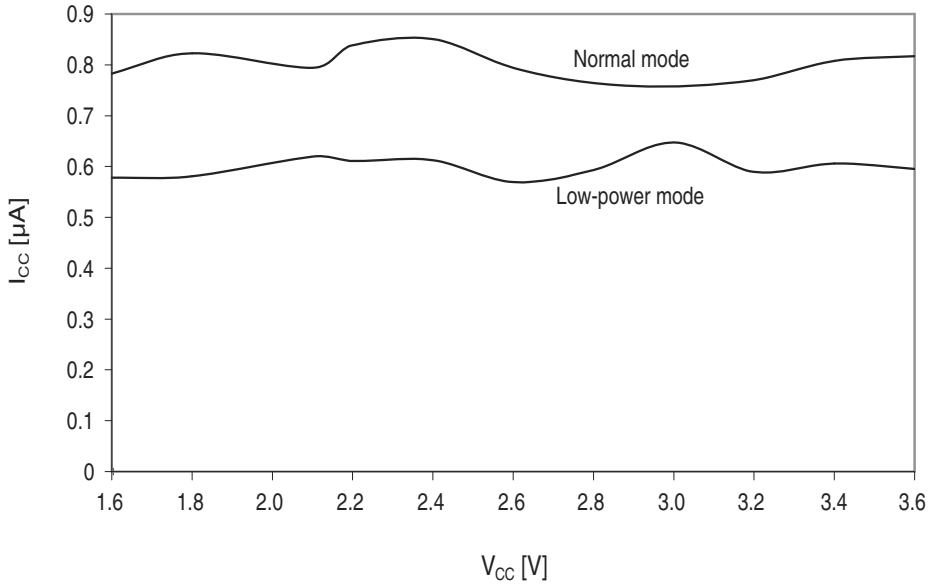


Figure 34-41.DNL Error vs. Input Code

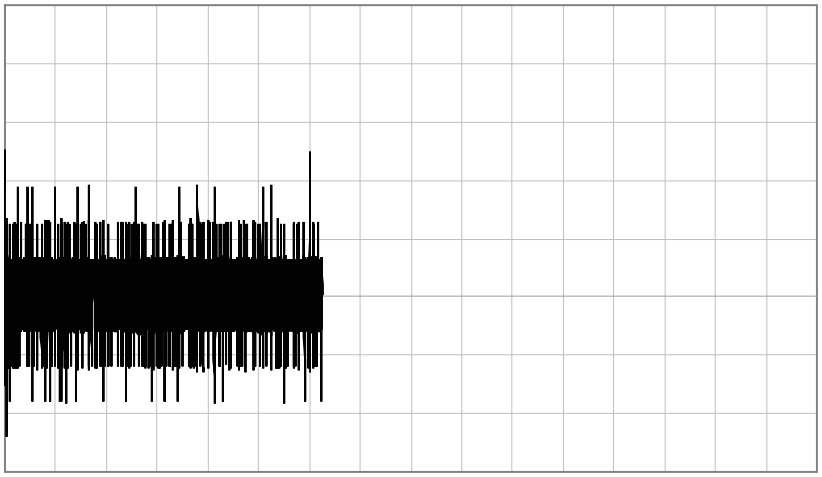


Figure 34-42. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

34.1.7 External Reset Characteristics

Figure 34-57. Minimum Reset Pin Pulse Width vs. V_{CC}

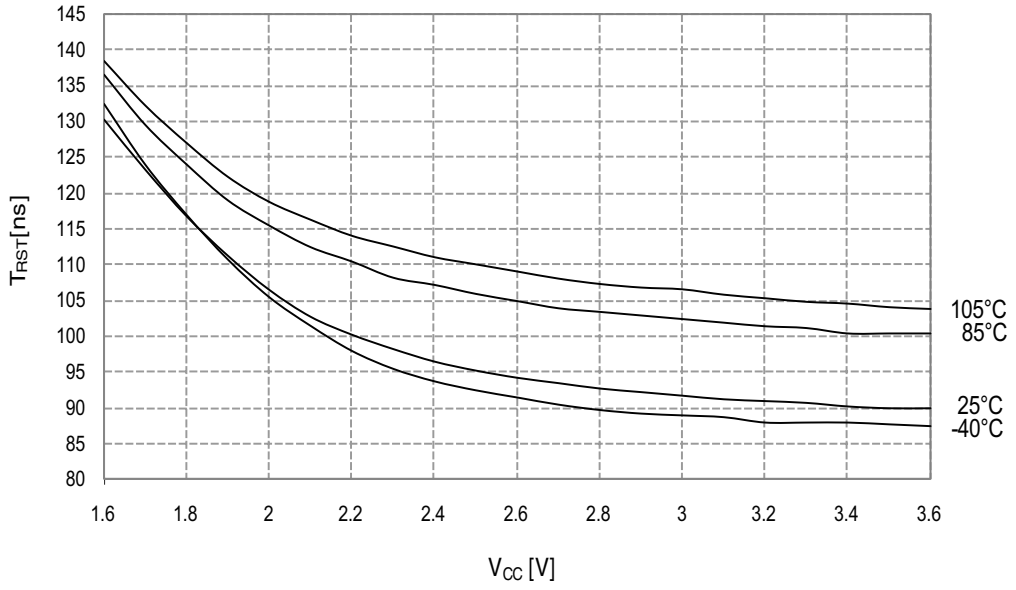


Figure 34-58. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

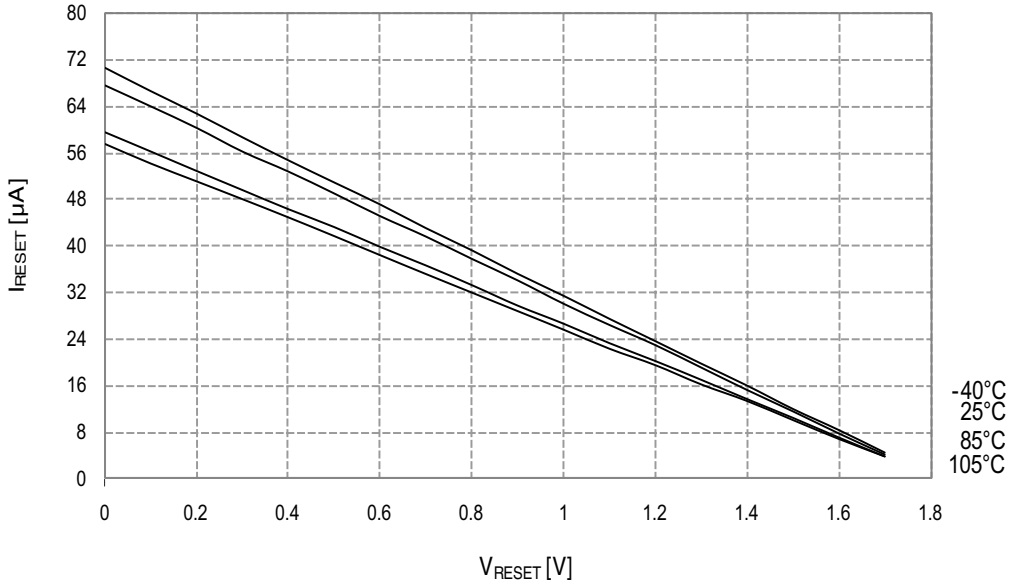
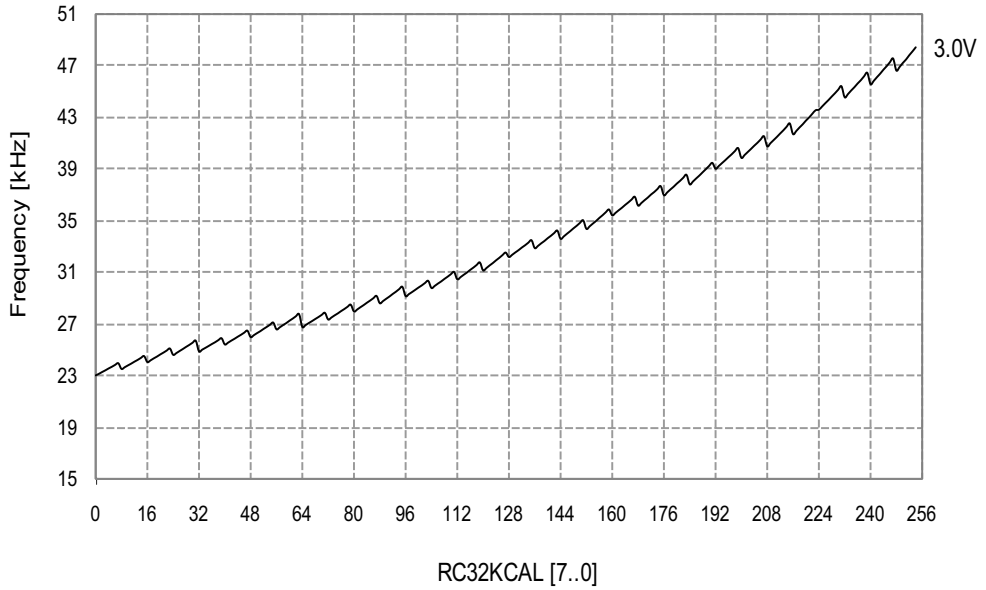


Figure 34-67. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



34.1.9.3 2MHz Internal Oscillator

Figure 34-68. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

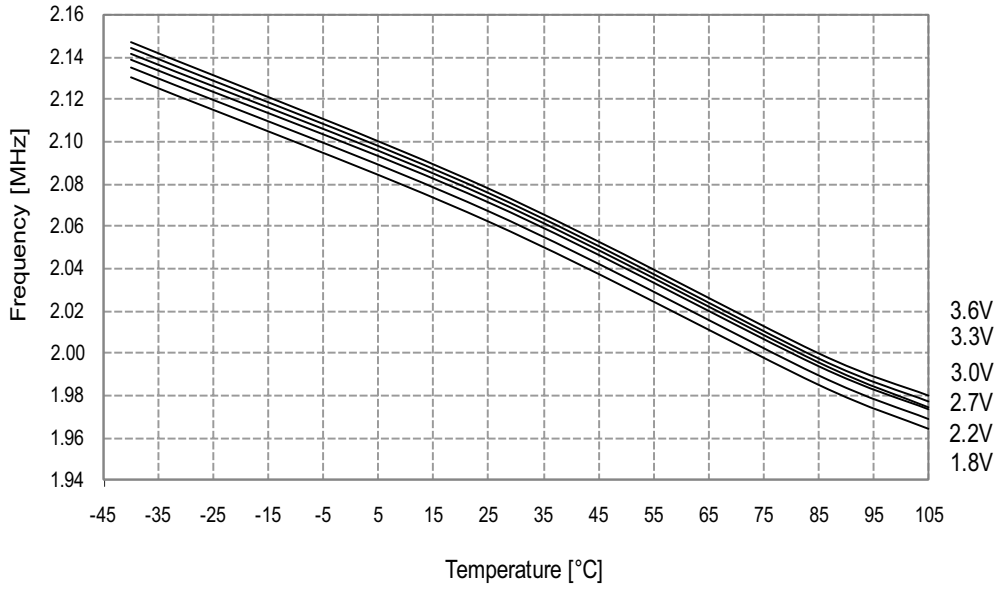


Figure 34-75. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

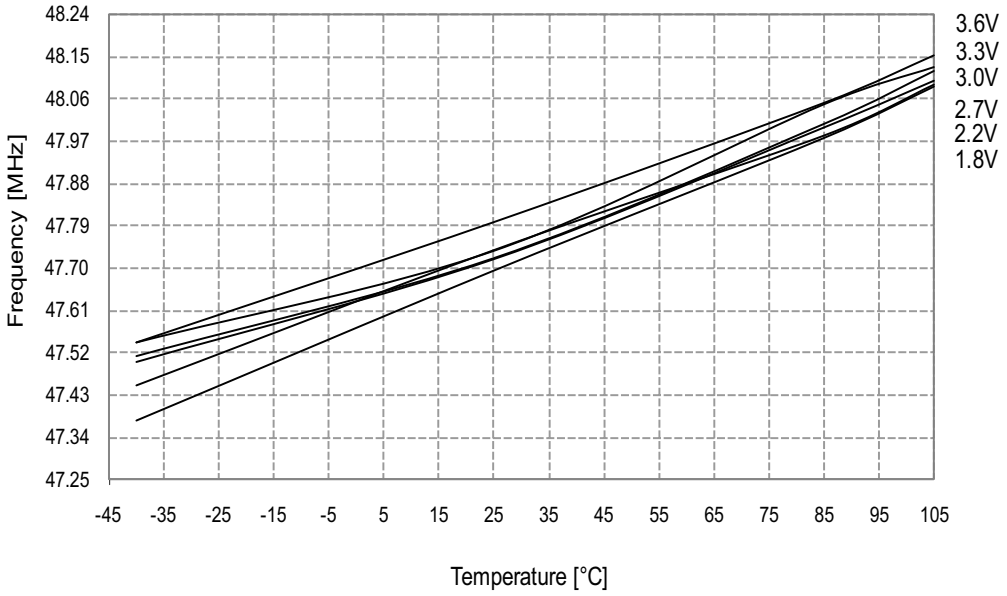
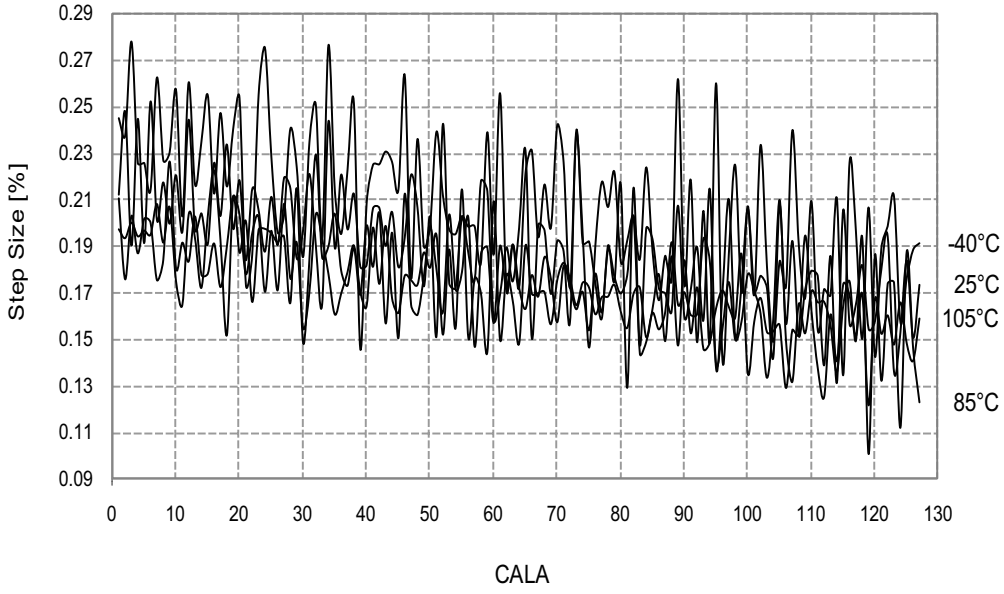


Figure 34-76. 48MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V



34.1.11 PDI Characteristics

Figure 34-79. Maximum PDI Frequency vs. V_{CC}

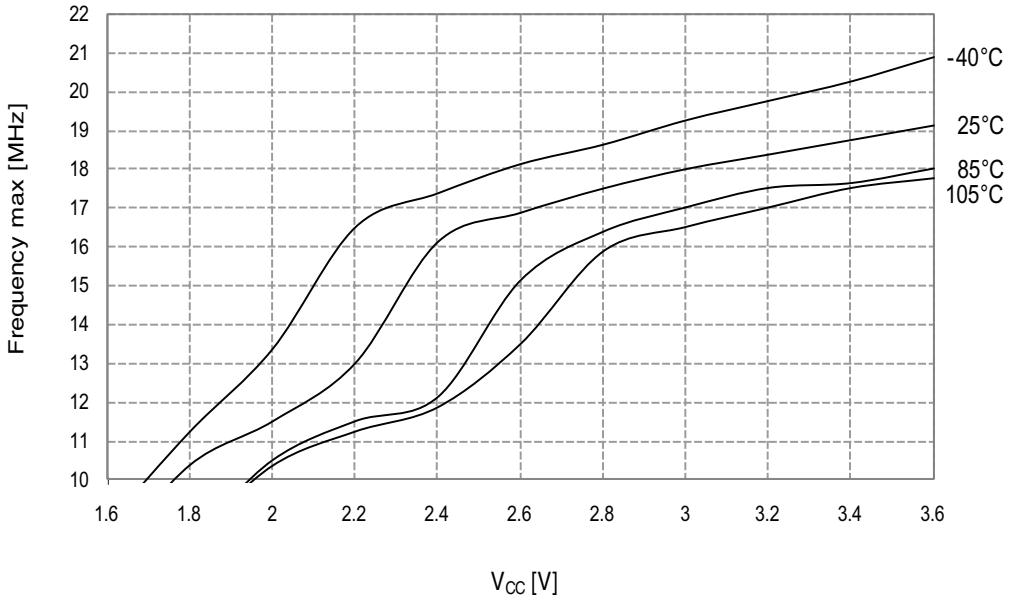


Figure 34-90. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

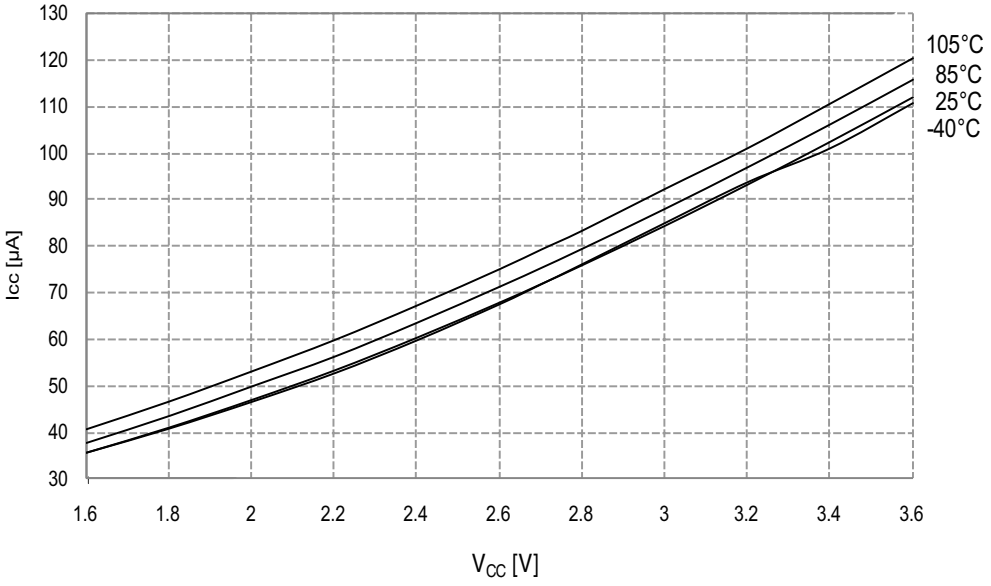


Figure 34-91. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

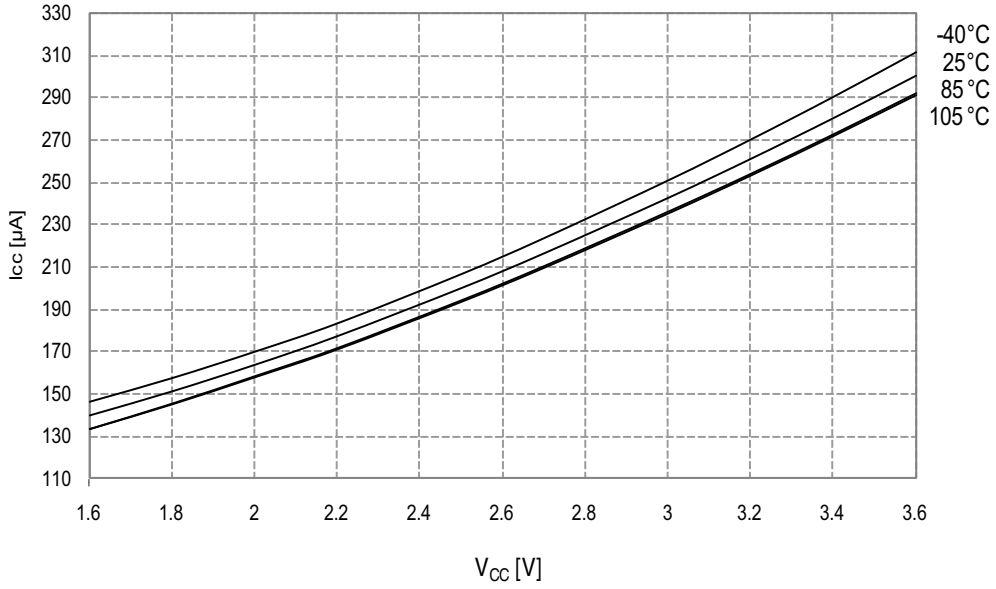
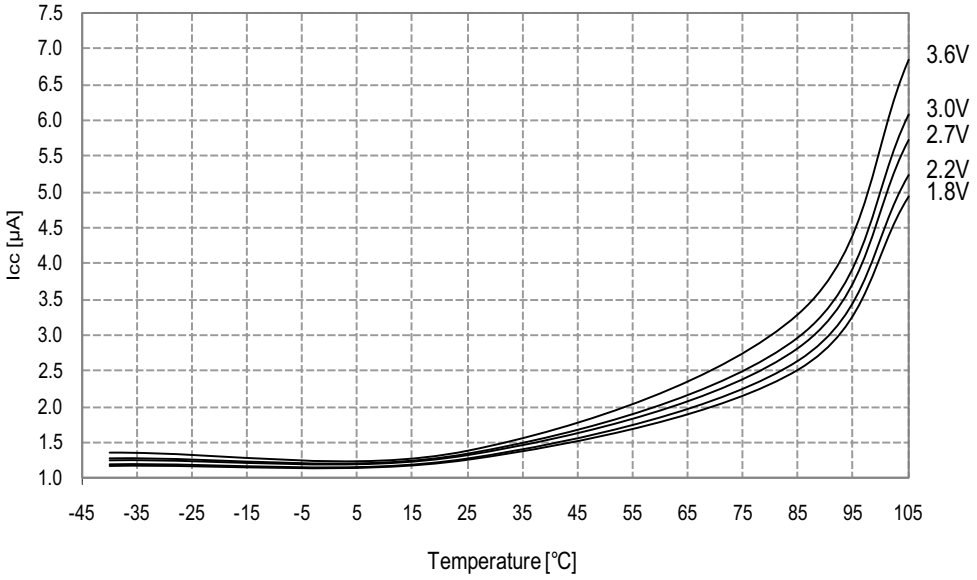


Figure 34-96. Power-down Mode Supply Current vs. Temperature

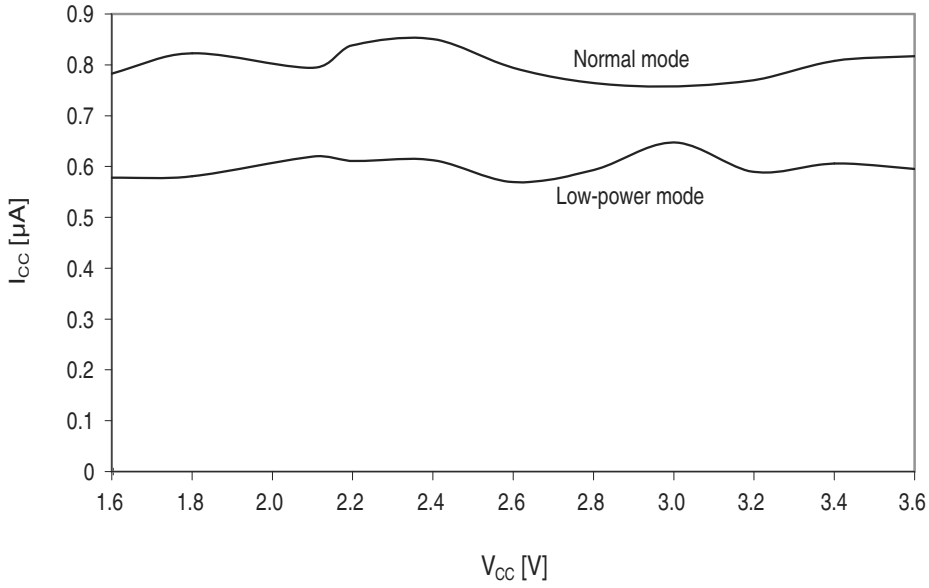
Watchdog and sampled BOD enabled and running from internal ULP oscillator



34.2.1.4 Power-save Mode Supply Current

Figure 34-97.Power-save Mode Supply Current vs.V_{CC}

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC



34.2.6 BOD Characteristics

Figure 34-134. BOD Thresholds vs. Temperature

BOD level = 1.6V

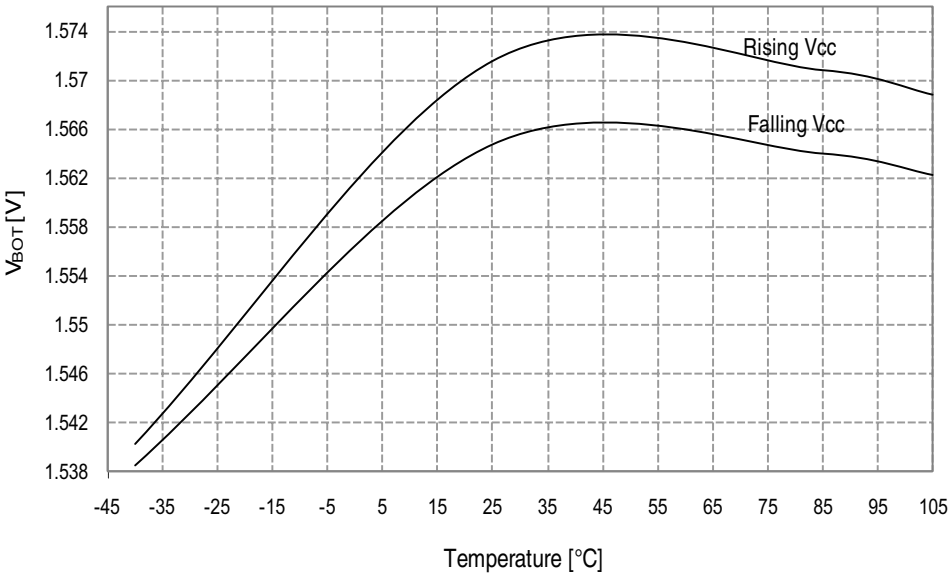
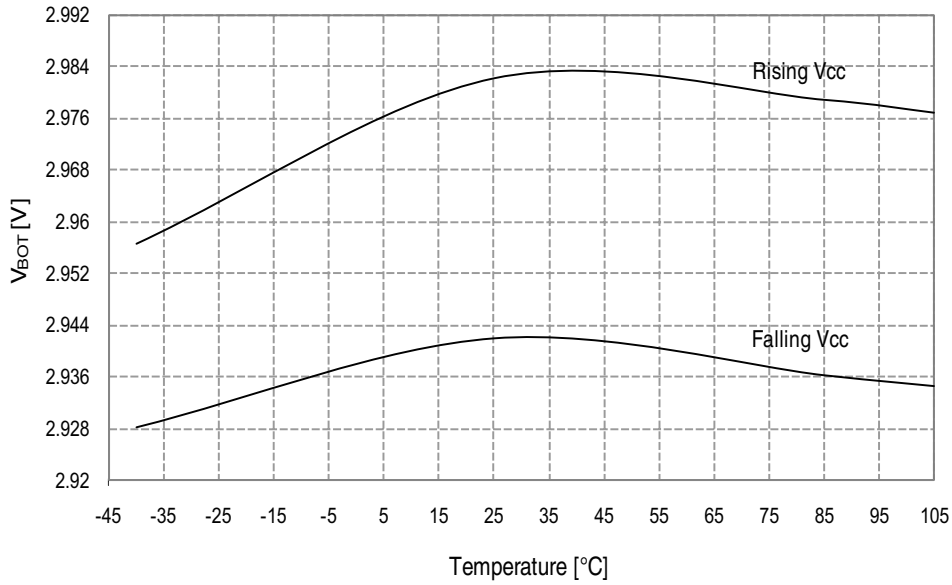


Figure 34-135. BOD Thresholds vs. Temperature

BOD level = 3.0V



36. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

36.1 8493I – 12/2014

1.	Some minor corrections according to the template.
2.	Trademark corrections.
3.	Several cross-references have been corrected.

36.2 8493H – 07/2014

1.	Updated the “Ordering Information” on page 2. Added ordering codes for ATxmega16C4/32C4 @ 105°C.
2.	Updated Table 33-4 on page 67 and Table 33-33 on page 86. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
3.	Updated Table 33-17 on page 75 and Table 33-46 on page 94. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
4.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and in Section 27.1 “Features” on page 48.
5.	Updated the typical characteristics of “Atmel ATxmega16C4” and “Atmel ATxmega32C4” with characterizations @105°C
6.	Changed V_{CC} to AV_{CC} in Section 26. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 27. “AC – Analog Comparator” on page 48.
7.	Changed values for TCCO in Table 29-3 on page 53.

36.3 8493G – 01/2014

1.	Updated the typical characteristics with characterization at 105°C.

36.4 8493F – 10/2013

1.	Updated pin locations of TOSC1 and TOSC2 in Port E - Alternate functions in Table 29-5 on page 54.
2.	Updated pin locations of XTAL1, XTAL2, TOSC1, and TOSC2 in Port R - Alternate functions in Table 29-6 on page 54.

36.5 8493E – 10/2013

1.	Updated Port C - Alternate functions in Table 29-3 on page 53.