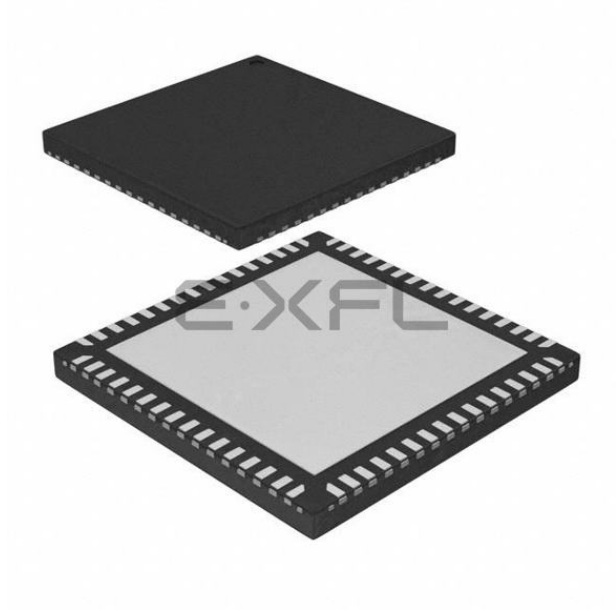

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What is "Embedded - Microcontrollers"?

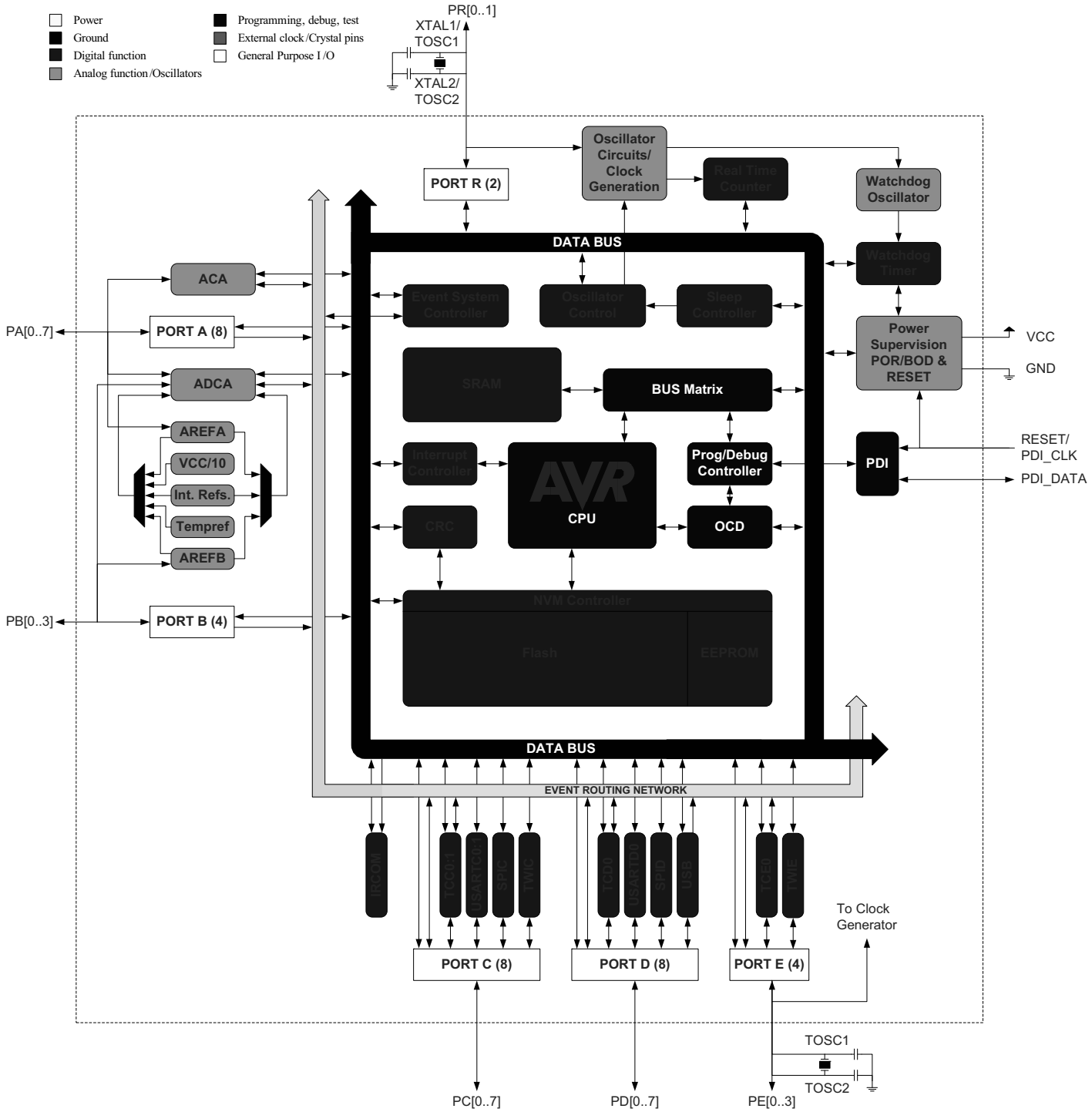
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32c4-mnr

3.1 Block Diagram

Figure 3-1. XMEGA C4 Block Diagram



13. Interrupts and Programmable Multilevel Interrupt Controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

13.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA C4 devices are shown in Table 13-1 on page 28. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA C manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1 on page 28. The program address is the word address.

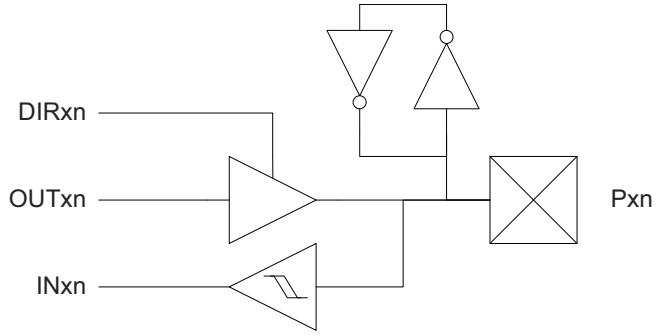
Table 13-1. Reset and Interrupt Vectors

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x056	PORTE_INT_base	Port E INT base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0FA	USB_INT_base	USB on port D Interrupt base

14.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 14-4. I/O Configuration - Totem-pole with Bus-keeper



14.3.5 Others

Figure 14-5. Output Configuration - Wired-OR with Optional Pull-down

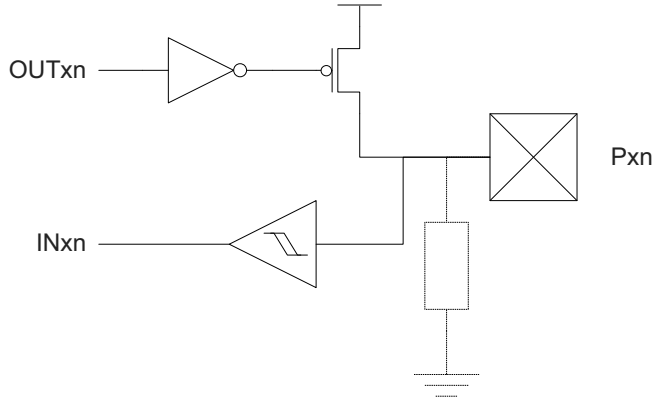
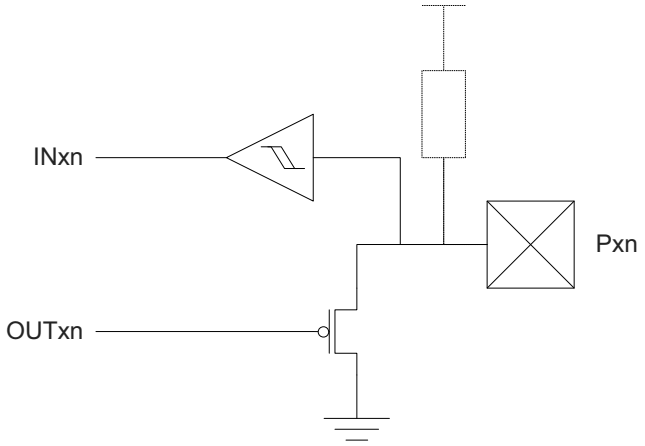


Figure 14-6. I/O Configuration - Wired-AND with Optional Pull-up



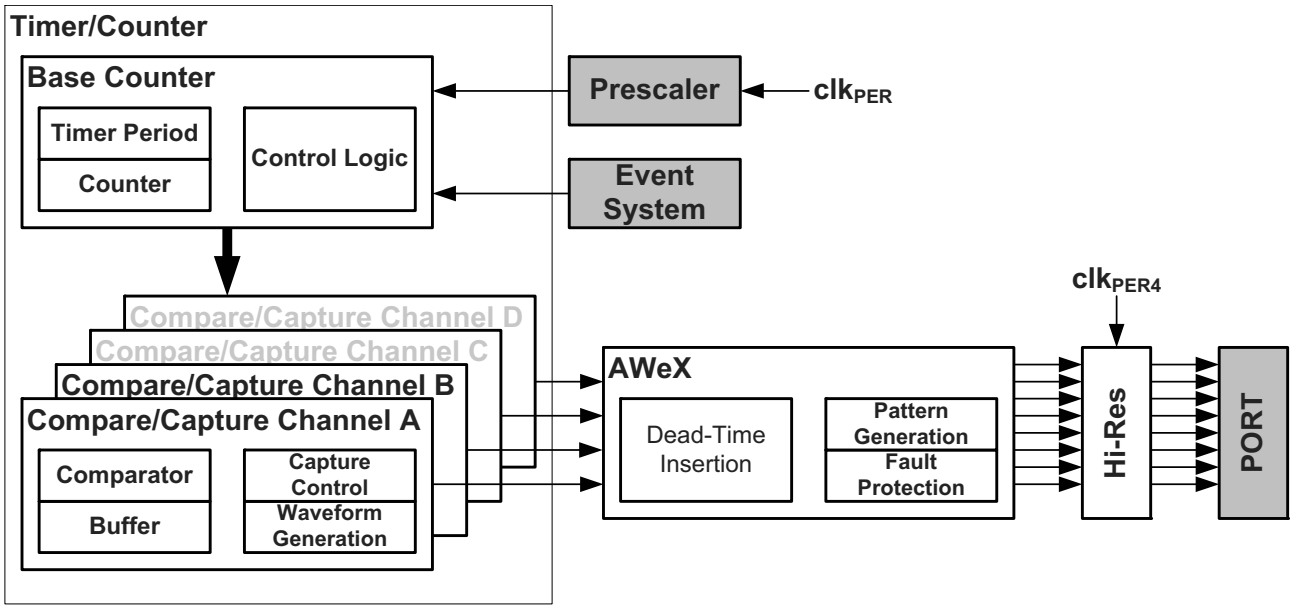
Only Timer/Counter 0 has the split mode feature that split it into two 8-bit Timer/Counters with four compare channels each.

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See “AWeX – Advanced Waveform Extension” on page 36 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 37 for more details.

Figure 15-1. Overview of a Timer/Counter and Closely Related Peripherals



PORTC has one Timer/Counter 0 and one Timer/Counter1. PORTD, and PORTE each has one timer/counter 0. Notation of these are TCC0 (time/counter C0), TCC1, TCD0, and TCE0 respectively.

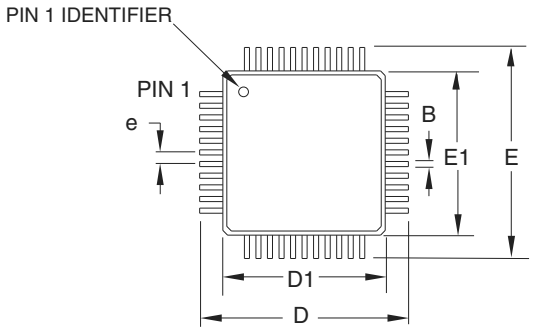
Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

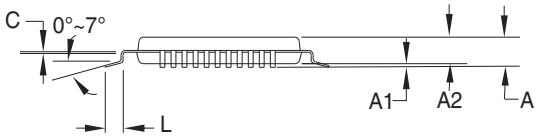
For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

32. Packaging Information

32.1 44A





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

	TITLE	DRAWING NO.	REV.
Atmel® Package Drawing Contact: packagedrawings@atmel.com	**44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)	44A	C

33.2.4 Wake-up Time from Sleep Modes

Table 33-35. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		5.0		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 33-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 33-9. Wake-up Time Definition

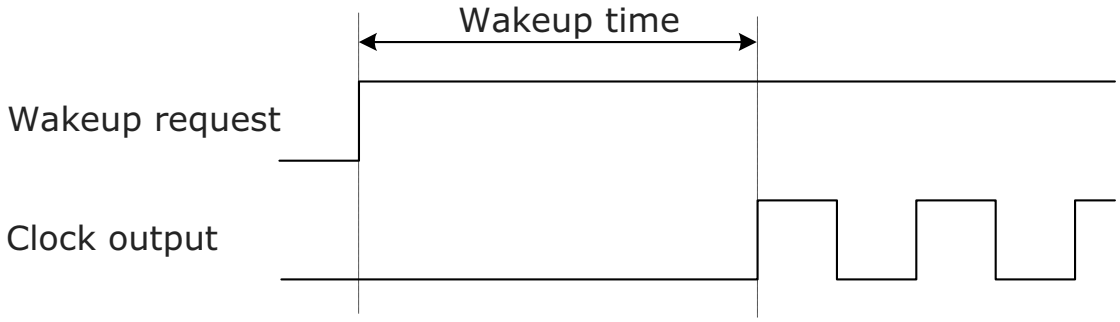


Table 33-39. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL[1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL[1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset Error	Differential mode			8		mV
			Temperature drift		0.01		mV/K
			Operating voltage drift		0.25		mV/V
	Gain Error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain Error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

33.2.8 Bandgap and Internal 1.0V Reference Characteristics

Table 33-42. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.98	1	1.02	
	Variation over voltage and temperature	Calibrated at T= 85°C, V_{CC} = 3.0V		±1.0		%

33.2.9 Brownout Detection Characteristics

Table 33-43. Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.50	1.62	1.75	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

33.2.10 External Reset Characteristics

Table 33-44. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V	0.6*V_{CC}			V
		V_{CC} = 1.6 - 2.7V	0.6*V_{CC}			
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V			0.5*V_{CC}	
		V_{CC} = 1.6 - 2.7V			0.4*V_{CC}	
R_{RST}	Reset pin pull-up resistor			25		kΩ

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, C_L=20pF		67k		
			2MHz crystal, C_L=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, C_L=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, C_L=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, C_L=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, C_L=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
R_Q	Negative impedance	XOSCPWR=1, FRQRANGE=1, C_L=20pF	9MHz crystal		1500		Ω
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, C_L=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, C_L=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, C_L=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, C_L=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, C_L=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, C_L=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, C_L=20pF		1.4		

Figure 34-11.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = MHz external clock

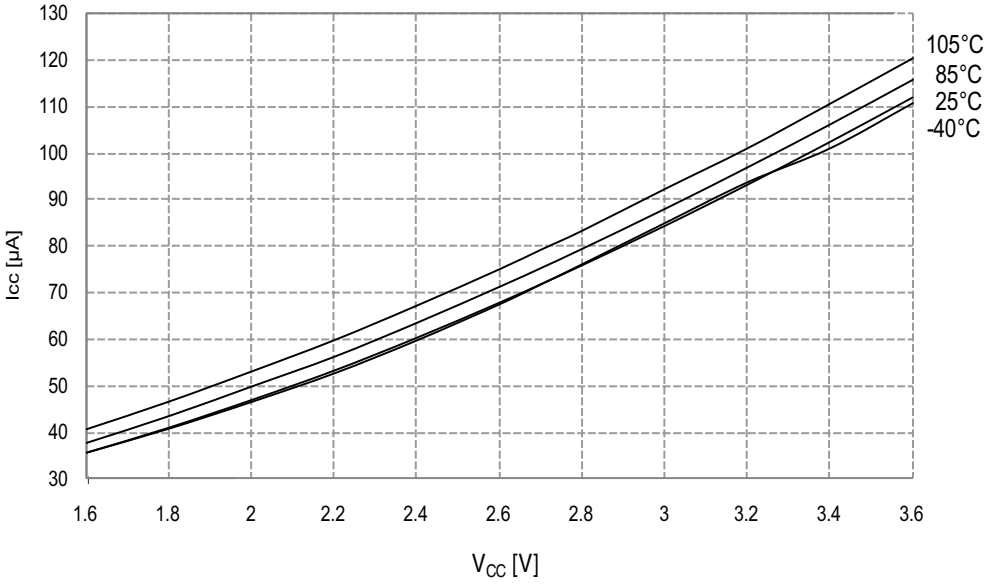


Figure 34-12.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

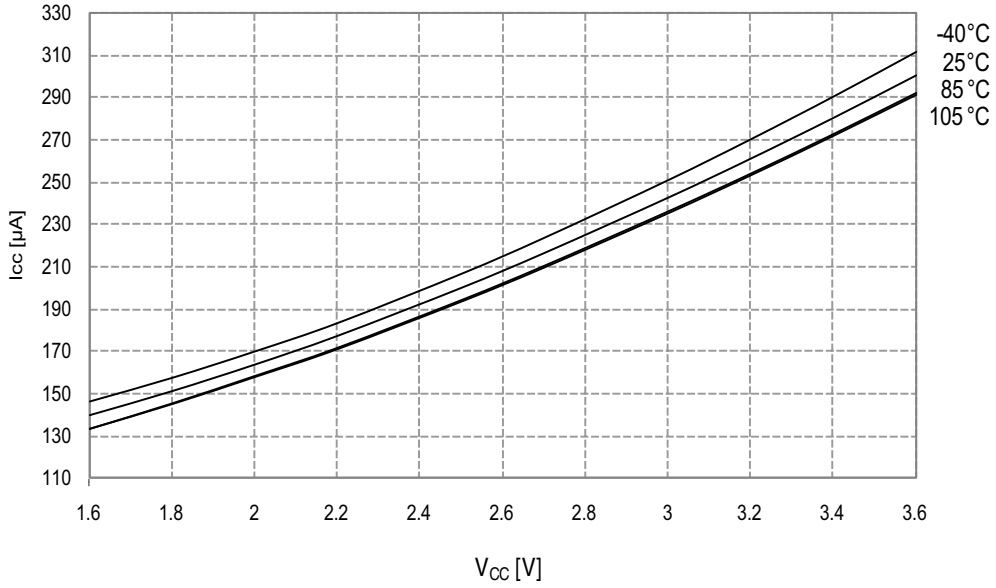
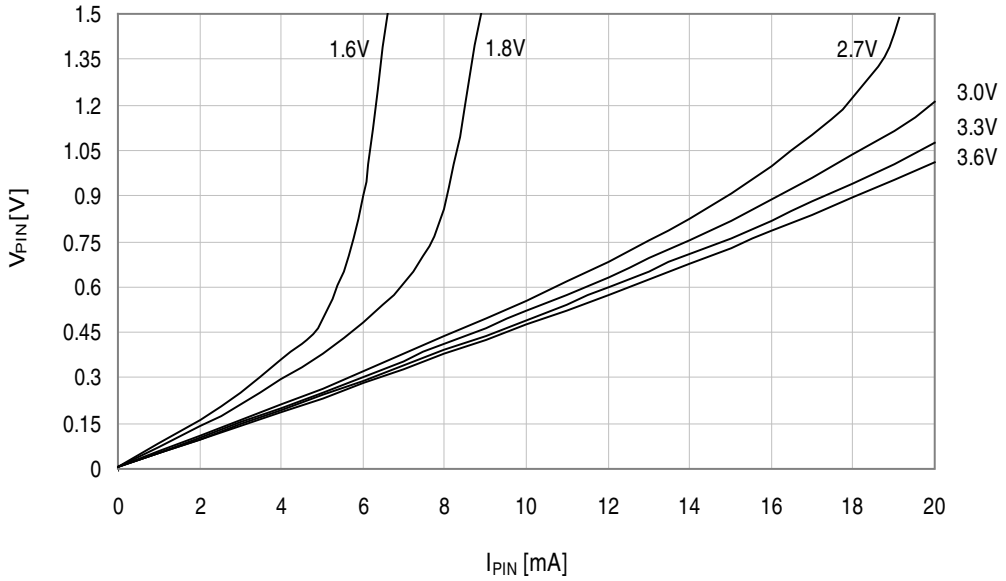


Figure 34-31. I/O Pin Output Voltage vs. Sink Current



34.1.2.3 Thresholds and Hysteresis

Figure 34-32.I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

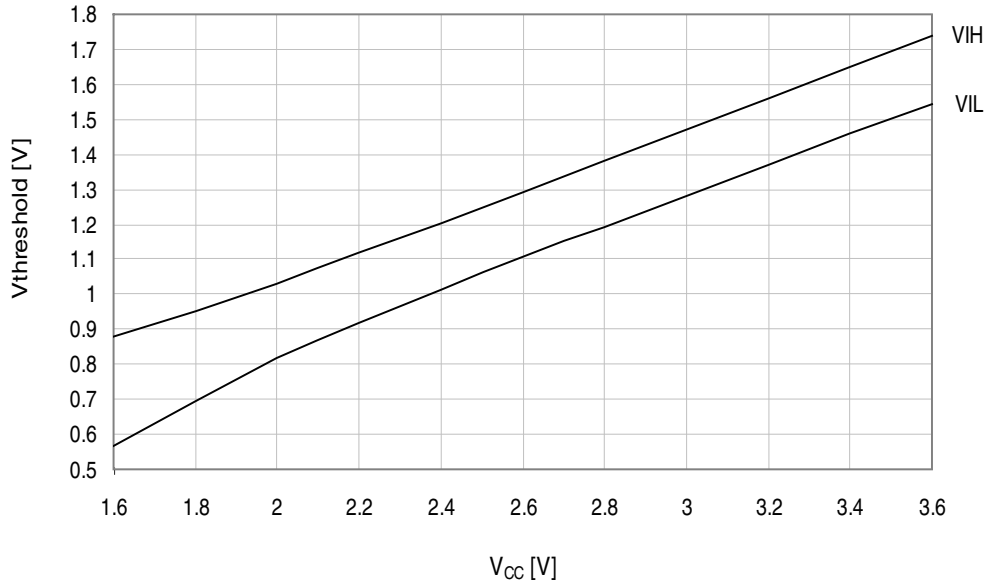


Figure 34-45. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

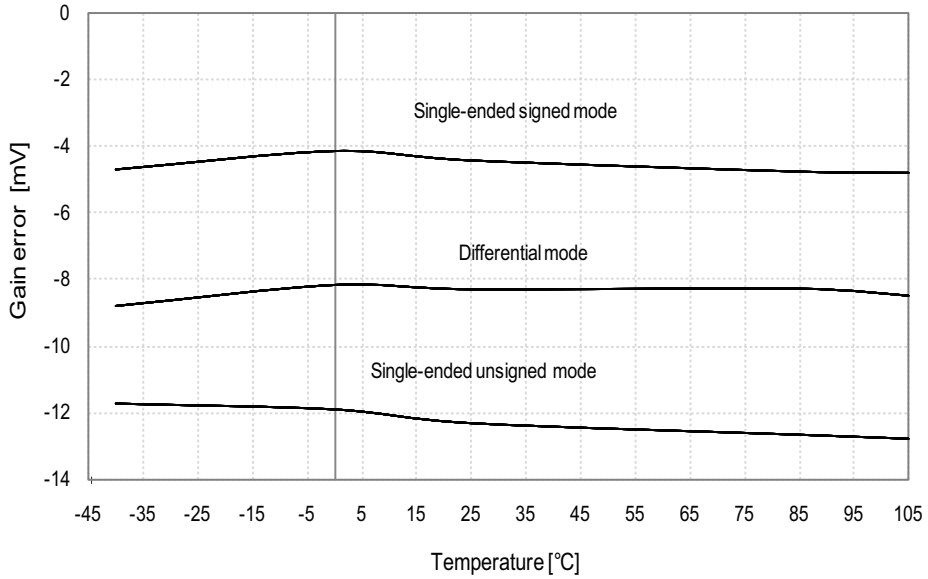


Figure 34-46. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

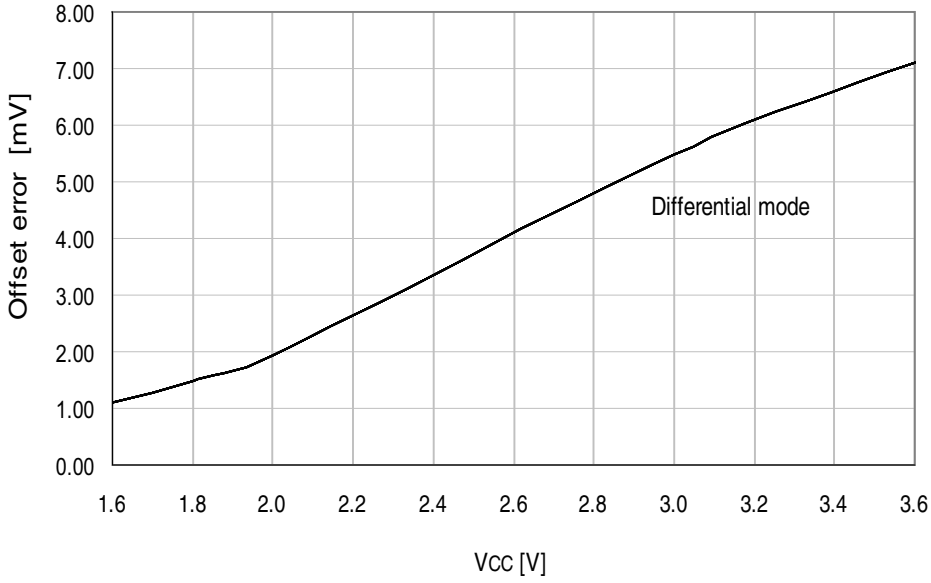


Figure 34-51. Analog Comparator Current Source vs. Calibration Value

T = 25°C

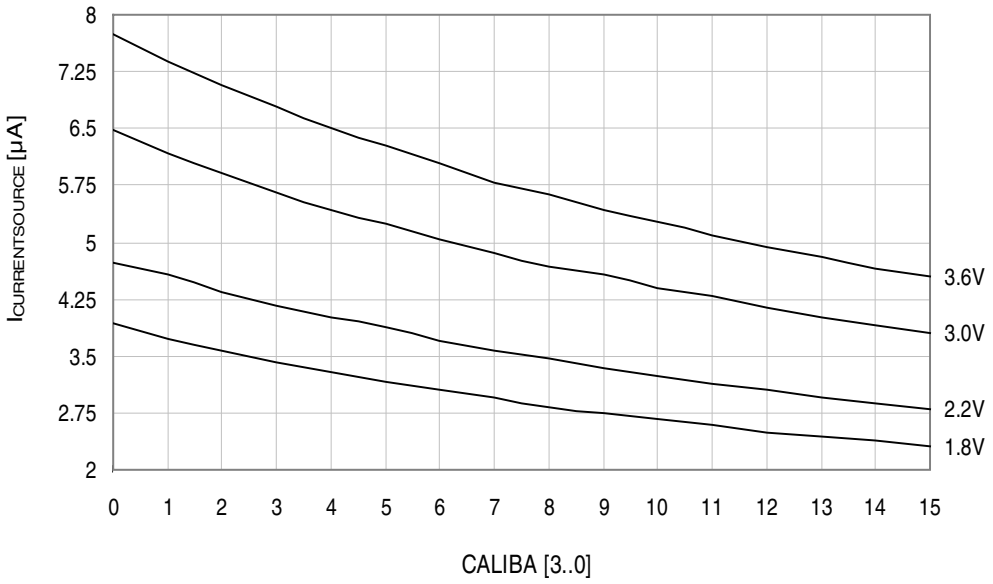
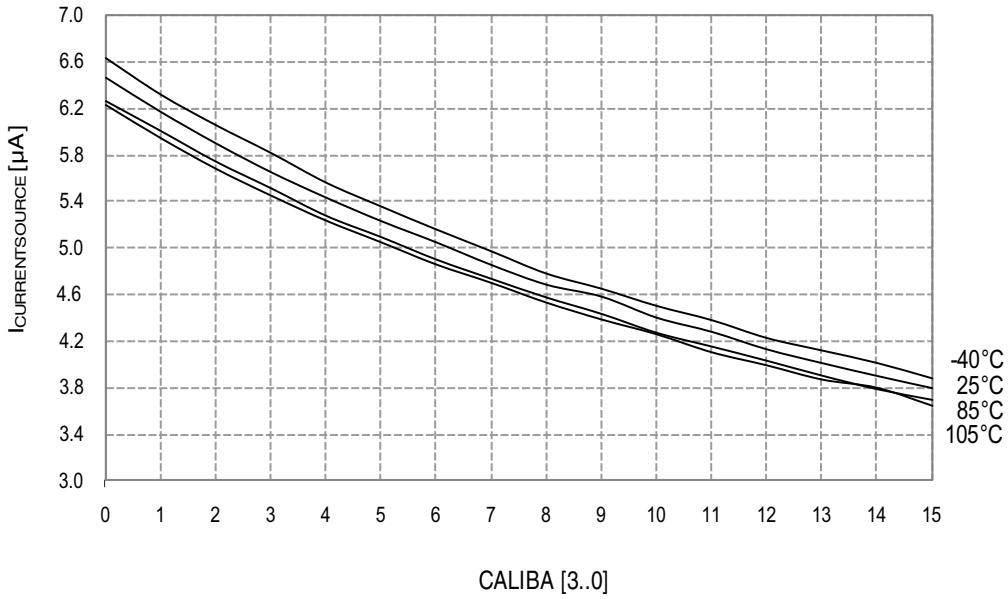


Figure 34-52. Analog Comparator Current Source vs. Calibration Value

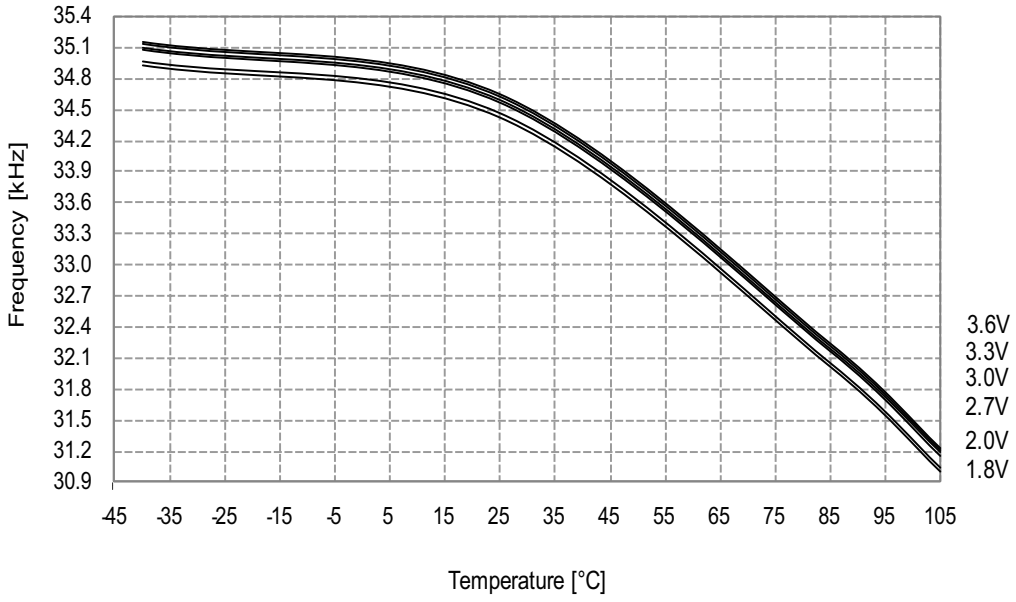
V_{CC} = 3.0V



34.1.9 Oscillator Characteristics

34.1.9.1 Ultra Low-Power Internal Oscillator

Figure 34-65.Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34.1.9.2 32.768kHz Internal Oscillator

Figure 34-66. 32.768kHz Internal Oscillator Frequency vs. Temperature

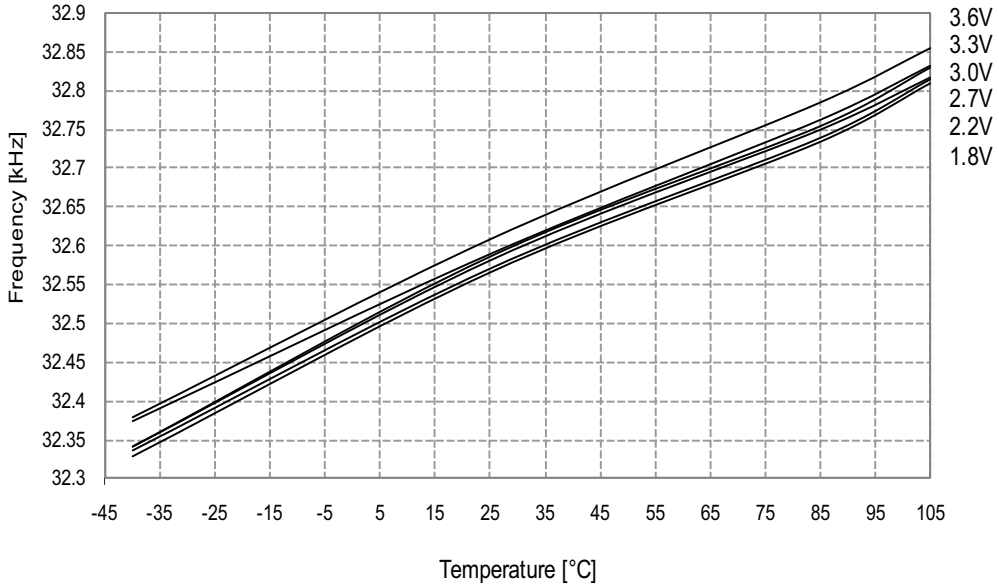


Figure 34-82. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

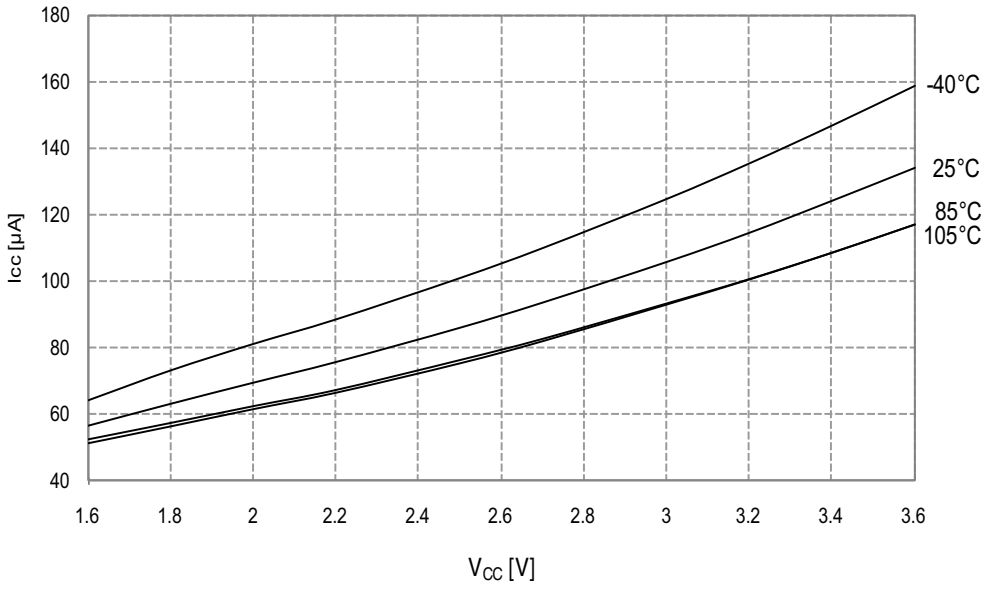


Figure 34-83. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

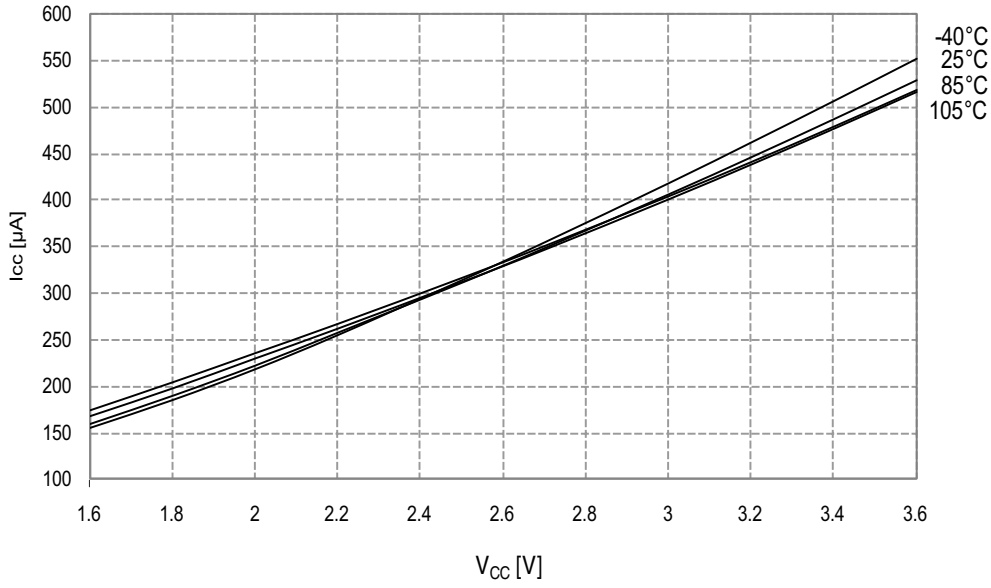
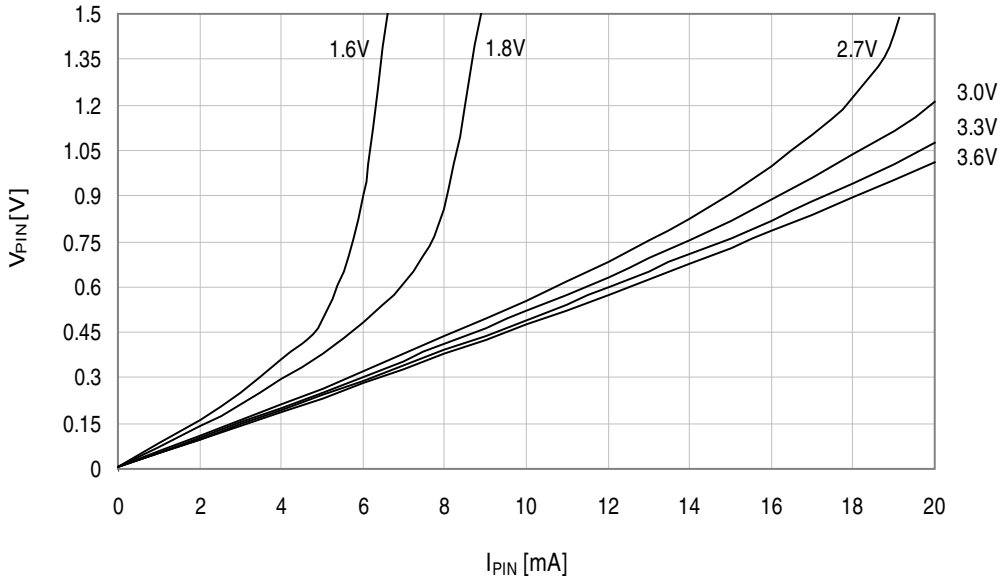


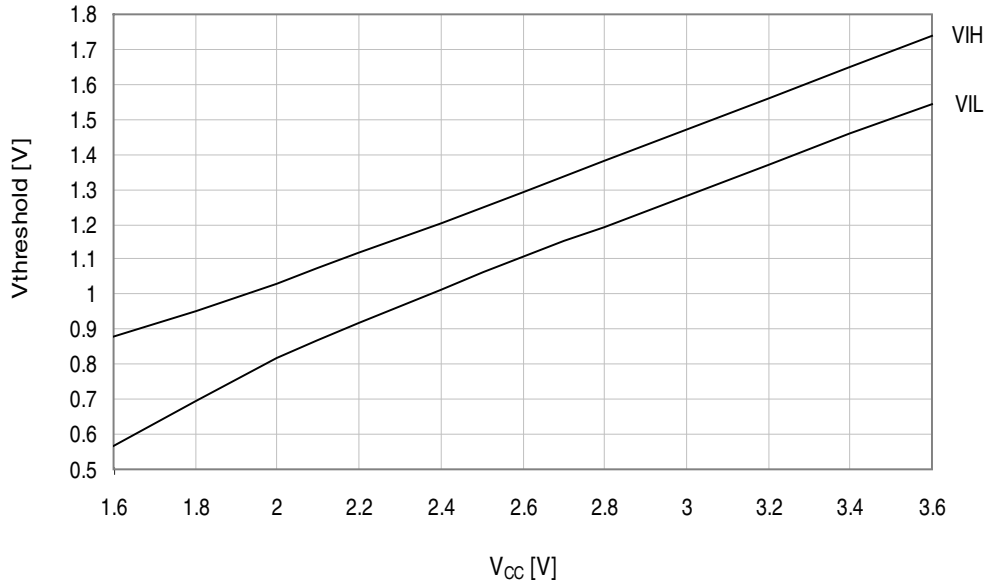
Figure 34-110. I/O Pin Output Voltage vs. Sink Current



34.2.2.3 Thresholds and Hysteresis

Figure 34-111. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C



34.2.6 BOD Characteristics

Figure 34-134. BOD Thresholds vs. Temperature

BOD level = 1.6V

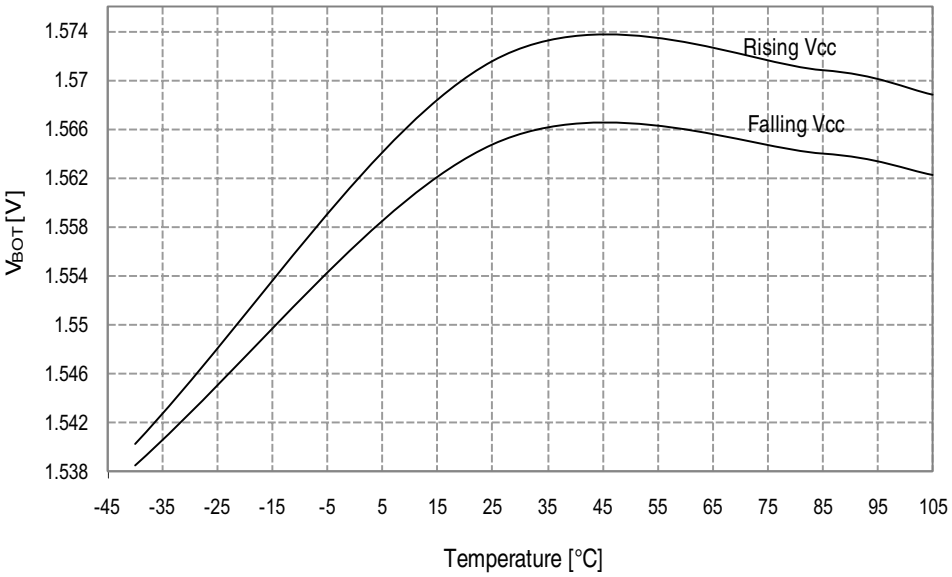
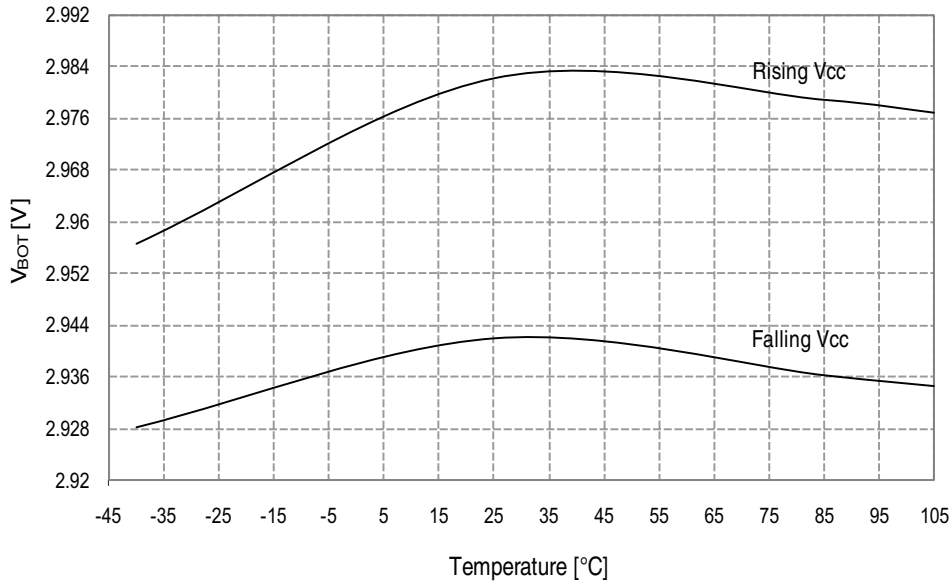


Figure 34-135. BOD Thresholds vs. Temperature

BOD level = 3.0V



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