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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	186
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k100fc256-2

...and More Features

- -1 speed grade devices are compliant with **PCI Local Bus Specification, Revision 2.2** for 5.0-V operation
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming additional device logic.
- Operate with a 2.5-V internal supply voltage
- In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay, clock skew, and clock multiplication
- Built-in, low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration
- Flexible interconnect
 - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Tri-state emulation that implements internal tri-state buses
 - Up to six global clock signals and four global clear signals
- Powerful I/O pins
 - Individual tri-state output enable control for each pin
 - Open-drain option on each I/O pin
 - Programmable output slew-rate control to reduce switching noise
 - Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
 - Supports hot-socketing

- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Flexible package options are available in 100 to 484 pins, including the innovative FineLine BGA™ packages (see [Tables 2 and 3](#))
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplcity, VeriBest, and Viewlogic

Table 2. ACEX 1K Package Options & I/O Pin Count *Notes (1), (2)*

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	66	92	120	136	136 (3)
EP1K30		102	147	171	171 (3)
EP1K50		102	147	186	249
EP1K100			147	186	333

Notes:

- (1) ACEX 1K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and FineLine BGA packages.
- (2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
- (3) This option is supported with a 256-pin FineLine BGA package. By using SameFrame™ pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin and 484-pin FineLine BGA packages.

Table 3. ACEX 1K Package Sizes

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.0
Area (mm ²)	256	484	936	289	529
Length × width (mm × mm)	16 × 16	22 × 22	30.6 × 30.6	17 × 17	23 × 23

General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

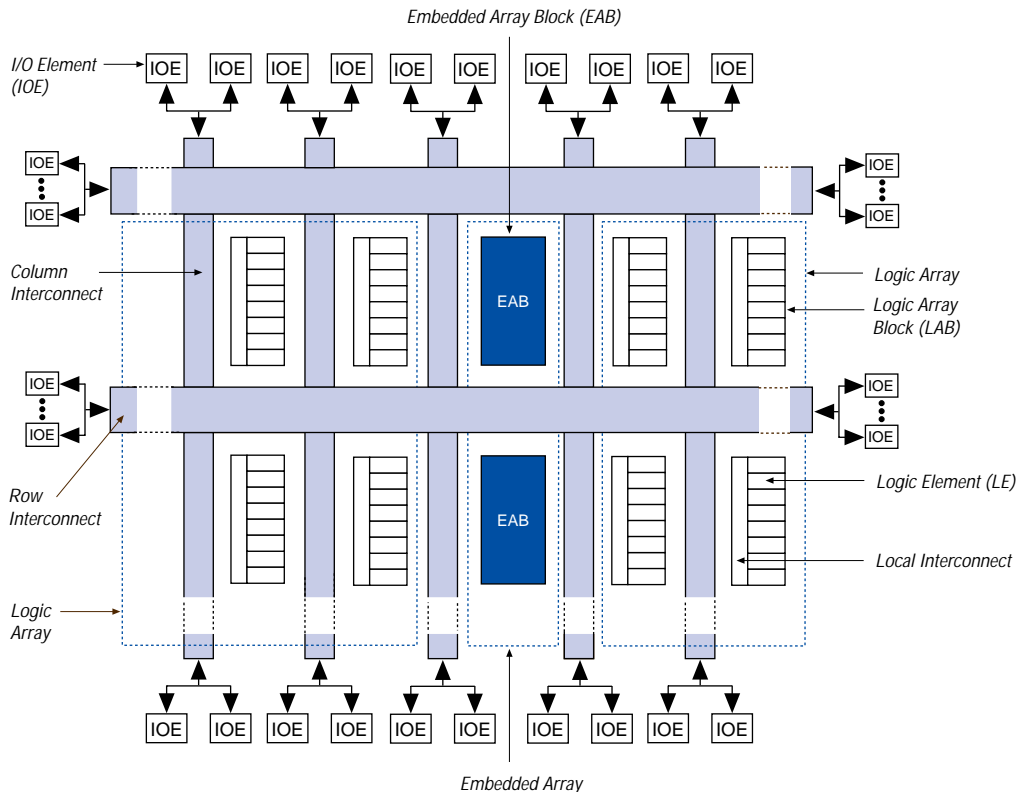
Table 4. ACEX 1K Device Performance

Application	Resources Used		Performance			
	LEs	EABs	Speed Grade			Units
			-1	-2	-3	
16-bit loadable counter	16	0	285	232	185	MHz
16-bit accumulator	16	0	285	232	185	MHz
16-to-1 multiplexer (1)	10	0	3.5	4.5	6.6	ns
16-bit multiplier with 3-stage pipeline (2)	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed (2)	0	1	278	196	143	MHz
256 × 16 RAM write cycle speed (2)	0	1	185	143	111	MHz

Notes:

- (1) This application uses combinatorial inputs and outputs.
- (2) This application uses registered inputs and outputs.

Figure 1. ACEX 1K Device Block Diagram

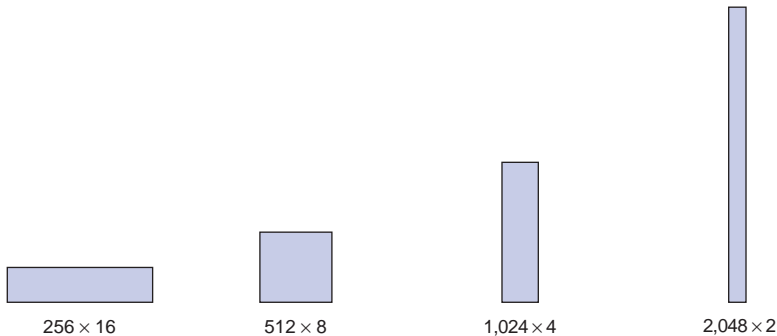


ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

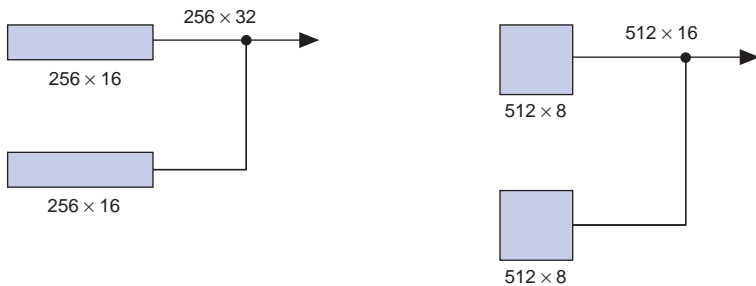
When used as RAM, each EAB can be configured in any of the following sizes: 256×16 ; 512×8 ; $1,024 \times 4$; or $2,048 \times 2$. Figure 5 shows the ACEX 1K EAB memory configurations.

Figure 5. ACEX 1K EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256×16 RAM blocks can be combined to form a 256×32 block, and two 512×8 RAM blocks can be combined to form a 512×16 block. Figure 6 shows examples of multiple EAB combination.

Figure 6. Examples of Combining ACEX 1K EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera software automatically combines EABs to meet a designer's RAM specifications.

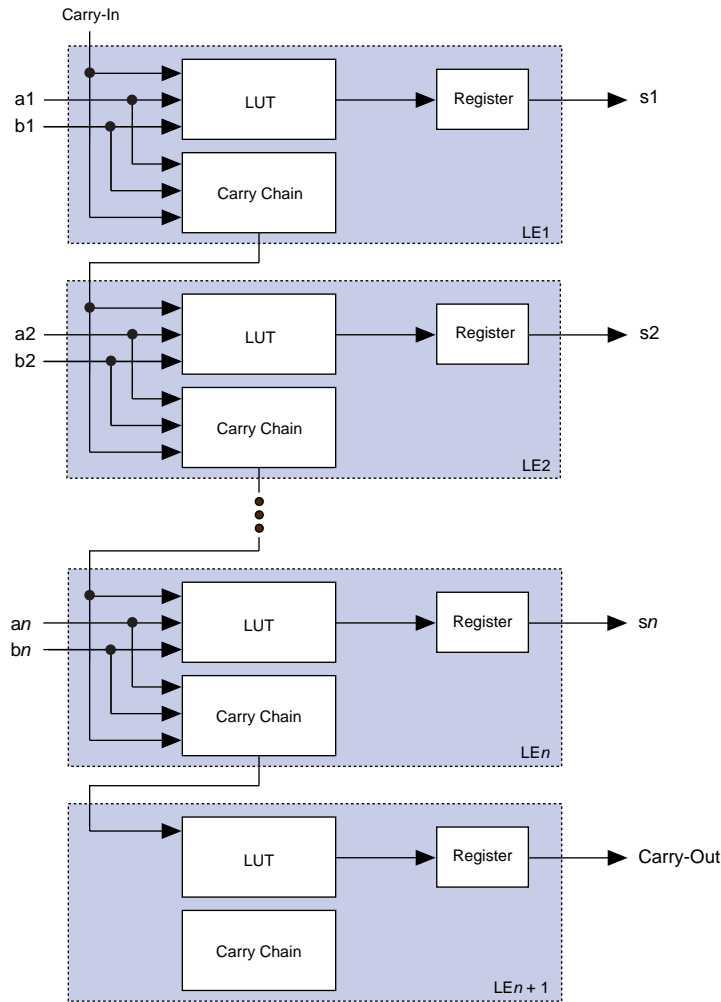
EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write-enable, read-enable, and clock-enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write-enable, read-enable, clear, clock, and clock-enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see [Figures 2 and 4](#)). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the ACEX 1K architecture, facilitating efficient routing with optimum device utilization and high performance. [Figure 7](#) shows the ACEX 1K LAB.

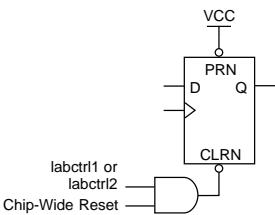
Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)



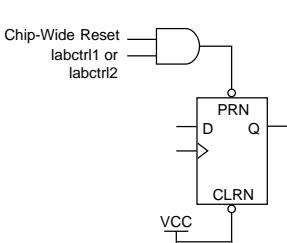
In addition to the six clear and preset modes, ACEX 1K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. ACEX 1K LE Clear & Preset Modes

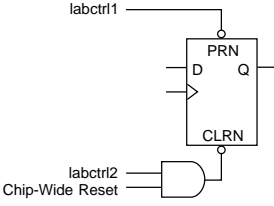
Asynchronous Clear



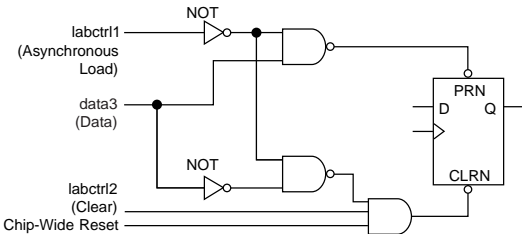
Asynchronous Preset



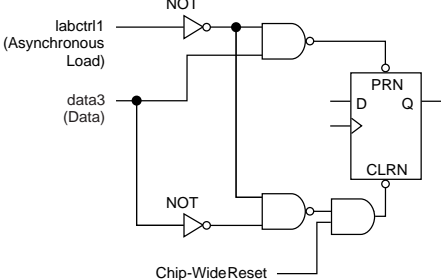
Asynchronous Preset & Clear



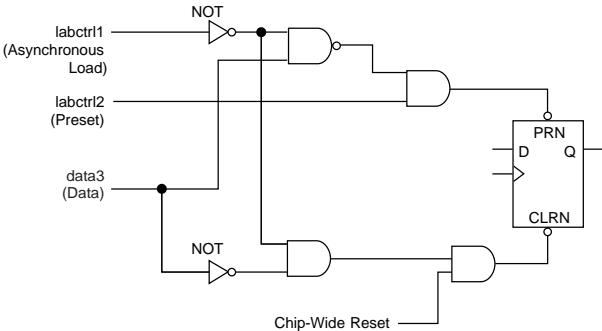
Asynchronous Load with Clear



Asynchronous Load without Clear or Preset



Asynchronous Load with Preset



For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 6 summarizes the FastTrack Interconnect routing structure resources available in each ACEX 1K device.

<i>Table 6. ACEX 1K FastTrack Interconnect Resources</i>				
Device	Rows	Channels per Row	Columns	Channels per Column
EP1K10	3	144	24	24
EP1K30	6	216	36	24
EP1K50	10	216	36	24
EP1K100	12	312	52	24

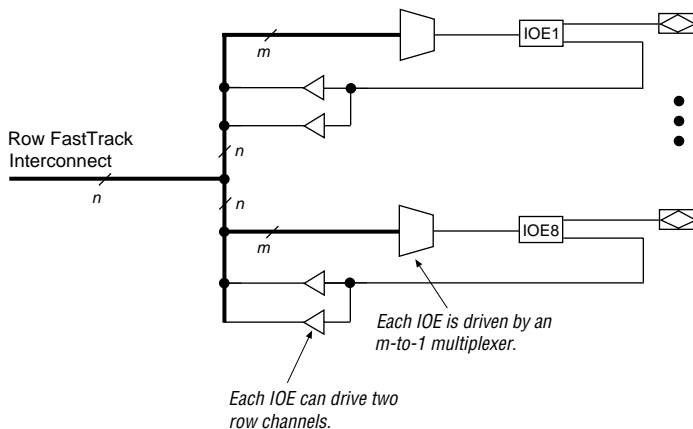
In addition to general-purpose I/O pins, ACEX 1K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output-enable and clock-enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. ACEX 1K Row-to-IOE Connections *Note (1)*



Note:

(1) The values for m and n are shown in Table 8.

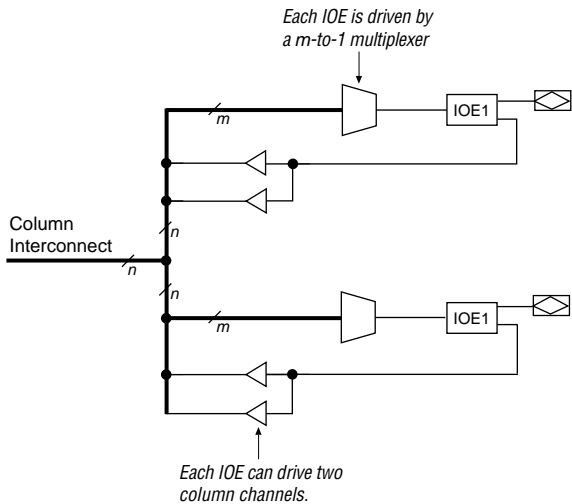
Table 8 lists the ACEX 1K row-to-IOE interconnect resources.

Table 8. ACEX 1K Row-to-IOE Interconnect Resources		
Device	Channels per Row (n)	Row Channels per Pin (m)
EP1K10	144	18
EP1K30	216	27
EP1K50	216	27
EP1K100	312	39

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see [Figure 17](#)).

Figure 17. ACEX 1K Column-to-IOE Connections Note (1)



Note:

- (1) The values for m and n are shown in [Table 9](#).

[Table 9](#) lists the ACEX 1K column-to-IOE interconnect resources.

Table 9. ACEX 1K Column-to-IOE Interconnect Resources		
Device	Channels per Column (n)	Column Channels per Pin (m)
EP1K10	24	16
EP1K30	24	16
EP1K50	24	16
EP1K100	24	16



For more information, search for “SameFrame” in MAX+PLUS II Help.

Table 10. ACEX 1K SameFrame Pin-Out Support		
Device	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	✓	(1)
EP1K30	✓	(1)
EP1K50	✓	✓
EP1K100	✓	✓

Note:
(1) This option is supported with a 256-pin FineLine BGA package and SameFrame migration.

ClockLock &
ClockBoost
Features

To support high-speed designs, -1 and -2 speed grade ACEX 1K devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in ACEX 1K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry lock onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

Table 16. 32-Bit IDCODE for ACEX 1K Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) <i>(2)</i>
EP1K10	0001	0001 0000 0001 0000	000011011110	1
EP1K30	0001	0001 0000 0011 0000	000011011110	1
EP1K50	0001	0001 0000 0101 0000	000011011110	1
EP1K100	0010	0000 0001 0000 0000	000011011110	1

Notes to tables:

- (1) The most significant bit (MSB) is on the left.
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

ACEX 1K devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

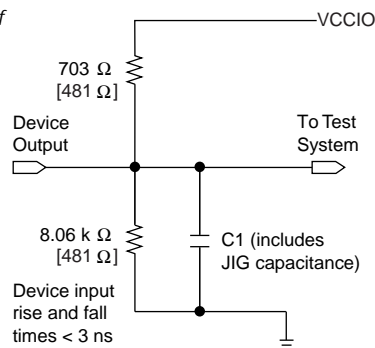
Figure 20 shows the timing requirements for the JTAG signals.

Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in [Figure 21](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. ACEX 1K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



Operating Conditions

[Tables 18](#) through [21](#) provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

Table 18. ACEX 1K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I			–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	°C

Table 24. EAB Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABRE1}	Read enable delay to EAB for combinatorial input	
t_{EABRE2}	Read enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCLR}	EAB register asynchronous clear time to output delay	
t_{AA}	Address access delay (including the read enable to output delay)	
t_{WP}	Write pulse width	
t_{RP}	Read pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	(5)
t_{WDH}	Data hold time after falling edge of write pulse	(5)
t_{WASU}	Address setup time before rising edge of write pulse	(5)
t_{WAH}	Address hold time after falling edge of write pulse	(5)
t_{RASU}	Address setup time before rising edge of read pulse	
t_{RAH}	Address hold time after falling edge of read pulse	
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	

Table 39. EP1K30 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
t_{EABWE1}		1.1		1.3		1.4	ns
t_{EABWE2}		0.4		0.4		0.5	ns
t_{EABRE1}		0.8		0.9		1.0	ns
t_{EABRE2}		0.4		0.4		0.5	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.4	ns
$t_{EABYPASS}$		0.5		0.6		0.7	ns
t_{EABSU}	0.9		1.0		1.2		ns
t_{EABH}	0.4		0.4		0.5		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.2		3.8		4.4	ns
t_{WP}	2.5		2.9		3.3		ns
t_{RP}	0.9		1.1		1.2		ns
t_{WDSU}	0.9		1.0		1.1		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.7		2.0		2.3		ns
t_{WAH}	1.8		2.1		2.4		ns
t_{RASU}	3.1		3.7		4.2		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.5		2.9		3.3	ns
t_{DD}		2.5		2.9		3.3	ns
t_{EABOUT}		0.5		0.6		0.7	ns
t_{EABCH}	1.5		2.0		2.3		ns
t_{EABCL}	2.5		2.9		3.3		ns

Table 52. EP1K100 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.7		2.0		2.6	ns
t_{IOC}		0.0		0.0		0.0	ns
t_{IOCO}		1.4		1.6		2.1	ns
t_{IOCOMB}		0.5		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.7		0.9		1.2		ns
t_{IOCLR}		0.5		0.7		0.9	ns
t_{OD1}		3.0		4.2		5.6	ns
t_{OD2}		3.0		4.2		5.6	ns
t_{OD3}		4.0		5.5		7.3	ns
t_{XZ}		3.5		4.6		6.1	ns
t_{ZX1}		3.5		4.6		6.1	ns
t_{ZX2}		3.5		4.6		6.1	ns
t_{ZX3}		4.5		5.9		7.8	ns
t_{INREG}		2.0		2.6		3.5	ns
t_{IOFD}		0.5		0.8		1.2	ns
t_{INCOMB}		0.5		0.8		1.2	ns

Table 53. EP1K100 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA1}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.1		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.1		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow ACEX 1K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, re-initializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 40 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an ACEX 1K device can be loaded with one of five configuration schemes (see Table 59), chosen on the basis of the target application. An EPC16, EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a ACEX 1K device, allowing automatic configuration on system power-up.

Multiple ACEX 1K devices can be configured in any of the five configuration schemes by connecting the configuration enable (*nCE*) and configuration enable output (*nCEO*) pins on each device. Additional APEX 20K, APEX 20KE, FLEX 10K, FLEX 10KA, FLEX 10KE, ACEX 1K, and FLEX 6000 devices can be configured in the same serial chain.

Table 59. Data Sources for ACEX 1K Configuration	
Configuration Scheme	Data Source
Configuration device	EPC16, EPC2, EPC1, or EPC1441 configuration device
Passive serial (PS)	BitBlaster or ByteBlasterMV download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL File or JBC File

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Documentation Library* for pin-out information.



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