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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	333
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k100fc484-2ngz

Figure 1. ACEX 1K Device Block Diagram
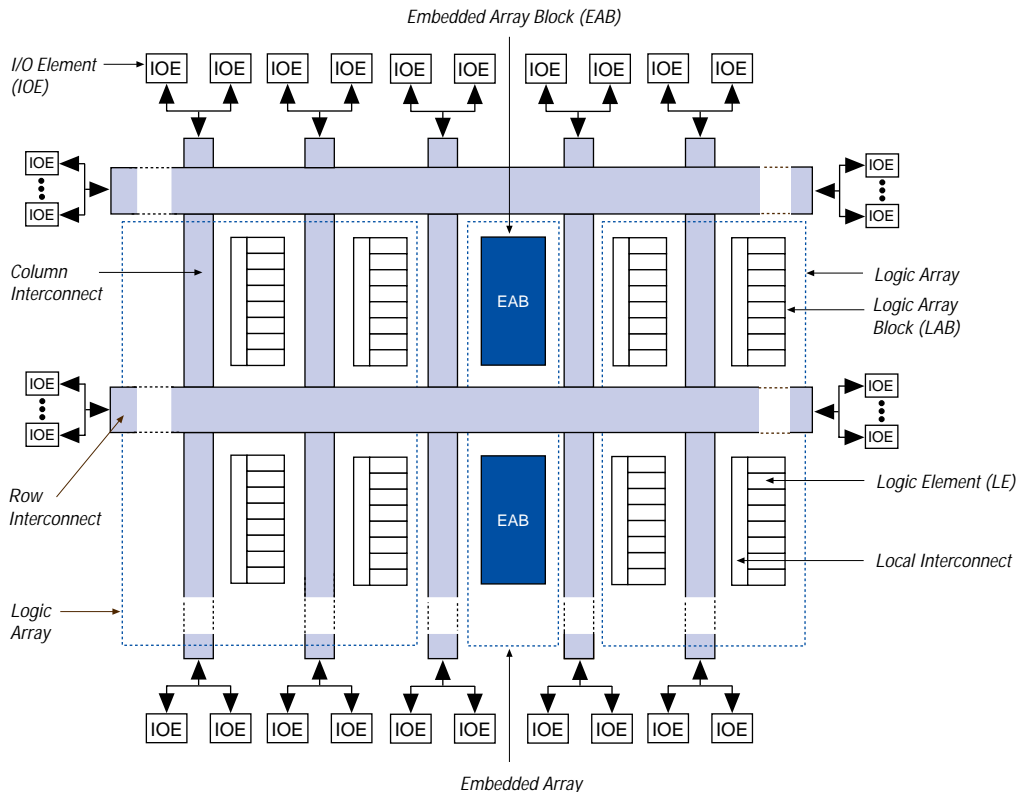
ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Figure 2. ACEX 1K Device in Dual-Port RAM Mode   *Note (1)*
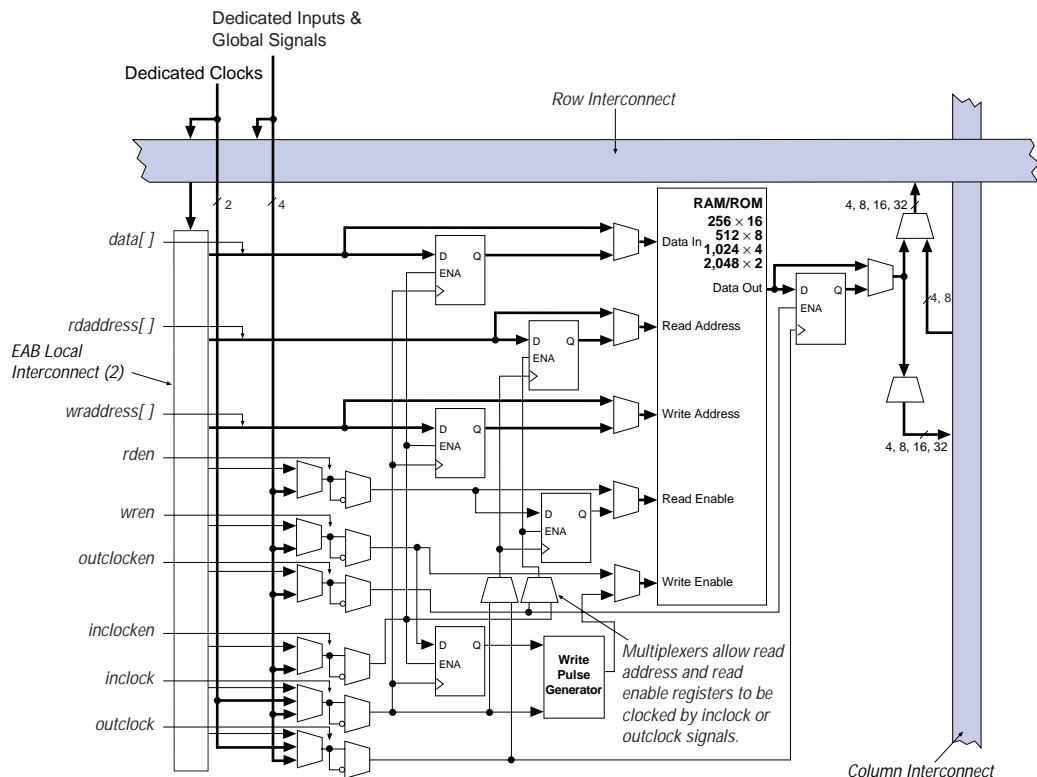
Notes:
(1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
(2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

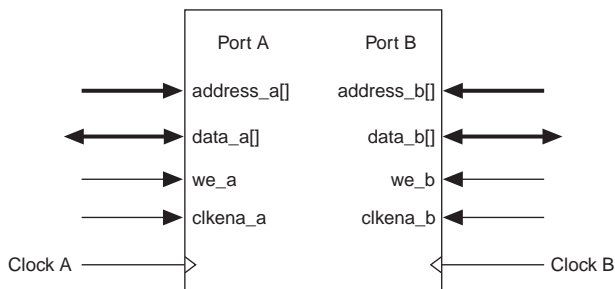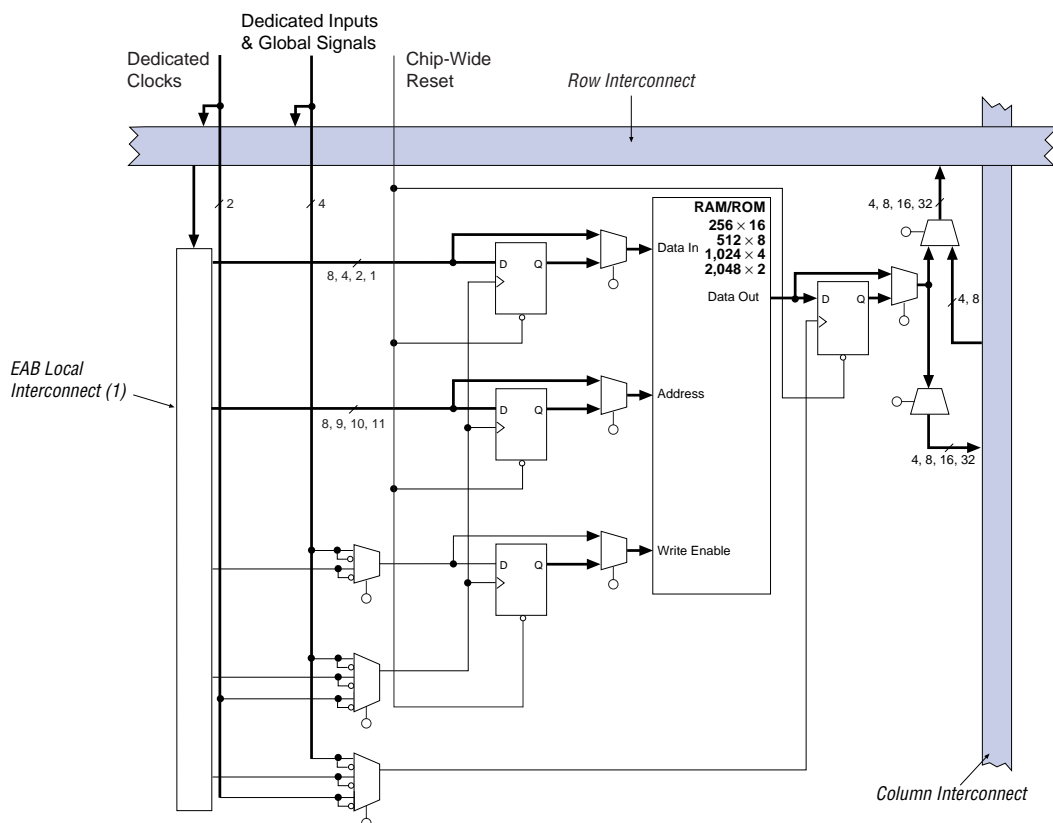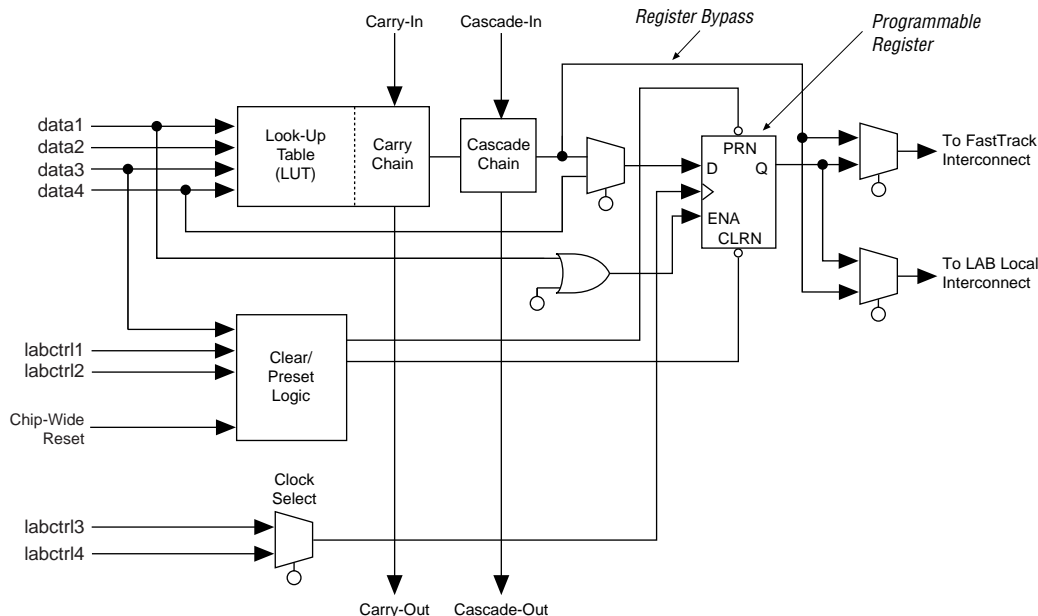*Figure 3. ACEX 1K EAB in Dual-Port RAM Mode*

Figure 4. ACEX 1K Device in Single-Port RAM Mode

Note:
(1)   EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

Figure 8. ACEX 1K Logic Element

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the LUT's output drives the LE's output.

The LE has two outputs that drive the interconnect: one drives the local interconnect, and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The ACEX 1K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders, and the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the ACEX 1K architecture to efficiently implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the compiler during design processing, or manually by the designer during design entry. Parameterized functions, such as LPM and DesignWare functions, automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EP1K50 device, the carry chain stops at the eighteenth LAB, and a new carry chain begins at the nineteenth LAB.

Figure 9 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 11, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

Asynchronous Clear

The flipflop can be cleared by either `LABCTRL1` or `LABCTRL2`. In this mode, the preset signal is tied to `VCC` to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If `DATA3` is tied to `VCC`, asserting `LABCTRL1` asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the register's input and output. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two `LABCTRL` signals, the `DATA3` input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, `LABCTRL1` controls the preset, and `LABCTRL2` controls the clear. `DATA3` is tied to `VCC`, so that asserting `LABCTRL1` asynchronously loads a one into the register, effectively presetting the register. Asserting `LABCTRL2` clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear. `LABCTRL2` implements the clear by controlling the register clear; `LABCTRL2` does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting `LABCTRL2` presets the register, while asserting `LABCTRL1` loads the register. The Altera software inverts the signal that drives `DATA3` to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear.

Figure 13. ACEX 1K LAB Connections to Row & Column Interconnect

Column
Channels

Row Channels

To Other
Columns

At each intersection,
six row channels can
drive column channels.

Each LE can drive two
row channels.

From Adjacent LAB
To Adjacent LAB

LE 1

LE 2

LE 8

Each LE can switch
interconnect access
with an LE in the
adjacent LAB.

To LAB Local
Interconnect

To Other Rows
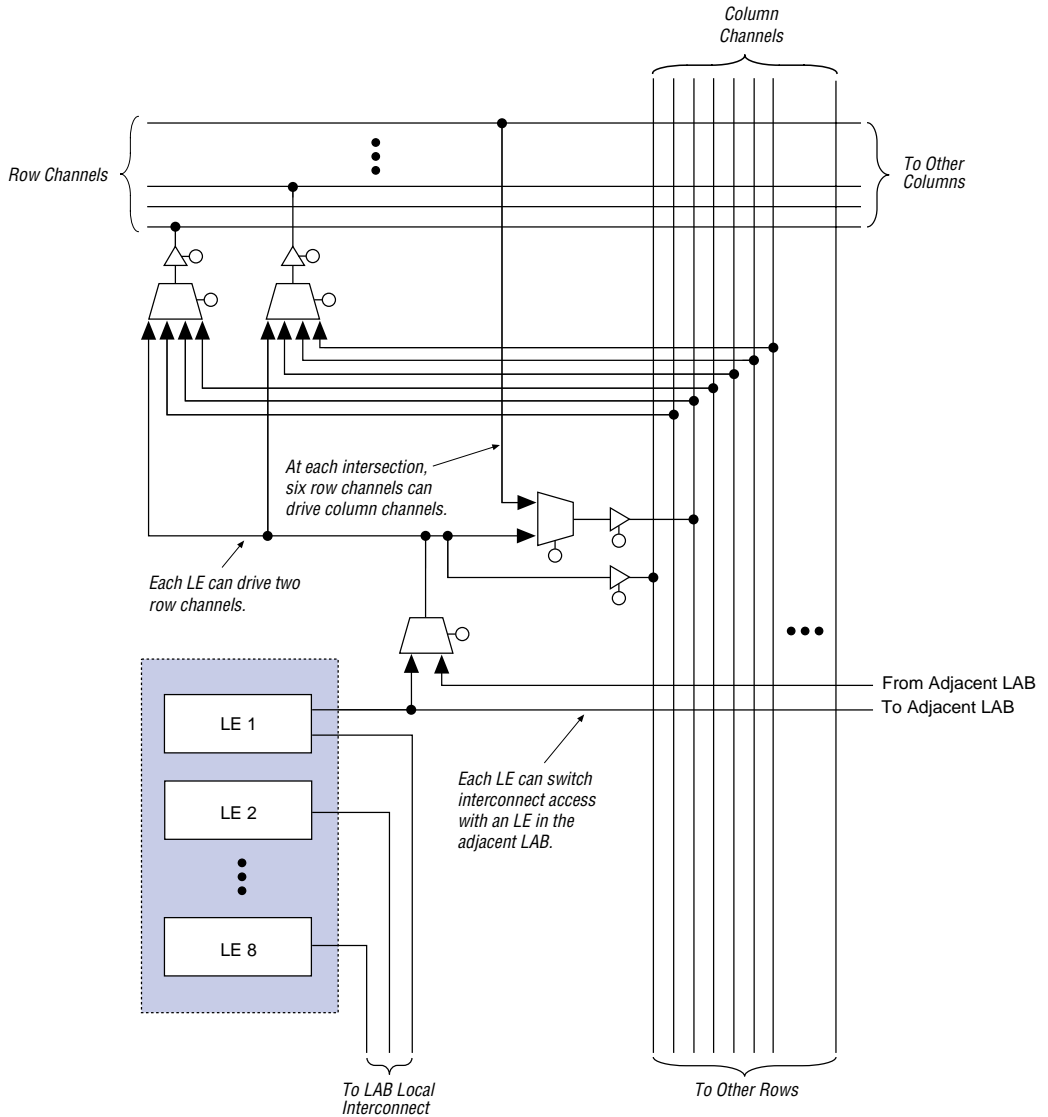
Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. ACEX 1K Row-to-IOE Connections   Note (1)
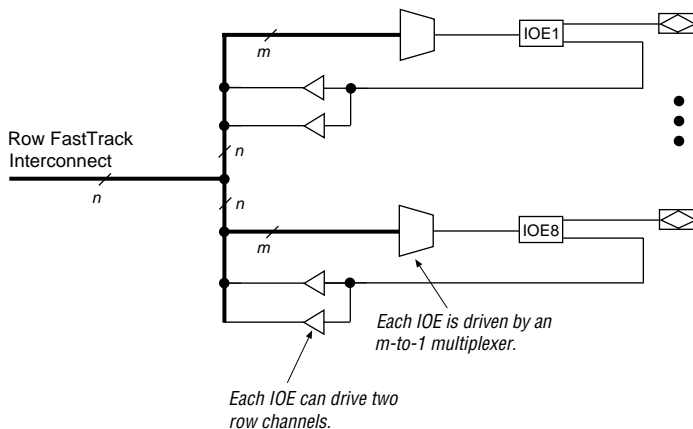
Note:
(1) The values for *m* and *n* are shown in Table 8.

Table 8 lists the ACEX 1K row-to-IOE interconnect resources.

Table 8. ACEX 1K Row-to-IOE Interconnect Resources

Device	Channels per Row (*n*)	Row Channels per Pin (*m*)
EP1K10	144	18
EP1K30	216	27
EP1K50	216	27
EP1K100	312	39

For more information, search for "SameFrame" in MAX+PLUS II Help.

Table 10. ACEX 1K SameFrame Pin-Out Support

Device	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	✓	*(1)*
EP1K30	✓	*(1)*
EP1K50	✓	✓
EP1K100	✓	✓

Note:
(1)   This option is supported with a 256-pin FineLine BGA package and SameFrame migration.

ClockLock & ClockBoost Features

To support high-speed designs, -1 and -2 speed grade ACEX 1K devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in ACEX 1K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry lock onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

Table 26. Interconnect Timing Microparameters   *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	(7)
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial and extended use in ACEX 1K devices

(3) Operating conditions: V_{CCIO} = 2.5 V ± 5% for commercial or industrial and extended use in ACEX 1K devices.

(4) Operating conditions: V_{CCIO} = 2.5 V or 3.3 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABBYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

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Table 37. EP1K30 Device LE Timing Microparameters (Part 2 of 2) Note (1)

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{COMB}		0.4		0.4		0.6	ns
t_{SU}	0.4		0.6		0.6		ns
t_H	0.7		1.0		1.3		ns
t_{PRE}		0.8		0.9		1.2	ns
t_{CLR}		0.8		0.9		1.2	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 38. EP1K30 Device IOE Timing Microparameters   Note (1)

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.4		2.8		3.8	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		1.0		1.1		1.6	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.2		1.4		1.9		ns
t_{IOH}	0.3		0.4		0.5		ns
t_{IOCLR}		1.0		1.1		1.6	ns
t_{OD1}		1.9		2.3		3.0	ns
t_{OD2}		1.4		1.8		2.5	ns
t_{OD3}		4.4		5.2		7.0	ns
t_{XZ}		2.7		3.1		4.3	ns
t_{ZX1}		2.7		3.1		4.3	ns
t_{ZX2}		2.2		2.6		3.8	ns
t_{ZX3}		5.2		6.0		8.3	ns
t_{INREG}		3.4		4.1		5.5	ns
t_{IOFD}		0.8		1.3		2.4	ns
t_{INCOMB}		0.8		1.3		2.4	ns

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Table 39. EP1K30 Device EAB Internal Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
t_{EABWE1}		1.1		1.3		1.4	ns
t_{EABWE2}		0.4		0.4		0.5	ns
t_{EABRE1}		0.8		0.9		1.0	ns
t_{EABRE2}		0.4		0.4		0.5	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.4	ns
$t_{EABBYPASS}$		0.5		0.6		0.7	ns
t_{EABSU}	0.9		1.0		1.2		ns
t_{EABH}	0.4		0.4		0.5		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.2		3.8		4.4	ns
t_{WP}	2.5		2.9		3.3		ns
t_{RP}	0.9		1.1		1.2		ns
t_{WDSU}	0.9		1.0		1.1		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.7		2.0		2.3		ns
t_{WAH}	1.8		2.1		2.4		ns
t_{RASU}	3.1		3.7		4.2		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.5		2.9		3.3	ns
t_{DD}		2.5		2.9		3.3	ns
t_{EABOUT}		0.5		0.6		0.7	ns
t_{EABCH}	1.5		2.0		2.3		ns
t_{EABCL}	2.5		2.9		3.3		ns

Table 40. EP1K30 Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
t_{EABWP}	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
t_{EABDD}		5.7		6.7		7.7	ns
$t_{EABDATACO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
t_{EABWAH}	0.5		0.5		0.4		ns
t_{EABWO}		5.1		6.0		6.8	ns

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Table 43. EP1K30 External Bidirectional Timing Parameters   *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (3)	2.8		3.9		5.2		ns
$t_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ (4)	3.8		4.9		–		ns
$t_{INHBIDIR}$ (4)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{XZBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{ZXBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{OUTCOBIDIR}$ (4)	0.5	3.9	0.5	4.9	–	–	ns
$t_{XZBIDIR}$ (4)		5.1		6.5		–	ns
$t_{ZXBIDIR}$ (4)		5.1		6.5		–	ns

Notes to tables:

(1)   All timing parameters are described in Tables 22 through 29 in this data sheet.
(2)   These parameters are specified by characterization.
(3)   This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4)   This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 44 through 50 show EP1K50 device external timing parameters.

Table 44. EP1K50 Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns
t_{CGENR}		0.1		0.1		0.1	ns
t_{CASC}		0.5		0.8		1.0	ns
t_C		0.5		0.6		0.8	ns

Table 46. EP1K50 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
t_{EABWE1}		1.0		1.4		1.9	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0.0		0.0		0.0	
t_{EABRE2}		0.4		0.6		0.8	
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		1.1		1.5	ns
$t_{EABBYPASS}$		0.0		0.0		0.0	ns
t_{EABSU}	0.7		1.0		1.3		ns
t_{EABH}	0.4		0.6		0.8		ns
t_{EABCLR}	0.8		1.1		1.5		
t_{AA}		2.0		2.8		3.8	ns
t_{WP}	2.0		2.8		3.8		ns
t_{RP}	1.0		1.4		1.9		
t_{WDSU}	0.5		0.7		0.9		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.0		1.4		1.9		ns
t_{WAH}	1.5		2.1		2.9		ns
t_{RASU}	1.5		2.1		2.8		
t_{RAH}	0.1		0.1		0.2		
t_{WO}		2.1		2.9		4.0	ns
t_{DD}		2.1		2.9		4.0	ns
t_{EABOUT}		0.0		0.0		0.0	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	1.5		2.0		2.5		ns

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

Table 51. EP1K100 Device LE Timing Microparameters Note (1)							
Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		1.0		1.5	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		0.6		0.8		1.1	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.2		0.3		0.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.9		1.2	ns
t_C		0.8		1.0		1.4	ns
t_{CO}		0.6		0.8		1.1	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.4		0.6		0.7		ns
t_H	0.5		0.7		0.9		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.8		1.0		1.4	ns
t_{CH}	1.5		2.0		2.5		ns
t_{CL}	1.5		2.0		2.5		ns

Table 55. EP1K100 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.6		4.4	ns
t_{DIN2LE}		0.3		0.4		0.5	ns
$t_{DIN2DATA}$		1.6		1.8		2.0	ns
$t_{DCLK2IOE}$		0.8		1.1		1.4	ns
$t_{DCLK2LE}$		0.3		0.4		0.5	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		2.5		3.4	ns
$t_{SAMECOLUMN}$		0.4		1.0		1.6	ns
$t_{DIFFROW}$		1.9		3.5		5.0	ns
$t_{TWOROWS}$		3.4		6.0		8.4	ns
$t_{LEPERIPH}$		4.3		5.4		6.5	ns
$t_{LABCARRY}$		0.5		0.7		0.9	ns
$t_{LABCASC}$		0.8		1.0		1.4	ns

Table 56. EP1K100 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	2.0		2.5		3.3		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t_{INSU} *(4)*	2.0		2.2		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns

Altera Corporation

Revision History

The information contained in the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4 supersedes information published in previous versions.

The following changes were made to the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4: added extended temperature support.