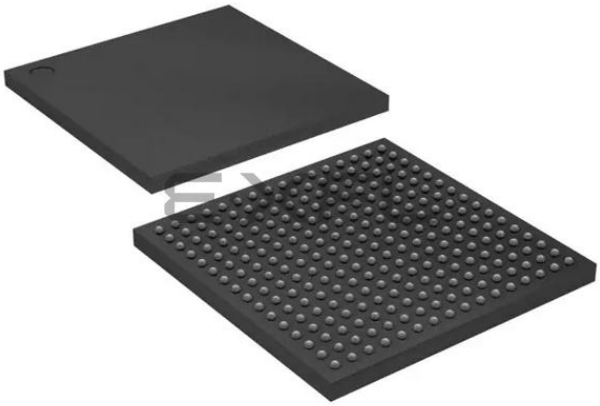


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	186
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k100fi256-2n

- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Flexible package options are available in 100 to 484 pins, including the innovative FineLine BGA™ packages (see Tables 2 and 3)
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 2. ACEX 1K Package Options & I/O Pin Count *Notes (1), (2)*

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	66	92	120	136	136 *(3)*
EP1K30		102	147	171	171 *(3)*
EP1K50		102	147	186	249
EP1K100			147	186	333

Notes:

(1) ACEX 1K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and FineLine BGA packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 256-pin FineLine BGA package. By using SameFrame™ pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin and 484-pin FineLine BGA packages.

Table 3. ACEX 1K Package Sizes

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.0
Area (mm^2)	256	484	936	289	529
Length × width (mm × mm)	16 × 16	22 × 22	30.6 × 30.6	17 × 17	23 × 23

Embedded Array Block

The EAB is a flexible block of RAM, with registers on the input and output ports, that is used to implement common gate array megafunctions. Because it is large and flexible, the EAB is suitable for functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in a single logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement any function with 8 inputs and 16 outputs. Parameterized functions, such as LPM functions, can take advantage of the EAB automatically.

The ACEX 1K enhanced EAB supports dual-port RAM. The dual-port structure is ideal for FIFO buffers with one or two clocks. The ACEX 1K EAB can also support up to 16-bit-wide RAM blocks. The ACEX 1K EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, allowing the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allow independent control of these sections.

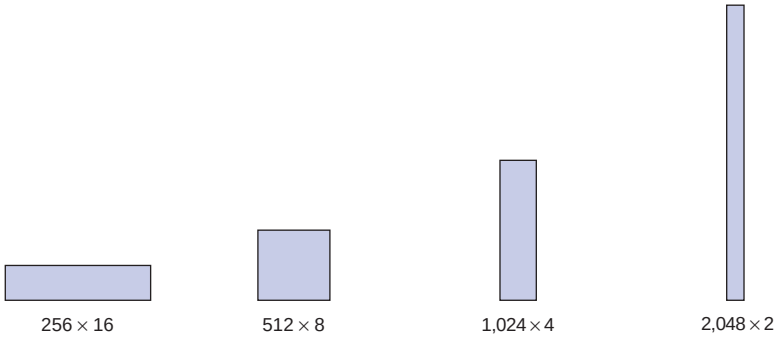
The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous reads or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16; 512 × 8; 1,024 × 4; or 2,048 × 2. Figure 5 shows the ACEX 1K EAB memory configurations.

Figure 5. ACEX 1K EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 block. Figure 6 shows examples of multiple EAB combination.

Figure 6. Examples of Combining ACEX 1K EABs

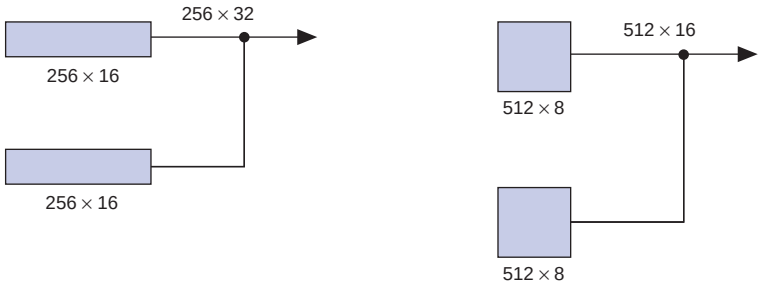
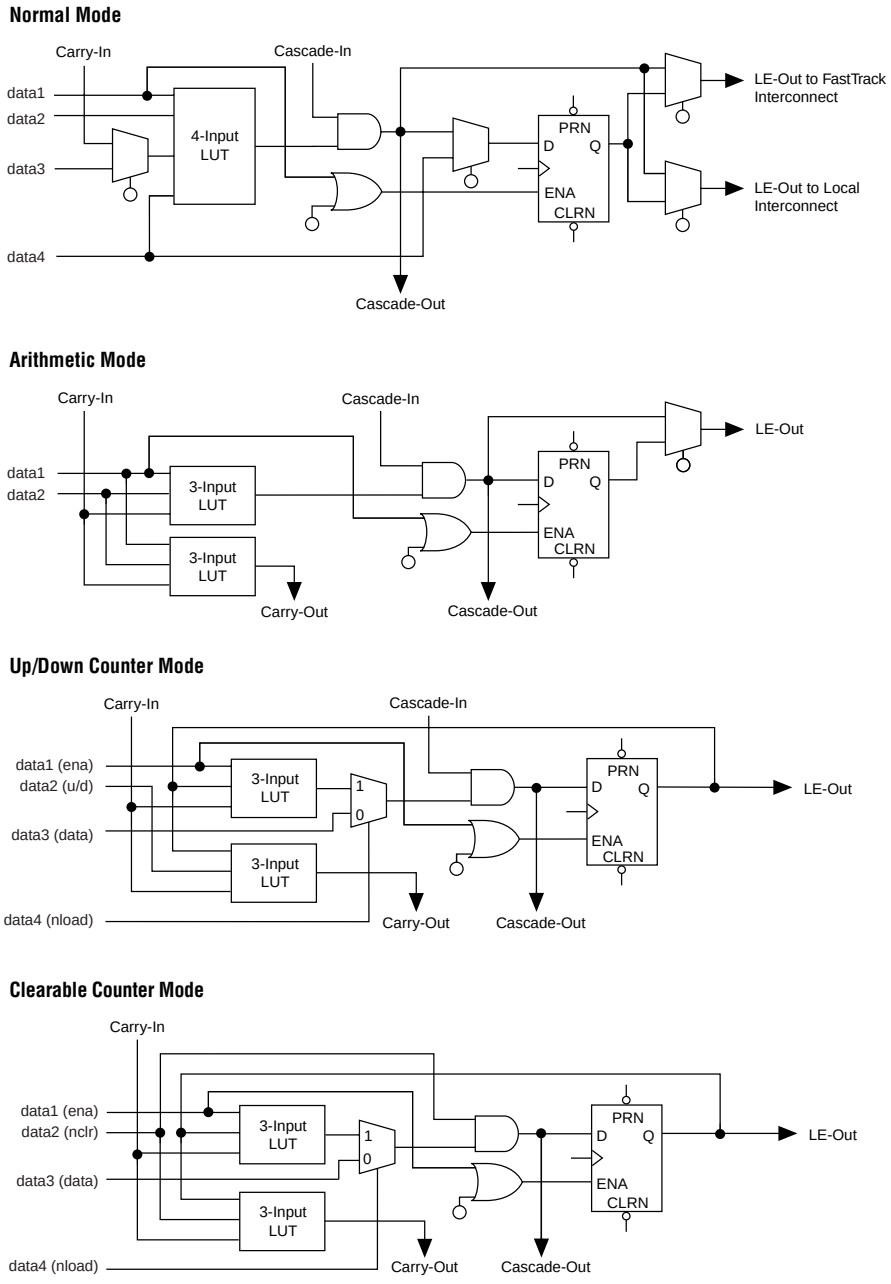


Figure 11. ACEX 1K LE Operating Modes



In addition to the six clear and preset modes, ACEX 1K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. ACEX 1K LE Clear & Preset Modes

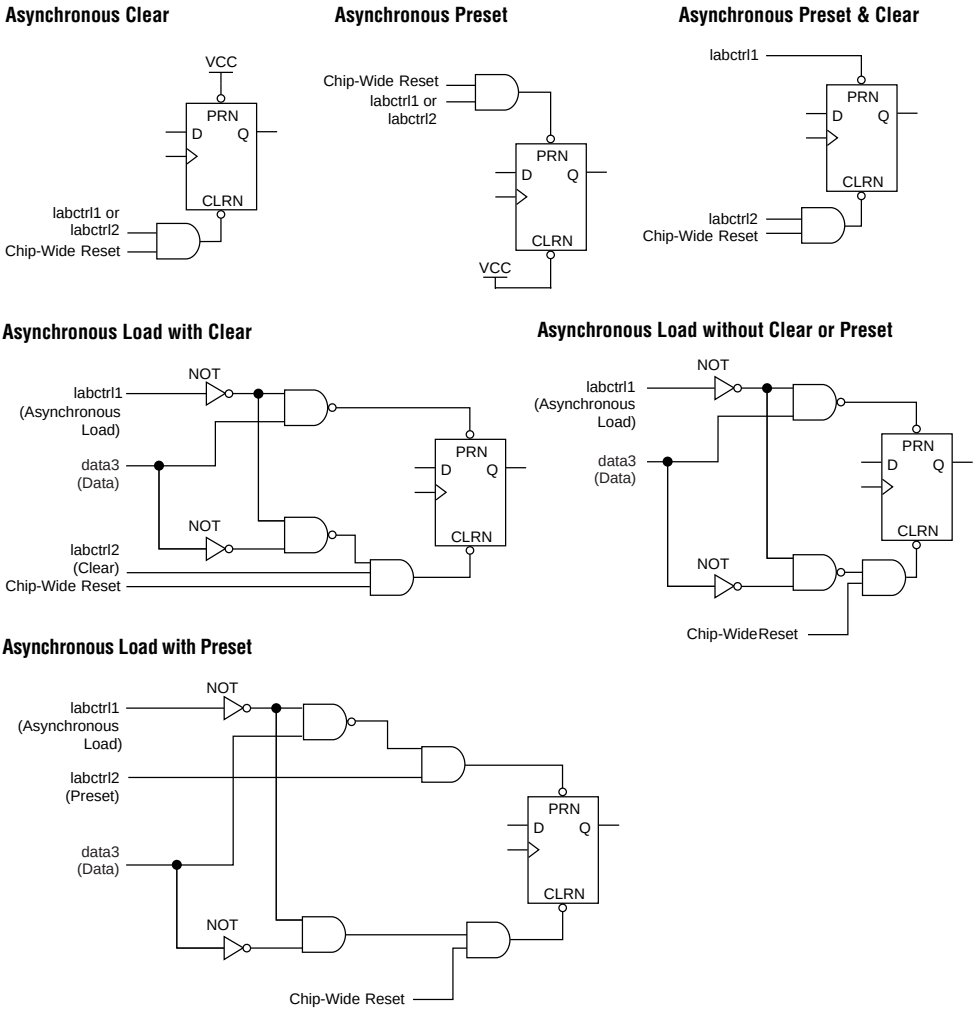
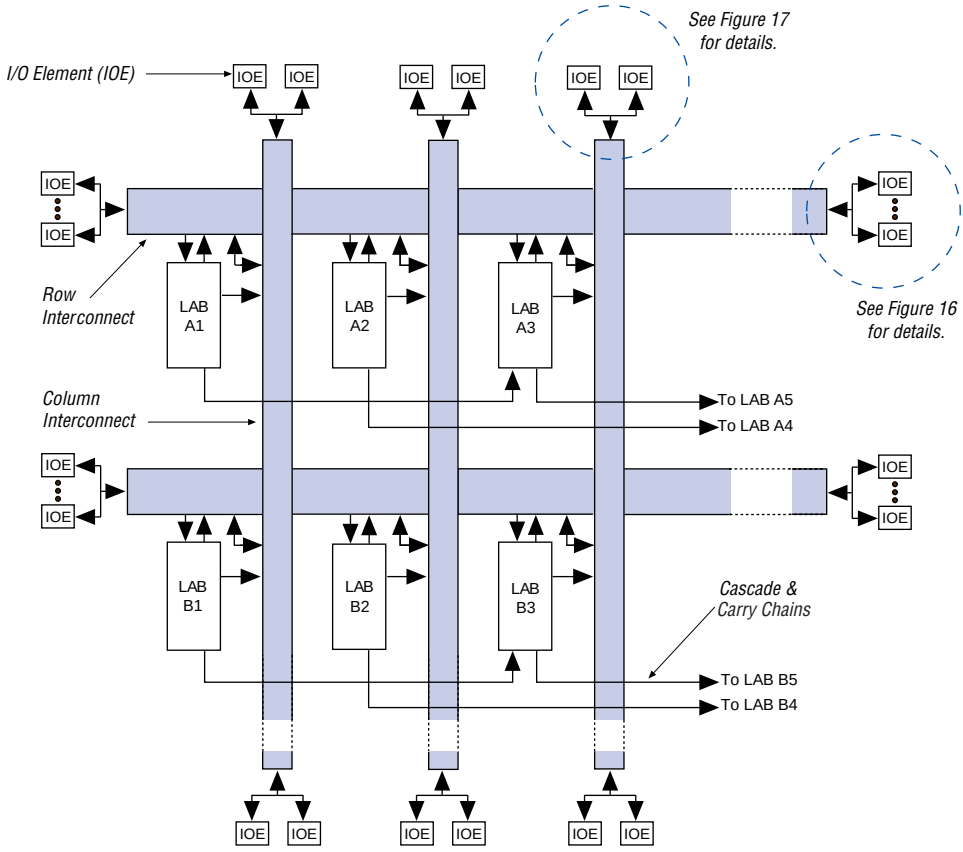


Figure 14. ACEX 1K Interconnect Resources



I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. For bidirectional registered I/O implementation, the output register should be in the IOE and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. Figure 15 shows the bidirectional I/O registers.

For more information, search for “SameFrame” in MAX+PLUS II Help.

Table 10. ACEX 1K SameFrame Pin-Out Support

Device	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	✓	*(1)*
EP1K30	✓	*(1)*
EP1K50	✓	✓
EP1K100	✓	✓

Note:
(1) This option is supported with a 256-pin FineLine BGA package and SameFrame migration.

ClockLock & ClockBoost Features

To support high-speed designs, -1 and -2 speed grade ACEX 1K devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in ACEX 1K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry lock onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

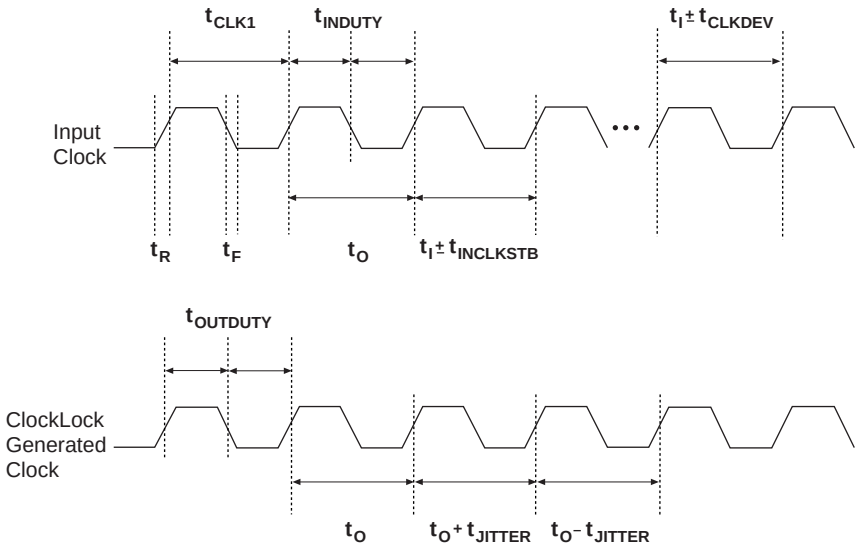
The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the GCLK1 pin. In the Altera software, the GCLK1 pin can feed both the ClockLock and ClockBoost circuitry in the ACEX 1K device. However, when both circuits are used, the other clock pin cannot be used.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

Figure 19. Specifications for the Incoming & Generated Clocks *Note (1)*



Note:

(1) The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 11. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the Altera software *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ <100			250 *(4)*	ps
		$t_{INCLKSTB}$ < 50			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Table 12. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		80	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		40	MHz
f_{CLKDEV}	Input deviation from user specification in the software *(1)*				25,000	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250 *(4)*	ps
		$t_{INCLKSTB}$ < 50			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes to tables:

(1) To implement the ClockLock and ClockBoost circuitry with the Altera software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

I/O Configuration

This section discusses the PCI pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for ACEX 1K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT}. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0 V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 13 summarizes ACEX 1K MultiVolt I/O support.

Table 13. ACEX 1K MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled on an input which is driven with a voltage higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an ACEX 1K device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on ACEX 1K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a higher V_{IH} than LVTTL. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting the CMOS V_{OH} requirement. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot-Socketing

Because ACEX 1K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

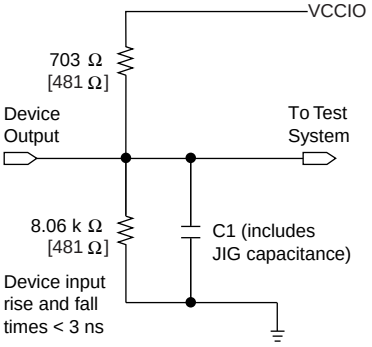
Signals can be driven into ACEX 1K devices before and during power up without damaging the device. Additionally, ACEX 1K devices do not drive out during power up. Once operating conditions are reached, ACEX 1K devices operate as specified by the user.

Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. ACEX 1K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



Operating Conditions

Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

Table 18. ACEX 1K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	° C

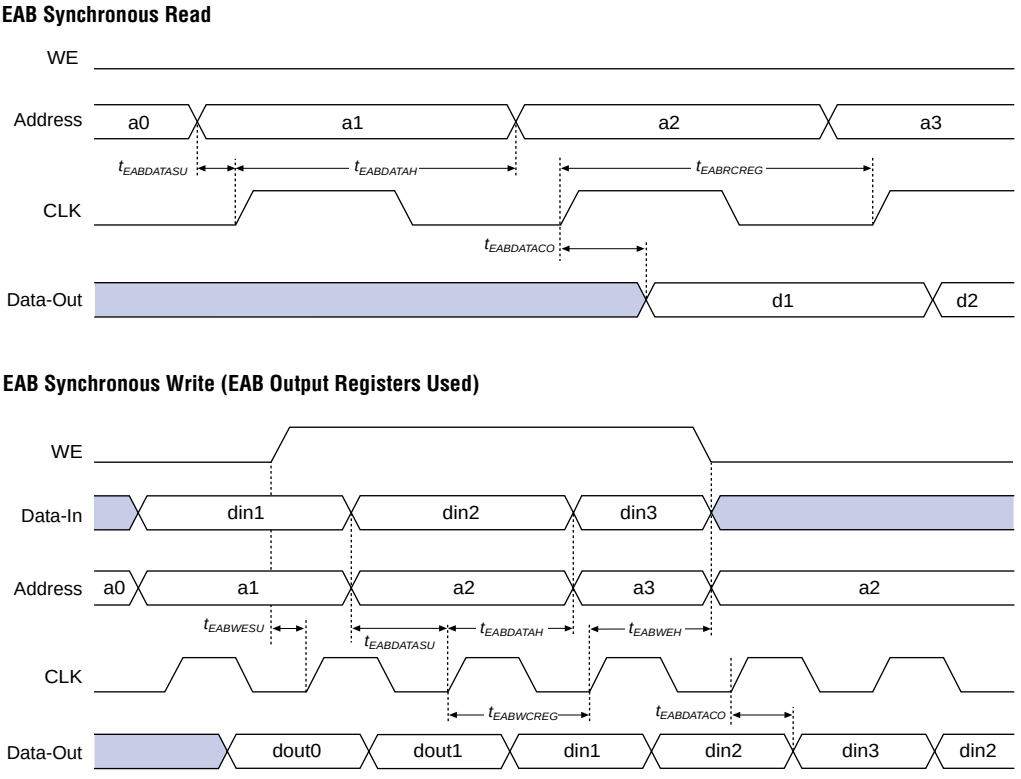
Table 21. ACEX 1K Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial- and extended-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the ACEX 1K Recommended Operating Conditions shown in Table 19 on page 46.
(8) The ACEX 1K input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 22.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed grade commercial temperature devices and -2 speed grade industrial and extended temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
(14) Capacitance is sample-tested only.

Figure 30. EAB Synchronous Timing Waveforms



Tables 22 through 26 describe the ACEX 1K device internal timing parameters.

Table 22. LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	

Tables 30 through 36 show EP1K10 device internal and external timing parameters.

Table 30. EP1K10 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		0.9		1.0		1.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.7		0.9		1.1	ns
t_{C}		1.1		1.3		1.7	ns
t_{CO}		0.5		0.7		0.9	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.7		0.8		1.0		ns
t_{H}	0.9		1.0		1.1		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 31. EP1K10 Device IOE Timing Microparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		2.6		3.1		4.0	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		0.9		1.0		1.4	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.3		1.5		2.0		ns
t_{IOH}	0.9		1.0		1.4		ns
t_{IOCLR}		1.1		1.3		1.7	ns
t_{OD1}		3.1		3.7		4.1	ns
t_{OD2}		2.6		3.3		3.9	ns
t_{OD3}		5.8		6.9		8.3	ns
t_{XZ}		3.8		4.5		5.9	ns
t_{ZX1}		3.8		4.5		5.9	ns
t_{ZX2}		3.3		4.1		5.7	ns
t_{ZX3}		6.5		7.7		10.1	ns
t_{INREG}		3.7		4.3		5.7	ns
t_{IOFD}		0.9		1.0		1.4	ns
t_{INCOMB}		1.9		2.3		3.0	ns

Table 37. EP1K30 Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{COMB}		0.4		0.4		0.6	ns
t_{SU}	0.4		0.6		0.6		ns
t_{H}	0.7		1.0		1.3		ns
t_{PRE}		0.8		0.9		1.2	ns
t_{CLR}		0.8		0.9		1.2	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 38. EP1K30 Device IOE Timing Microparameters *Note (1)*

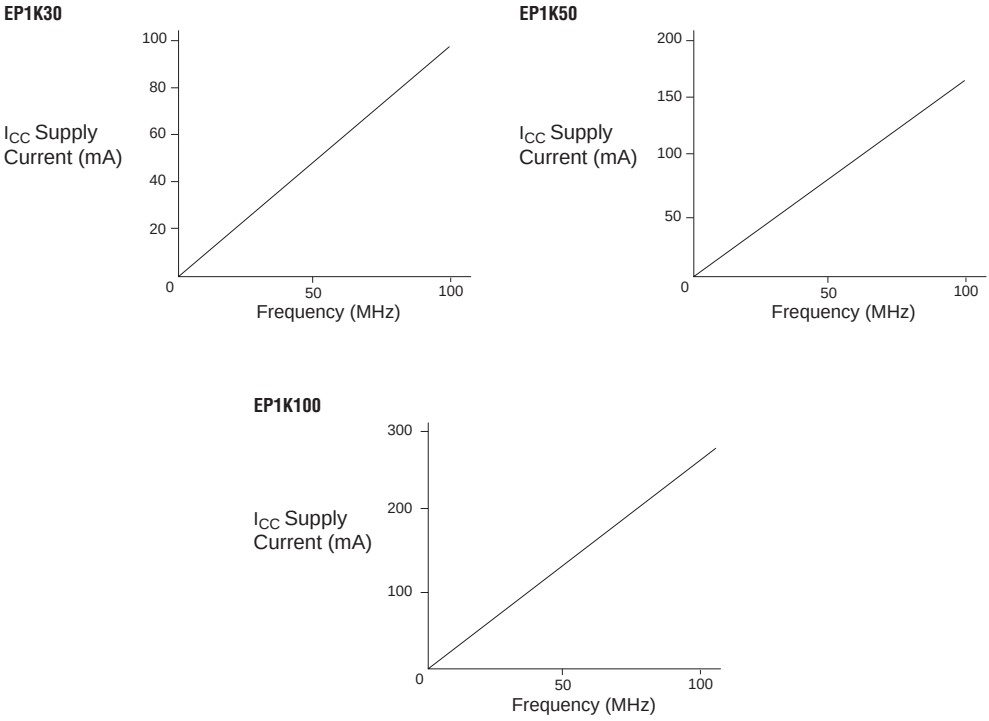
Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.4		2.8		3.8	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		1.0		1.1		1.6	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.2		1.4		1.9		ns
t_{IOH}	0.3		0.4		0.5		ns
t_{IOCLR}		1.0		1.1		1.6	ns
t_{OD1}		1.9		2.3		3.0	ns
t_{OD2}		1.4		1.8		2.5	ns
t_{OD3}		4.4		5.2		7.0	ns
t_{XZ}		2.7		3.1		4.3	ns
t_{ZX1}		2.7		3.1		4.3	ns
t_{ZX2}		2.2		2.6		3.8	ns
t_{ZX3}		5.2		6.0		8.3	ns
t_{INREG}		3.4		4.1		5.5	ns
t_{IOFD}		0.8		1.3		2.4	ns
t_{INCOMB}		0.8		1.3		2.4	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
t_{EABWP}	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
t_{EABDD}		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
t_{EABWEH}	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
t_{EABWAH}	0.9		1.2		1.8		ns
t_{EABWO}		3.1		4.3		5.9	ns

Table 54. EP1K100 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Figure 31. ACEX 1K $I_{CCACTIVE}$ vs. Operating Frequency



Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50 µs.

When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.