



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	147
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1k100qc208-2ngz">https://www.e-xfl.com/product-detail/intel/ep1k100qc208-2ngz</a>

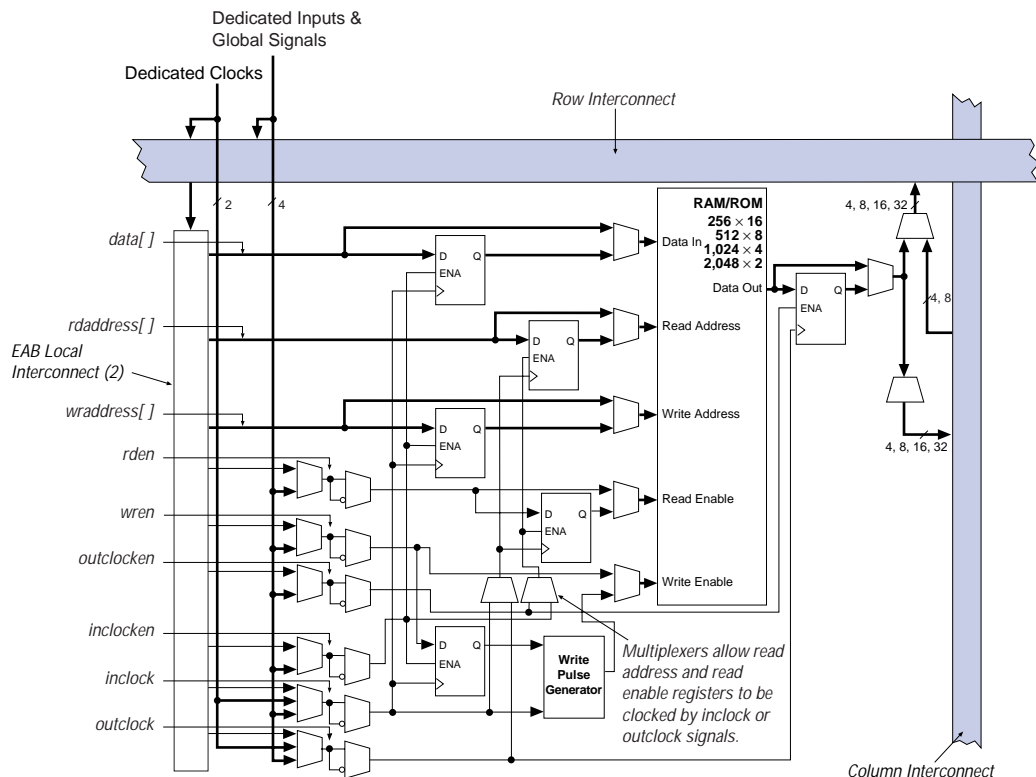
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input LUT, a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable logic gates.

Signal interconnections within ACEX 1K devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.1 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 2.5 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

**Figure 1** shows a block diagram of the ACEX 1K device architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 2. ACEX 1K Device in Dual-Port RAM Mode *Note (1)*



**Notes:**

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

Figure 3. ACEX 1K EAB in Dual-Port RAM Mode

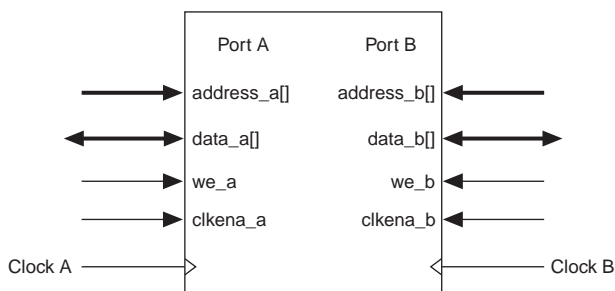
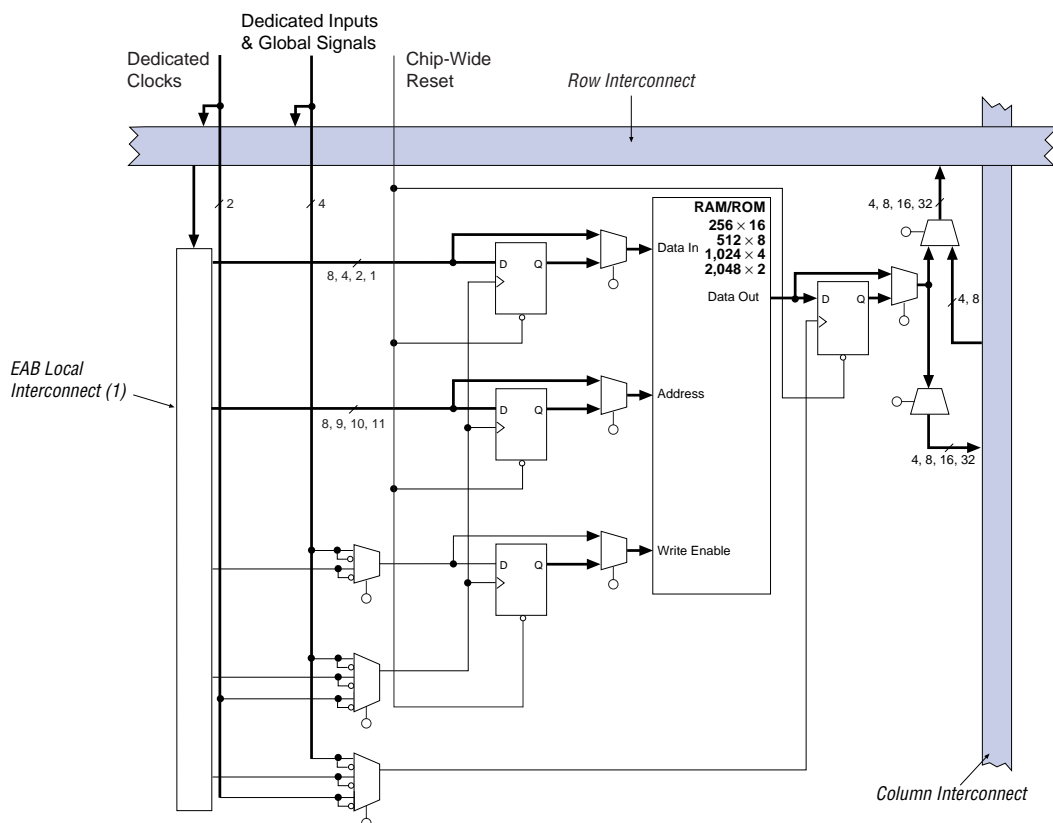


Figure 4. ACEX 1K Device in Single-Port RAM Mode



**Note:**

- (1) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the ACEX 1K architecture, has a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure. [Figure 8](#) shows the ACEX 1K LE.

### *Carry Chain*

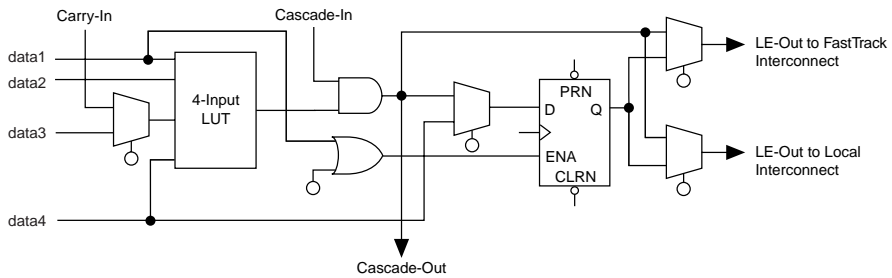
The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the ACEX 1K architecture to efficiently implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the compiler during design processing, or manually by the designer during design entry. Parameterized functions, such as LPM and DesignWare functions, automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EP1K50 device, the carry chain stops at the eighteenth LAB, and a new carry chain begins at the nineteenth LAB.

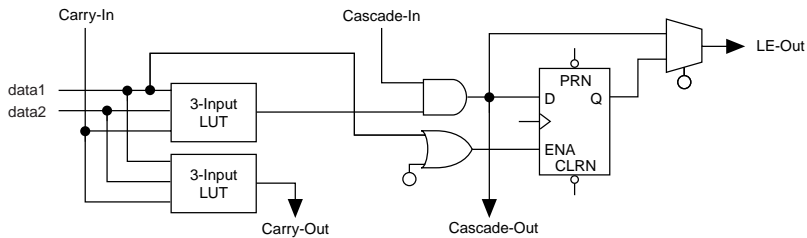
**Figure 9** shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 11. ACEX 1K LE Operating Modes

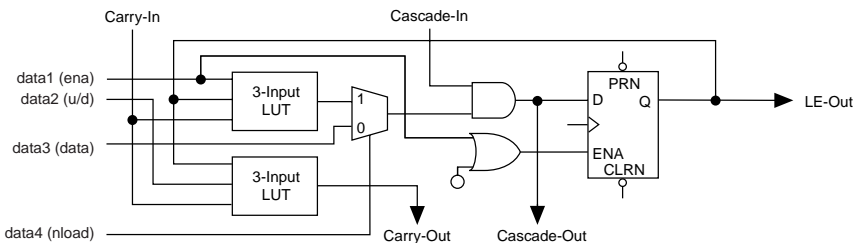
**Normal Mode**



**Arithmetic Mode**



**Up/Down Counter Mode**



**Clearable Counter Mode**

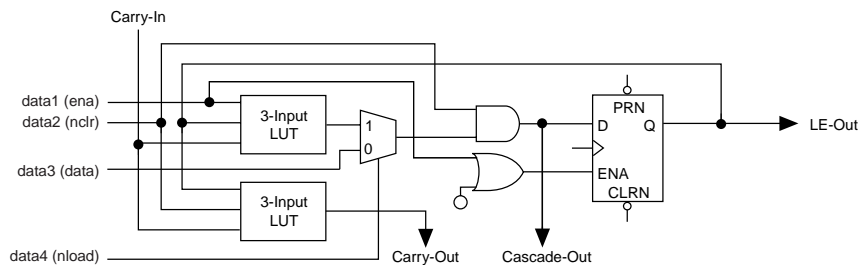
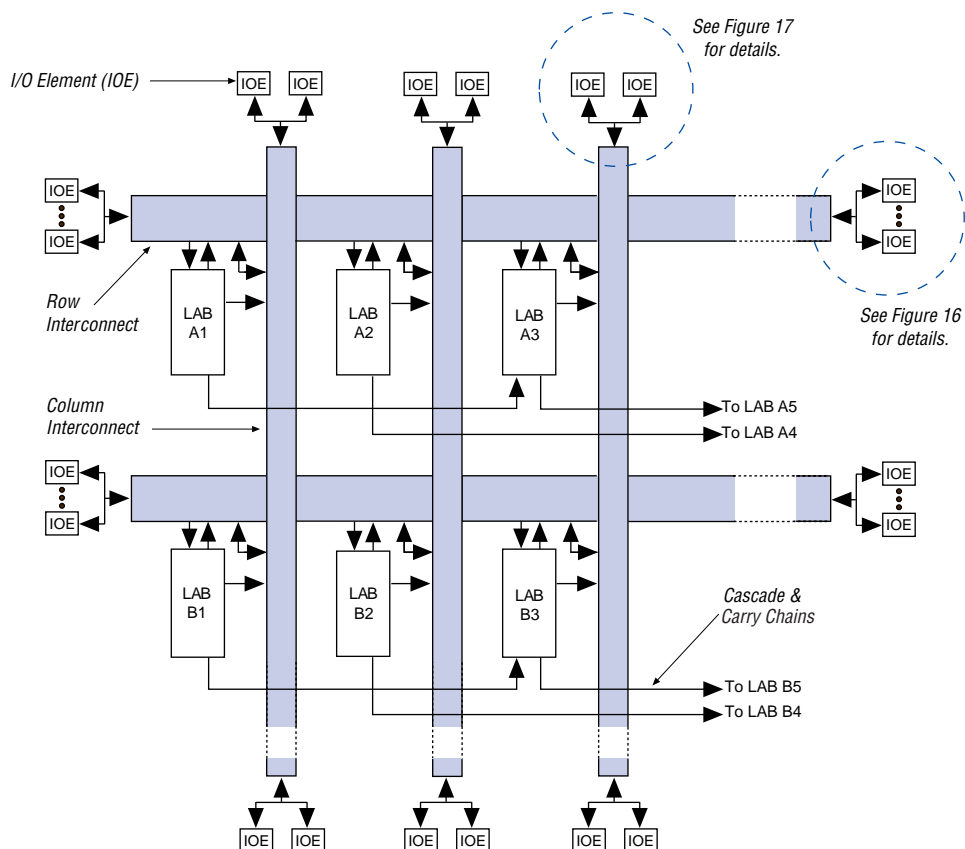


Figure 14. ACEX 1K Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. For bidirectional registered I/O implementation, the output register should be in the IOE and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. [Figure 15](#) shows the bidirectional I/O registers.





For more information, search for “SameFrame” in MAX+PLUS II Help.

Table 10. ACEX 1K SameFrame Pin-Out Support		
Device	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	✓	(1)
EP1K30	✓	(1)
EP1K50	✓	✓
EP1K100	✓	✓

**Note:**  
(1) This option is supported with a 256-pin FineLine BGA package and SameFrame migration.

ClockLock &  
ClockBoost  
Features

To support high-speed designs, -1 and -2 speed grade ACEX 1K devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in ACEX 1K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry lock onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

Table 12. ClockLock &amp; ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_R$	Input rise time				5	ns
$t_F$	Input fall time				5	ns
$t_{INDUTY}$	Input duty cycle		40		60	%
$f_{CLK1}$	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		80	MHz
$f_{CLK2}$	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		40	MHz
$f_{CLKDEV}$	Input deviation from user specification in the software (1)				25,000	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
$t_{LOCK}$	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
$t_{JITTER}$	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250 (4)	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

**Notes to tables:**

- (1) To implement the ClockLock and ClockBoost circuitry with the Altera software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The  $f_{CLKDEV}$  parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the  $t_{LOCK}$  value is less than the time required for configuration.
- (4) The  $t_{JITTER}$  specification is measured under long-term observation. The maximum value for  $t_{JITTER}$  is 200 ps if  $t_{INCLKSTB}$  is lower than 50 ps.

## I/O Configuration

This section discusses the PCI pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for ACEX 1K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting  $V_{CCIO}$  to a different voltage than  $V_{CCINT}$ . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

Table 19. ACEX 1K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage for internal logic and input buffers	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V <sub>CCIO</sub>	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V <sub>I</sub>	Input voltage	(2), (5)	−0.5	5.75	V
V <sub>O</sub>	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>A</sub>	Ambient temperature	Commercial range	0	70	°C
		Industrial range	−40	85	°C
T <sub>J</sub>	Junction temperature	Commercial range	0	85	°C
		Industrial range	−40	100	°C
		Extended range	−40	125	°C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

Table 20. ACEX 1K Device DC Operating Conditions (Part 1 of 2) Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High-level input voltage		1.7, 0.5 × V <sub>CCIO</sub> (8)		5.75	V
V <sub>IL</sub>	Low-level input voltage		−0.5		0.8, 0.3 × V <sub>CCIO</sub> (8)	V
V <sub>OH</sub>	3.3-V high-level TTL output voltage	I <sub>OH</sub> = −8 mA DC, V <sub>CCIO</sub> = 3.00 V (9)	2.4			V
	3.3-V high-level CMOS output voltage	I <sub>OH</sub> = −0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (9)	V <sub>CCIO</sub> − 0.2			V
	3.3-V high-level PCI output voltage	I <sub>OH</sub> = −0.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (9)	0.9 × V <sub>CCIO</sub>			V
	2.5-V high-level output voltage	I <sub>OH</sub> = −0.1 mA DC, V <sub>CCIO</sub> = 2.375 V (9)	2.1			V
		I <sub>OH</sub> = −1 mA DC, V <sub>CCIO</sub> = 2.375 V (9)	2.0			V
		I <sub>OH</sub> = −2 mA DC, V <sub>CCIO</sub> = 2.375 V (9)	1.7			V

Figure 22 shows the required relationship between  $V_{CCIO}$  and  $V_{CCINT}$  to satisfy 3.3-V PCI compliance.

Figure 22. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

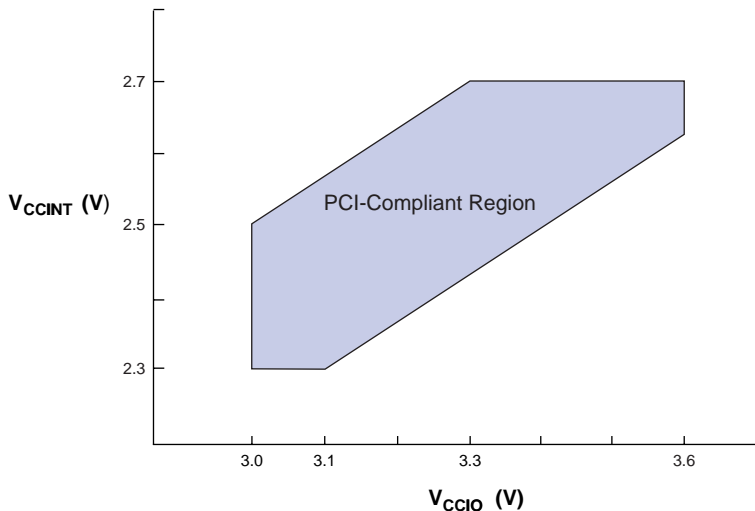
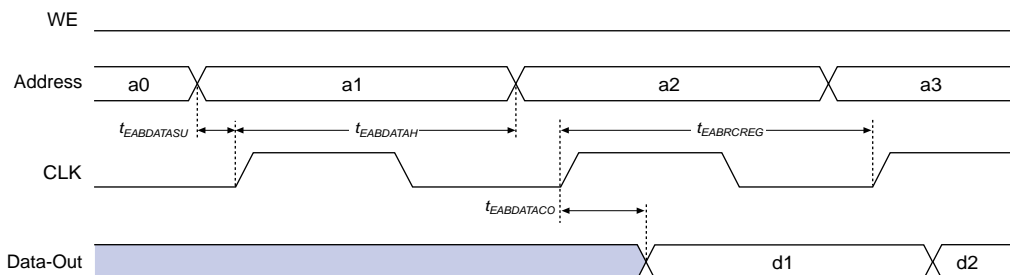
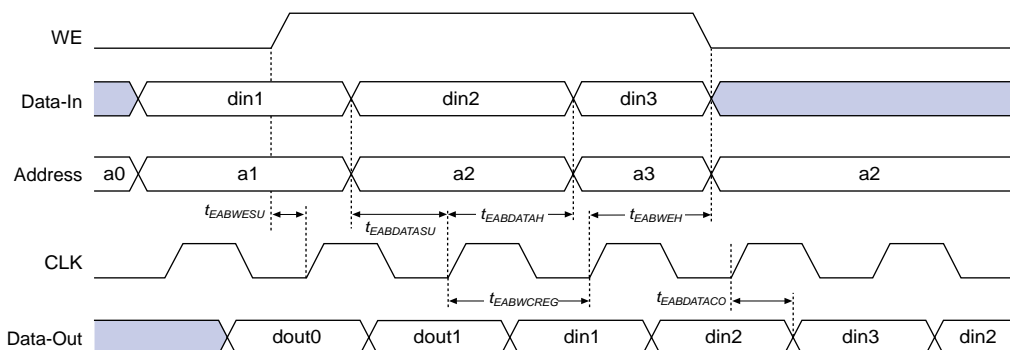


Figure 23 shows the typical output drive characteristics of ACEX 1K devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compliant to the **3.3-V PCI Local Bus Specification, Revision 2.2** (when  $V_{CCIO}$  pins are connected to 3.3 V). ACEX 1K devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCINT}$  pins are powered with a minimum supply of 2.375 V, and  $V_{CCIO}$  pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Figure 30. EAB Synchronous Timing Waveforms

**EAB Synchronous Read****EAB Synchronous Write (EAB Output Registers Used)**

Tables 22 through 26 describe the ACEX 1K device internal timing parameters.

Table 22. LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions
$t_{LUT}$	LUT delay for data-in	
$t_{CLUT}$	LUT delay for carry-in	
$t_{RLUT}$	LUT delay for LE register feedback	
$t_{PACKED}$	Data-in to packed register delay	
$t_{EN}$	LE register enable delay	
$t_{CICO}$	Carry-in to carry-out delay	
$t_{CGEN}$	Data-in to carry-out delay	
$t_{CGENR}$	LE register feedback to carry-out delay	

Table 22. LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions
$t_{CASC}$	Cascade-in to cascade-out delay	
$t_C$	LE register control signal delay	
$t_{CO}$	LE register clock-to-output delay	
$t_{COMB}$	Combinatorial delay	
$t_{SU}$	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
$t_H$	LE register hold time for data and enable signals after clock	
$t_{PRE}$	LE register preset delay	
$t_{CLR}$	LE register clear delay	
$t_{CH}$	Minimum clock high time from clock pin	
$t_{CL}$	Minimum clock low time from clock pin	

Table 23. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{IOD}$	IOE data delay	
$t_{IOC}$	IOE register control signal delay	
$t_{IOCO}$	IOE register clock-to-output delay	
$t_{IOCOMB}$	IOE combinatorial delay	
$t_{IOSU}$	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
$t_{IOH}$	IOE register hold time for data and enable signals after clock	
$t_{IOCLR}$	IOE register clear time	
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF (3)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
$t_{XZ}$	IOE output buffer disable delay	
$t_{ZX1}$	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF (2)
$t_{ZX2}$	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF (3)
$t_{ZX3}$	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
$t_{INREG}$	IOE input pad and buffer to IOE register delay	
$t_{OFD}$	IOE register feedback delay	
$t_{INCOMB}$	IOE input pad and buffer to FastTrack Interconnect delay	

Table 24. EAB Timing Microparameters <i>Note (1)</i>		
Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
$t_{EABWE1}$	Write enable delay to EAB for combinatorial input	
$t_{EABWE2}$	Write enable delay to EAB for registered input	
$t_{EABRE1}$	Read enable delay to EAB for combinatorial input	
$t_{EABRE2}$	Read enable delay to EAB for registered input	
$t_{EABCLK}$	EAB register clock delay	
$t_{EABCO}$	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
$t_{EABSU}$	EAB register setup time before clock	
$t_{EABH}$	EAB register hold time after clock	
$t_{EABCLR}$	EAB register asynchronous clear time to output delay	
$t_{AA}$	Address access delay (including the read enable to output delay)	
$t_{WP}$	Write pulse width	
$t_{RP}$	Read pulse width	
$t_{WDSU}$	Data setup time before falling edge of write pulse	(5)
$t_{WDH}$	Data hold time after falling edge of write pulse	(5)
$t_{WASU}$	Address setup time before rising edge of write pulse	(5)
$t_{WAH}$	Address hold time after falling edge of write pulse	(5)
$t_{RASU}$	Address setup time before rising edge of read pulse	
$t_{RAH}$	Address hold time after falling edge of read pulse	
$t_{WO}$	Write enable to data output valid delay	
$t_{DD}$	Data-in to data-out valid delay	
$t_{EABOUT}$	Data-out delay	
$t_{EABCH}$	Clock high time	
$t_{EABCL}$	Clock low time	

Table 26. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
$t_{DIN2LE}$	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	(7)
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TROWROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

**Notes to tables:**

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial or industrial and extended use in ACEX 1K devices
- (3) Operating conditions:  $V_{CCIO} = 2.5\text{ V} \pm 5\%$  for commercial or industrial and extended use in ACEX 1K devices.
- (4) Operating conditions:  $V_{CCIO} = 2.5\text{ V}$  or  $3.3\text{ V}$ .
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the  $WE$  signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.



Tables 27 through 29 describe the ACEX 1K external timing parameters and their symbols.

Table 27. External Reference Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{\text{DRR}}$	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	(2)

Table 28. External Timing Parameters

Symbol	Parameter	Conditions
$t_{\text{INSU}}$	Setup time with global clock at IOE register	(3)
$t_{\text{INH}}$	Hold time with global clock at IOE register	(3)
$t_{\text{OUTCO}}$	Clock-to-output delay with global clock at IOE register	(3)
$t_{\text{PCISU}}$	Setup time with global clock for registers used in PCI designs	(3), (4)
$t_{\text{PCIH}}$	Hold time with global clock for registers used in PCI designs	(3), (4)
$t_{\text{PCICO}}$	Clock-to-output delay with global clock for registers used in PCI designs	(3), (4)

Table 29. External Bidirectional Timing Parameters *Note (3)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{INHBIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	CI = 35 pF
$t_{\text{XZBIDIR}}$	Synchronous IOE output buffer disable delay	CI = 35 pF
$t_{\text{ZXBIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate = off	CI = 35 pF

**Notes to tables:**

- (1) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
- (2) Contact Altera Applications for test circuit specifications and test conditions.
- (3) These timing parameters are sample-tested only.
- (4) This parameter is measured with the measurement and test conditions, including load, specified in the *PCI Local Bus Specification, Revision 2.2*.

Table 43. EP1K30 External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (3)	2.8		3.9		5.2		ns
t <sub>INHBIDIR</sub> (3)	0.0		0.0		0.0		ns
t <sub>INSUBIDIR</sub> (4)	3.8		4.9		–		ns
t <sub>INHBIDIR</sub> (4)	0.0		0.0		–		ns
t <sub>OUTCOBIDIR</sub> (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t <sub>XZBIDIR</sub> (3)		6.1		7.5		9.7	ns
t <sub>ZXBIDIR</sub> (3)		6.1		7.5		9.7	ns
t <sub>OUTCOBIDIR</sub> (4)	0.5	3.9	0.5	4.9	–	–	ns
t <sub>XZBIDIR</sub> (4)		5.1		6.5		–	ns
t <sub>ZXBIDIR</sub> (4)		5.1		6.5		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 22 through 29 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 44 through 50 show EP1K50 device external timing parameters.

Table 44. EP1K50 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.6		0.8		1.1	ns
$t_{CLUT}$		0.5		0.6		0.8	ns
$t_{RLUT}$		0.6		0.7		0.9	ns
$t_{PACKED}$		0.2		0.3		0.4	ns
$t_{EN}$		0.6		0.7		0.9	ns
$t_{CICO}$		0.1		0.1		0.1	ns
$t_{CGEN}$		0.4		0.5		0.6	ns
$t_{CGENR}$		0.1		0.1		0.1	ns
$t_{CASC}$		0.5		0.8		1.0	ns
$t_C$		0.5		0.6		0.8	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

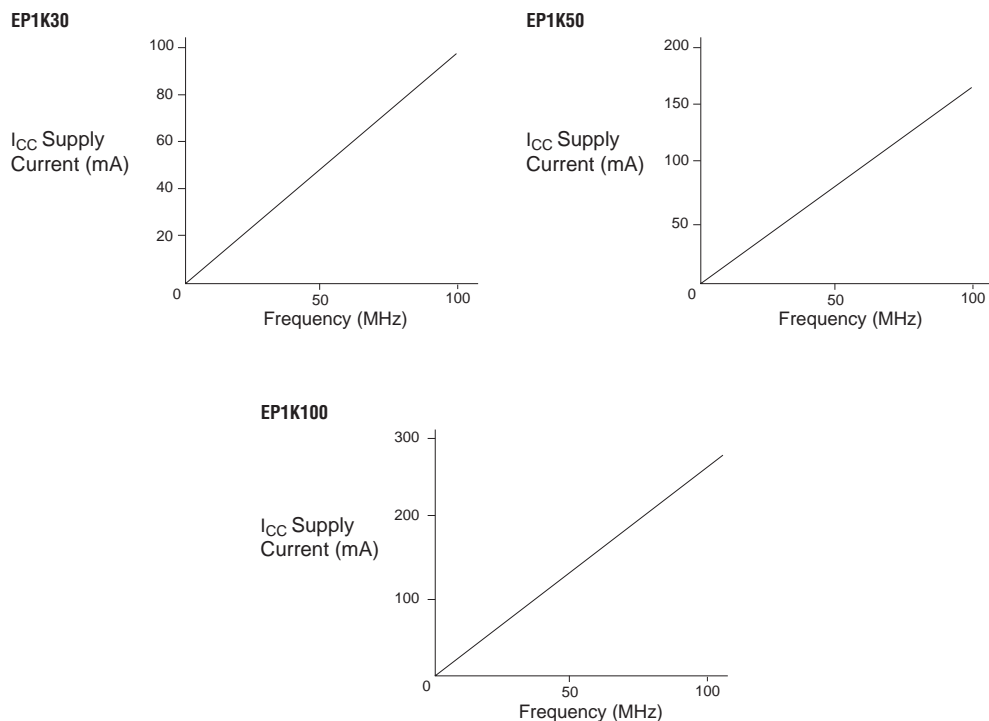
Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATA CO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

Table 50. EP1K50 External Bidirectional Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (2)	2.7		3.2		4.3		ns
t <sub>INHBIDIR</sub> (2)	0.0		0.0		0.0		ns
t <sub>INSUBIDIR</sub> (3)	3.7		4.2		–		ns
t <sub>INHBIDIR</sub> (3)	0.0		0.0		–		ns
t <sub>OUTCOBIDIR</sub> (2)	2.0	4.5	2.0	5.2	2.0	7.3	ns
t <sub>XZBIDIR</sub> (2)		6.8		7.8		10.1	ns
t <sub>ZXBIDIR</sub> (2)		6.8		7.8		10.1	ns
t <sub>OUTCOBIDIR</sub> (3)	0.5	3.5	0.5	4.2	–	–	
t <sub>XZBIDIR</sub> (3)		6.8		8.4		–	ns
t <sub>ZXBIDIR</sub> (3)		6.8		8.4		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 22 through 29.
- (2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
- (3) This parameter is measured with use of the ClockLock or ClockBoost circuits

Figure 31. ACEX 1K  $I_{CCACTIVE}$  vs. Operating Frequency

## Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as  $V_{CC}$  rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50  $\mu$ s.



When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.