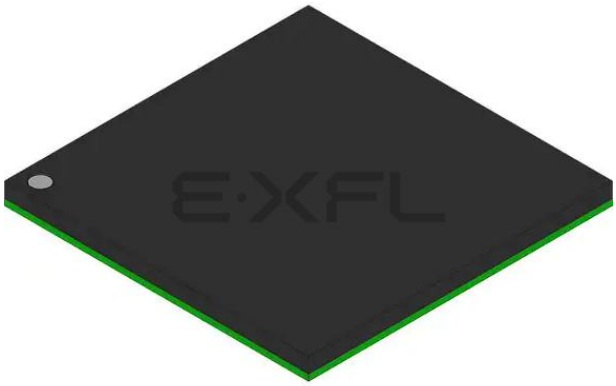

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	72
Number of Logic Elements/Cells	576
Total RAM Bits	-
Number of I/O	136
Number of Gates	-
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1k10fc256-1

General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 4. ACEX 1K Device Performance

Application	Resources Used		Performance			
	LEs	EABs	Speed Grade			Units
			-1	-2	-3	
16-bit loadable counter	16	0	285	232	185	MHz
16-bit accumulator	16	0	285	232	185	MHz
16-to-1 multiplexer *(1)*	10	0	3.5	4.5	6.6	ns
16-bit multiplier with 3-stage pipeline*(2)*	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed *(2)*	0	1	278	196	143	MHz
256 × 16 RAM write cycle speed *(2)*	0	1	185	143	111	MHz

Notes:
(1) This application uses combinatorial inputs and outputs.
(2) This application uses registered inputs and outputs.

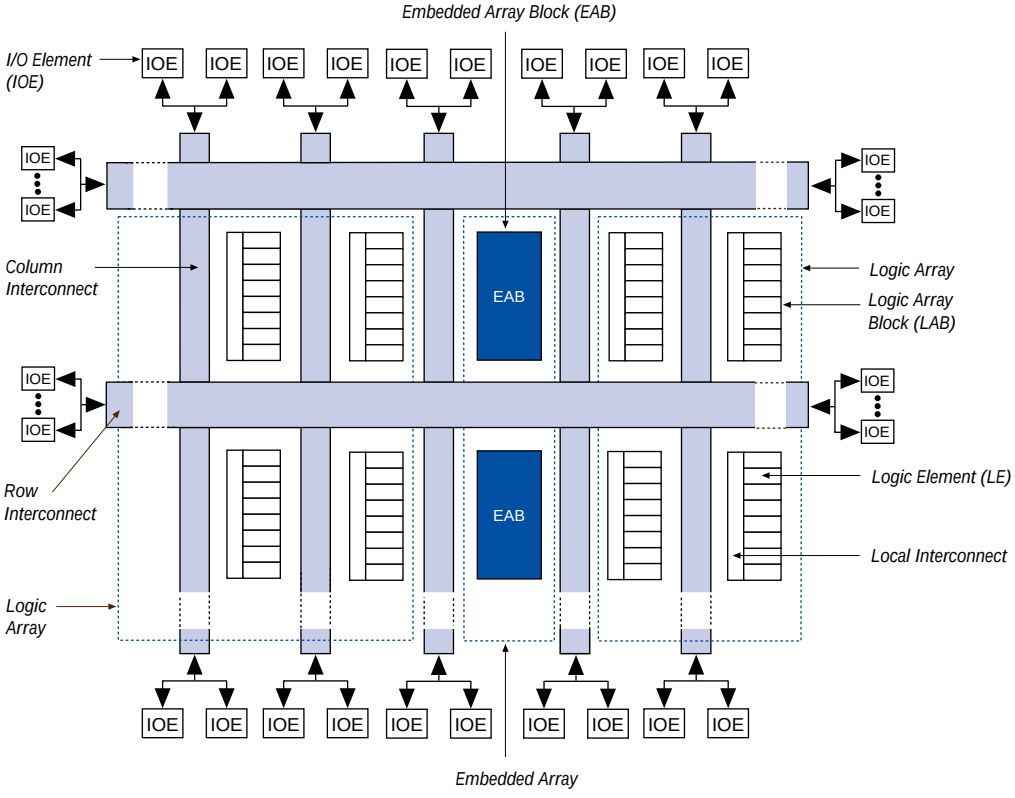
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input LUT, a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable logic gates.

Signal interconnections within ACEX 1K devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I / O pin is fed by an I / O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I / O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.1 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 2.5 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

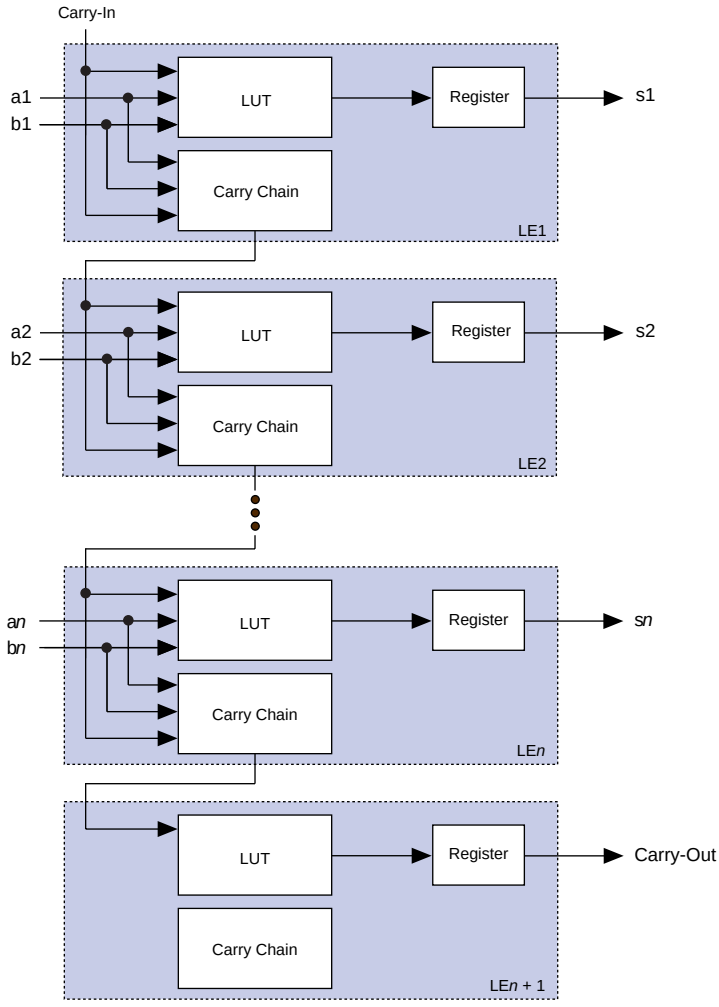
Figure 1 shows a block diagram of the ACEX 1K device architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 1. ACEX 1K Device Block Diagram



ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)



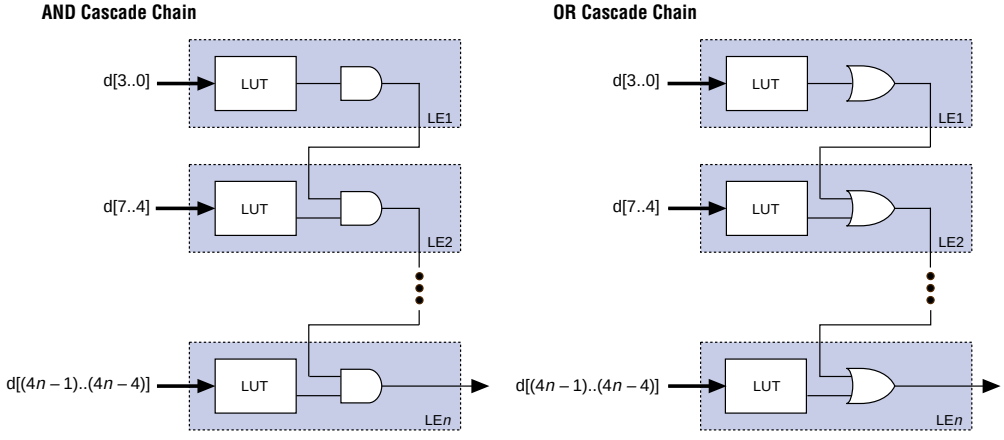
Cascade Chain

With the cascade chain, the ACEX 1K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. With a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EP1K50 device, the cascade chain stops at the eighteenth LAB, and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is 1.3 ns; the cascade chain delay is 0.6 ns. With the cascade chain, decoding a 16-bit address requires 3.1 ns.

Figure 10. ACEX 1K Cascade Chain Operation



FastTrack Interconnect Routing Structure

In the ACEX 1K architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

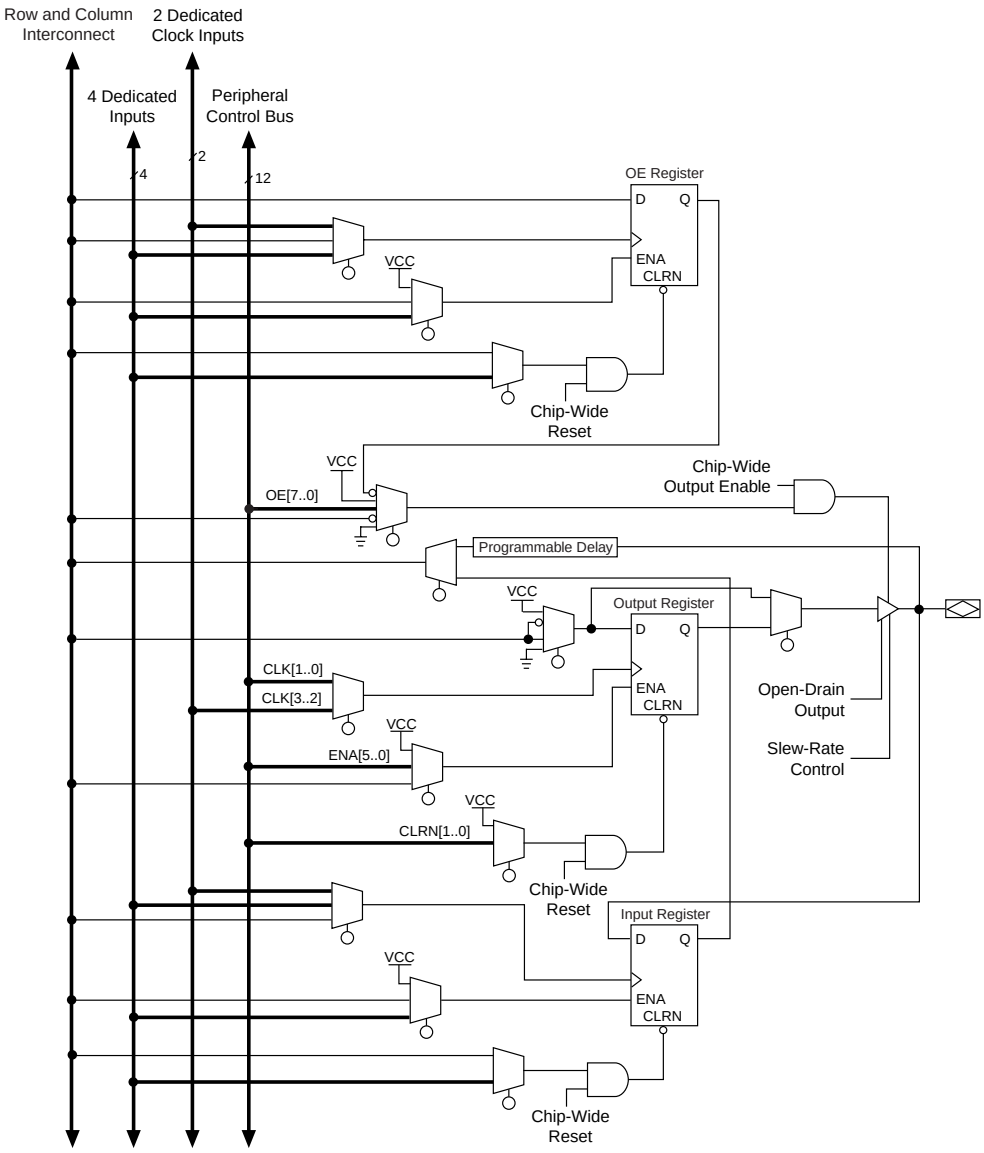
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently. Figure 13 shows the ACEX 1K LAB.

Figure 15. ACEX 1K Bidirectional I/O Registers



PCI Pull-Up Clamping Diode Option

ACEX 1K devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When V_{CCIO} is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which allows a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

Open-Drain Output Option

ACEX 1K devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

MultiVolt I/O Interface

The ACEX 1K device architecture supports the MultiVolt I/O interface feature, which allows ACEX 1K devices in all packages to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All ACEX 1K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. ACEX 1K devices can also be configured using the JTAG pins through the ByteBlasterMV or BitBlaster download cable, or via hardware that uses the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. ACEX 1K devices support the JTAG instructions shown in Table 14.

Table 14. ACEX 1K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, allowing the BST data to pass synchronously through a selected device to adjacent devices during normal operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring an ACEX 1K device via JTAG ports using a MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor.

The instruction register length of ACEX 1K devices is 10 bits. The USERCODE register length in ACEX 1K devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. Tables 15 and 16 show the boundary-scan register length and device IDCODE information for ACEX 1K devices.

Table 15. ACEX 1K Boundary-Scan Register Length

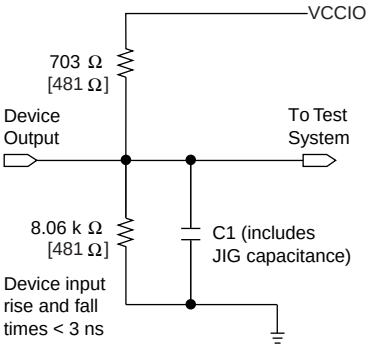
Device	Boundary-Scan Register Length
EP1K10	438
EP1K30	690
EP1K50	798
EP1K100	1,050

Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. ACEX 1K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



Operating Conditions

Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

Table 18. ACEX 1K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	° C

Table 26. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	*(7)*
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial and extended use in ACEX 1K devices
(3) Operating conditions: V_{CCIO} = 2.5 V ± 5% for commercial or industrial and extended use in ACEX 1K devices.
(4) Operating conditions: V_{CCIO} = 2.5 V or 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Tables 27 through 29 describe the ACEX 1K external timing parameters and their symbols.

Table 27. External Reference Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(2)*

Table 28. External Timing Parameters

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	*(3)*
t_{INH}	Hold time with global clock at IOE register	*(3)*
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	*(3)*
t_{PCISU}	Setup time with global clock for registers used in PCI designs	*(3)*, *(4)*
t_{PCIH}	Hold time with global clock for registers used in PCI designs	*(3)*, *(4)*
t_{PCICO}	Clock-to-output delay with global clock for registers used in PCI designs	*(3)*, *(4)*

Table 29. External Bidirectional Timing Parameters *Note (3)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	CI = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	CI = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	CI = 35 pF

Notes to tables:

(1) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(2) Contact Altera Applications for test circuit specifications and test conditions.
(3) These timing parameters are sample-tested only.
(4) This parameter is measured with the measurement and test conditions, including load, specified in the ***PCI Local Bus Specification, Revision 2.2.***

Tables 30 through 36 show EP1K10 device internal and external timing parameters.

Table 30. EP1K10 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		0.9		1.0		1.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.7		0.9		1.1	ns
t_{C}		1.1		1.3		1.7	ns
t_{CO}		0.5		0.7		0.9	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.7		0.8		1.0		ns
t_{H}	0.9		1.0		1.1		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABBYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

Table 33. EP1K10 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		6.7		7.3		7.3	ns
$t_{EABRCCOMB}$	6.7		7.3		7.3		ns
$t_{EABRCREG}$	4.7		4.9		4.9		ns
t_{EABWP}	2.7		2.8		2.8		ns
$t_{EABWCCOMB}$	6.4		6.7		6.7		ns
$t_{EABWCREG}$	7.4		7.6		7.6		ns
t_{EABDD}		6.0		6.5		6.5	ns
$t_{EABDATACO}$		0.8		0.9		0.9	ns
$t_{EABDATASU}$	1.6		1.7		1.7		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.4		1.4		1.4		ns
t_{EABWEH}	0.1		0.0		0.0		ns
$t_{EABWDSU}$	1.6		1.7		1.7		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.1		3.4		3.4		ns
t_{EABWAH}	0.6		0.5		0.5		ns
t_{EABWO}		5.4		5.8		5.8	ns

Table 34. EP1K10 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.3		2.7		3.6	ns
t_{DIN2LE}		0.8		1.1		1.4	ns
$t_{DIN2DATA}$		1.1		1.4		1.8	ns
$t_{DCLK2IOE}$		2.3		2.7		3.6	ns
$t_{DCLK2LE}$		0.8		1.1		1.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.8		2.1		2.9	ns
$t_{SAMECOLUMN}$		0.3		0.4		0.7	ns
$t_{DIFFROW}$		2.1		2.5		3.6	ns
$t_{TWOROWS}$		3.9		4.6		6.5	ns
$t_{LEPERIPH}$		3.3		3.7		4.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.0		1.4	ns

Table 35. EP1K10 External Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		7.5		9.5		12.5	ns
t_{INSU} *(2), (3)*	2.4		2.7		3.6		ns
t_{INH} *(2), (3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(2), (3)*	2.0	6.6	2.0	7.8	2.0	9.6	ns
t_{INSU} *(4), (3)*	1.4		1.7		–		ns
t_{INH} *(4), (3)*	0.5	5.1	0.5	6.4	–	–	ns
t_{OUTCO} *(4), (3)*	0.0		0.0		–		ns
t_{PCISU} *(3)*	3.0		4.2		6.4		ns
t_{PCIH} *(3)*	0.0		0.0		–		ns
t_{PCICO} *(3)*	2.0	6.0	2.0	7.5	2.0	10.2	ns

Table 36. EP1K10 External Bidirectional Timing Parameters *Notes (1), (3)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (2)	2.2		2.3		3.2		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	2.0	6.6	2.0	7.8	2.0	9.6	ns
$t_{XZBIDIR}$ (2)		8.8		11.2		14.0	ns
$t_{ZXBIDIR}$ (2)		8.8		11.2		14.0	ns
$t_{INSUBIDIR}$ (4)	3.1		3.3		–	–	
$t_{INHBIDIR}$ (4)	0.0		0.0		–		
$t_{OUTCOBIDIR}$ (4)	0.5	5.1	0.5	6.4	–	–	ns
$t_{XZBIDIR}$ (4)		7.3		9.2		–	ns
$t_{ZXBIDIR}$ (4)		7.3		9.2		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 22 through 29 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) These parameters are specified by characterization.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.8		1.0	ns
t_{C}		0.0		0.0		0.0	ns
t_{CO}		0.3		0.4		0.5	ns

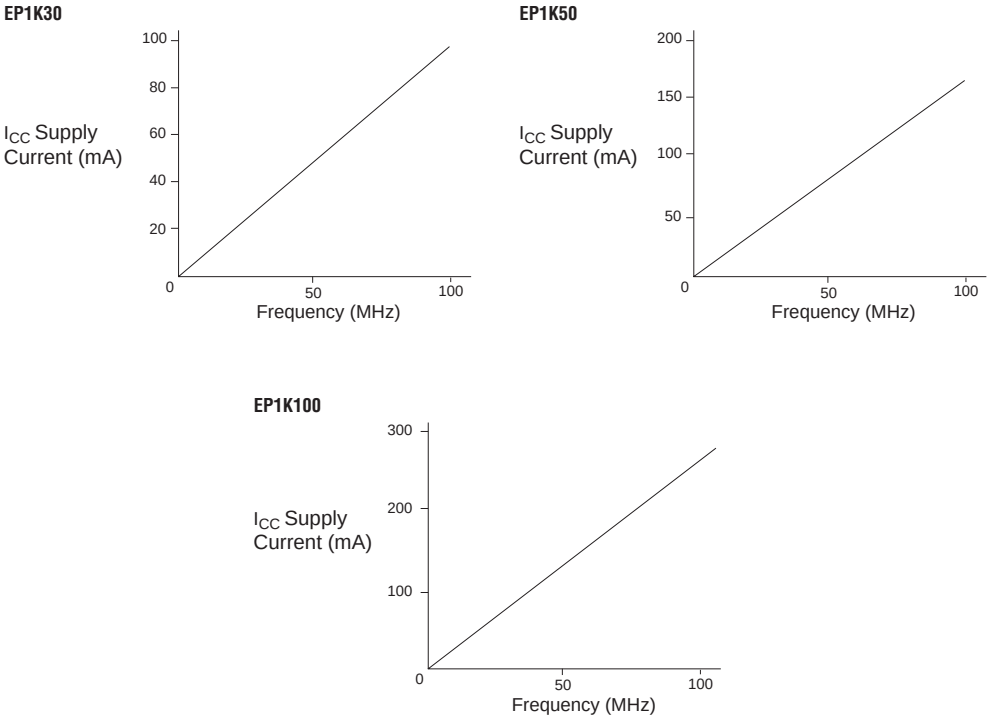
Table 37. EP1K30 Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{COMB}		0.4		0.4		0.6	ns
t_{SU}	0.4		0.6		0.6		ns
t_{H}	0.7		1.0		1.3		ns
t_{PRE}		0.8		0.9		1.2	ns
t_{CLR}		0.8		0.9		1.2	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 38. EP1K30 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.4		2.8		3.8	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		1.0		1.1		1.6	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.2		1.4		1.9		ns
t_{IOH}	0.3		0.4		0.5		ns
t_{IOCLR}		1.0		1.1		1.6	ns
t_{OD1}		1.9		2.3		3.0	ns
t_{OD2}		1.4		1.8		2.5	ns
t_{OD3}		4.4		5.2		7.0	ns
t_{XZ}		2.7		3.1		4.3	ns
t_{ZX1}		2.7		3.1		4.3	ns
t_{ZX2}		2.2		2.6		3.8	ns
t_{ZX3}		5.2		6.0		8.3	ns
t_{INREG}		3.4		4.1		5.5	ns
t_{IOFD}		0.8		1.3		2.4	ns
t_{INCOMB}		0.8		1.3		2.4	ns

Figure 31. ACEX 1K $I_{CCACTIVE}$ vs. Operating Frequency



Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50 µs.

When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.

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