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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 72 |
| Number of Logic Elements/Cells | 576 |
| Total RAM Bits | 12288 |
| Number of I/O | 136 |
| Number of Gates | 56000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1k10fc256-1n |

# General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

*Table 4. ACEX 1K Device Performance*

| Application | Resources Used | | Performance | | | |
|---|---|---|---|---|---|---|
| | LEs | EABs | Speed Grade | | | Units |
| | | | -1 | -2 | -3 | |
| 16-bit loadable counter | 16 | 0 | 285 | 232 | 185 | MHz |
| 16-bit accumulator | 16 | 0 | 285 | 232 | 185 | MHz |
| 16-to-1 multiplexer *(1)* | 10 | 0 | 3.5 | 4.5 | 6.6 | ns |
| 16-bit multiplier with 3-stage pipeline *(2)* | 592 | 0 | 156 | 131 | 93 | MHz |
| 256 × 16 RAM read cycle speed *(2)* | 0 | 1 | 278 | 196 | 143 | MHz |
| 256 × 16 RAM write cycle speed *(2)* | 0 | 1 | 185 | 143 | 111 | MHz |

*Notes:*

(1)   This application uses combinatorial inputs and outputs.
(2)   This application uses registered inputs and outputs.

Table 5 shows ACEX 1K device performance for more complex designs. These designs are available as Altera MegaCore™ functions.

*Table 5. ACEX 1K Device Performance for Complex Designs*

| Application | LEs Used | Performance | | | Units |
|---|---|---|---|---|---|
| | | Speed Grade | | | |
| | | -1 | -2 | -3 | |
| 16-bit, 8-tap parallel finite impulse response (FIR) filter | 597 | 192 | 156 | 116 | MSPS |
| 8-bit, 512-point Fast Fourier transform (FFT) function | 1,854 | 23.4 | 28.7 | 38.9 | µs |
| | | 113 | 92 | 68 | MHz |
| a16450 universal asynchronous receiver/transmitter (UART) | 342 | 36 | 28 | 20.5 | MHz |

Each ACEX 1K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

ACEX 1K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers EPC16, EPC2, EPC1, and EPC1441 configuration devices, which configure ACEX 1K devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cables. After an ACEX 1K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 40 ms, real-time changes can be made during system operation.

ACEX 1K devices contain an interface that permits microprocessors to configure ACEX 1K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat an ACEX 1K device as memory and configure it by writing to a virtual memory location, simplifying device reconfiguration.

For more information on the configuration of ACEX 1K devices, see the following documents:

- *Configuration Devices for ACEX, APEX, FLEX, & Mercury Devices Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*

ACEX 1K devices are supported by Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the ACEX 1K device architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

# Functional Description

Each ACEX 1K device contains an enhanced embedded array that implements memory and specialized logic functions, and a logic array that implements general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

*Figure 1. ACEX 1K Device Block Diagram*
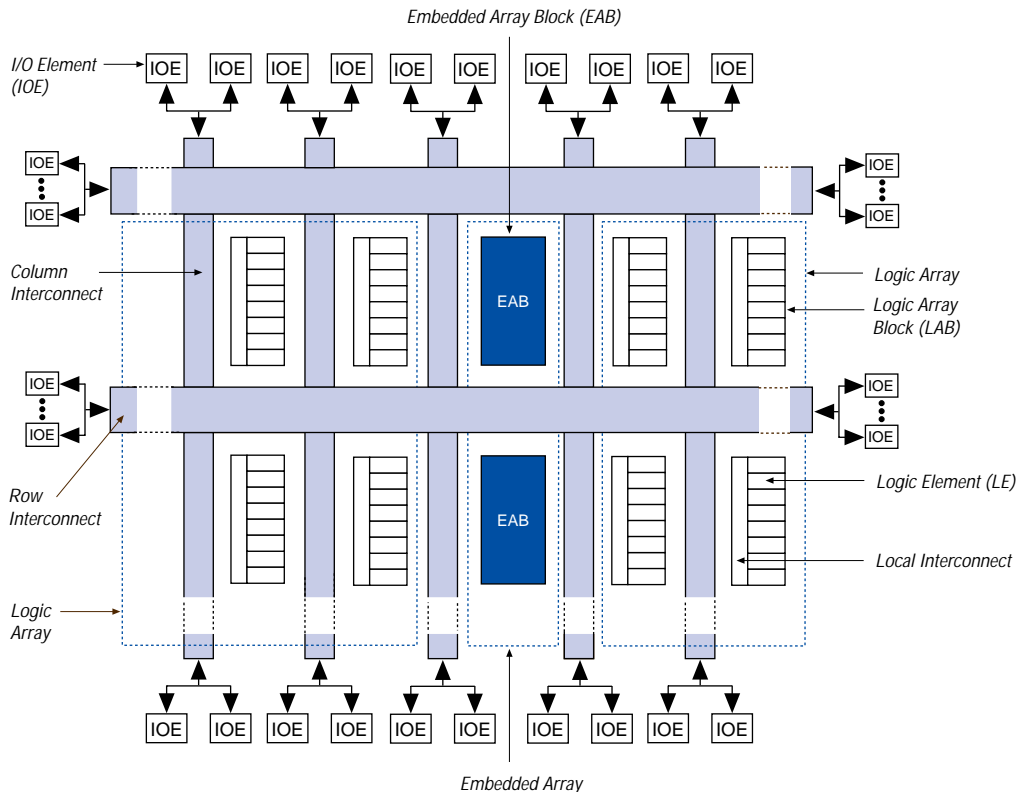


ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

*Figure 2. ACEX 1K Device in Dual-Port RAM Mode*   *Note (1)*
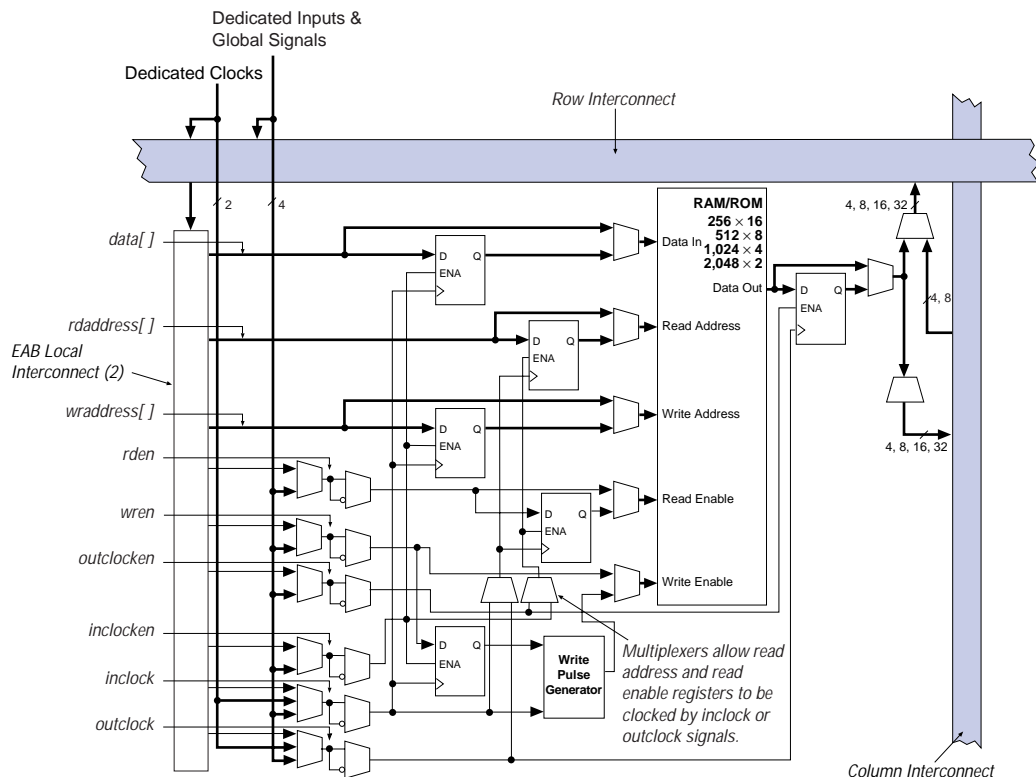


**Notes:**
(1)   All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
(2)   EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: $256 \times 16$; $512 \times 8$; $1,024 \times 4$; or $2,048 \times 2$. Figure 5 shows the ACEX 1K EAB memory configurations.

*Figure 5. ACEX 1K EAB Memory Configurations*



| $256 \times 16$ | $512 \times 8$ | $1,024 \times 4$ | $2,048 \times 2$ |
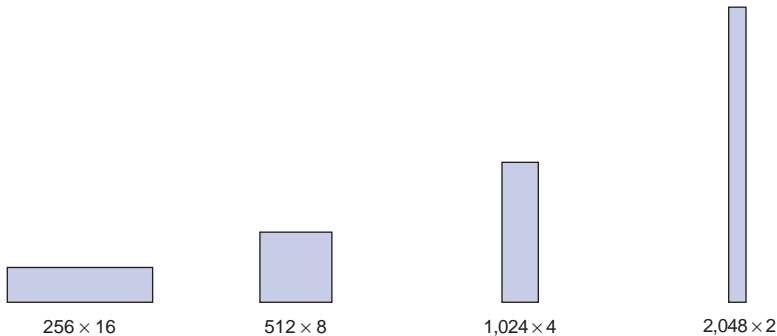
Larger blocks of RAM are created by combining multiple EABs. For example, two $256 \times 16$ RAM blocks can be combined to form a $256 \times 32$ block, and two $512 \times 8$ RAM blocks can be combined to form a $512 \times 16$ block. Figure 6 shows examples of multiple EAB combination.

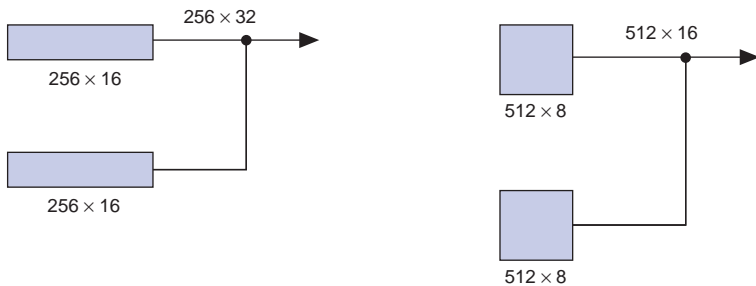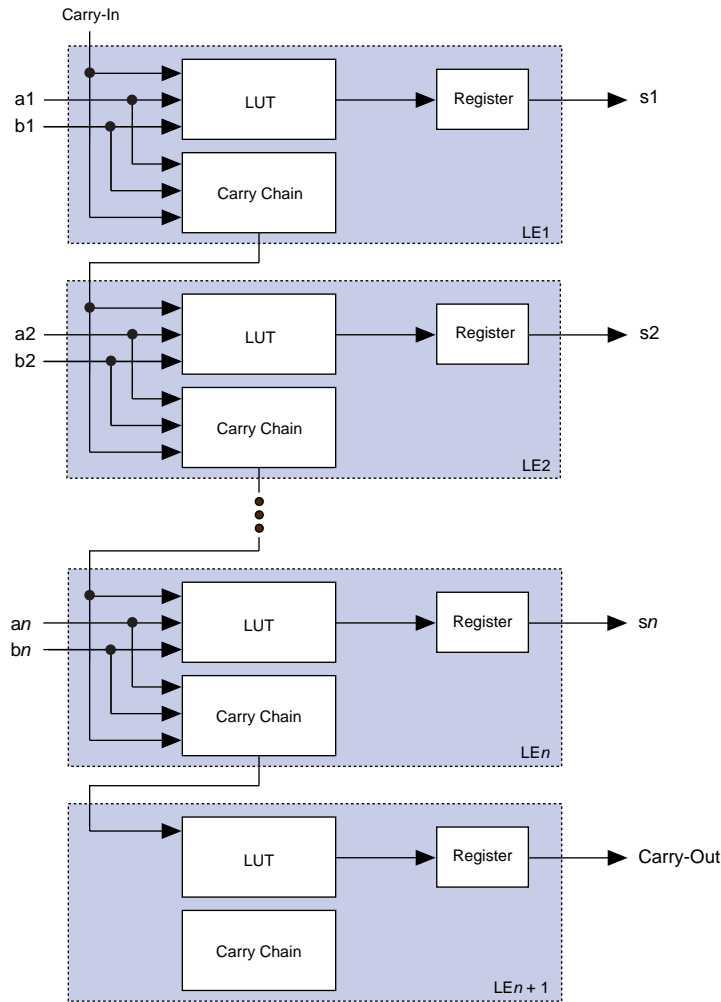*Figure 6. Examples of Combining ACEX 1K EABs*

*Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)*

*Cascade Chain*

With the cascade chain, the ACEX 1K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. With a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EP1K50 device, the cascade chain stops at the eighteenth LAB, and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with $n$ LEs. The LE delay is 1.3 ns; the cascade chain delay is 0.6 ns. With the cascade chain, decoding a 16-bit address requires 3.1 ns.

*Figure 10. ACEX 1K Cascade Chain Operation*
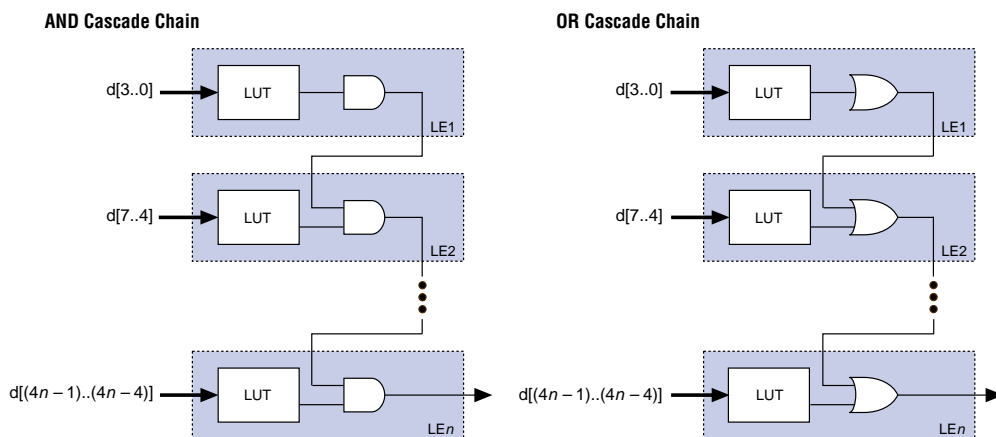
For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 6 summarizes the FastTrack Interconnect routing structure resources available in each ACEX 1K device.

*Table 6. ACEX 1K FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|--------|------|------------------|---------|---------------------|
| EP1K10 | 3 | 144 | 24 | 24 |
| EP1K30 | 6 | 216 | 36 | 24 |
| EP1K50 | 10 | 216 | 36 | 24 |
| EP1K100 | 12 | 312 | 52 | 24 |

In addition to general-purpose I/O pins, ACEX 1K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output-enable and clock-enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

*Column-to-IOE Connections*

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

*Figure 17. ACEX 1K Column-to-IOE Connections*   *Note (1)*

Each IOE is driven by
a m-to-1 multiplexer

Column
Interconnect

Each IOE can drive two
column channels.
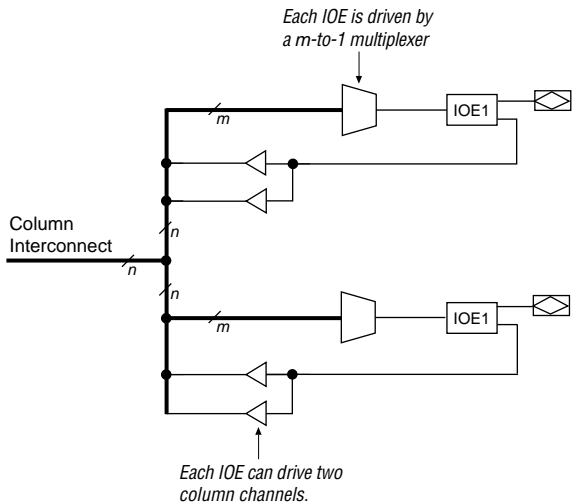
*Note:*
(1)    The values for *m* and *n* are shown in Table 9.

Table 9 lists the ACEX 1K column-to-IOE interconnect resources.

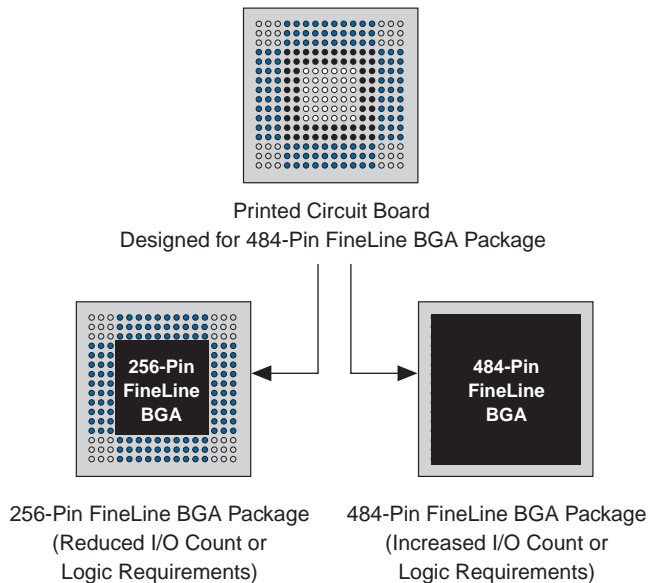*Table 9.  ACEX 1K Column-to-IOE Interconnect Resources*

| Device | Channels per Column (n) | Column Channels per Pin (m) |
|---|---|---|
| EP1K10 | 24 | 16 |
| EP1K30 | 24 | 16 |
| EP1K50 | 24 | 16 |
| EP1K100 | 24 | 16 |

## SameFrame Pin-Outs

ACEX 1K devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EP1K10 device in a 256-pin FineLine BGA package to an EP1K100 device in a 484-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board that takes advantage of this migration. Figure 18 shows an example of SameFrame pin-out.

*Figure 18. SameFrame Pin-Out Example*



Printed Circuit Board
Designed for 484-Pin FineLine BGA Package

256-Pin FineLine BGA

484-Pin FineLine BGA

256-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

484-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)

Table 10 shows the ACEX 1K device/package combinations that support SameFrame pin-outs for ACEX 1K devices. All FineLine BGA packages support SameFrame pin-outs, providing the flexibility to migrate not only from device to device within the same package, but also from one package to another. The I/O count will vary from device to device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the GCLK1 pin. In the Altera software, the GCLK1 pin can feed both the ClockLock and ClockBoost circuitry in the ACEX 1K device. However, when both circuits are used, the other clock pin cannot be used.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

*Figure 19. Specifications for the Incoming & Generated Clocks    Note (1)*
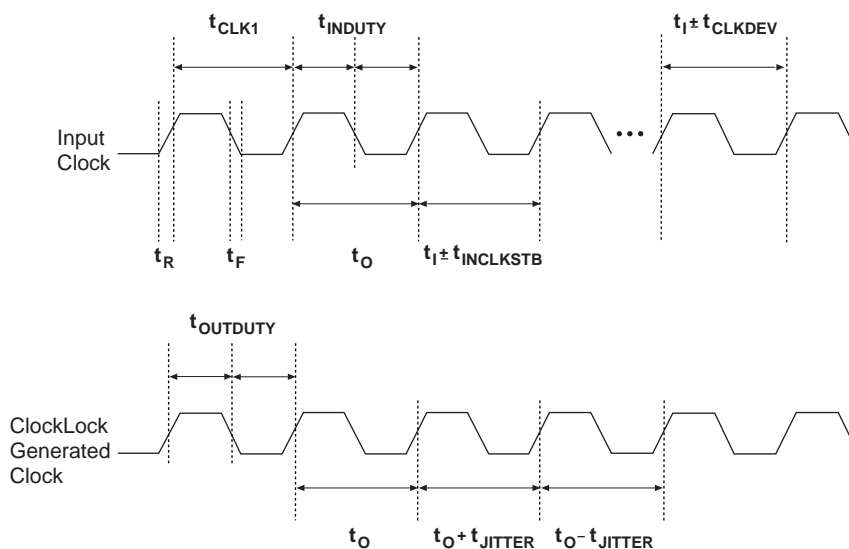


*Note:*

(1)    The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.

### PCI Pull-Up Clamping Diode Option

ACEX 1K devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which allows a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

### Open-Drain Output Option

ACEX 1K devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

### MultiVolt I/O Interface

The ACEX 1K device architecture supports the MultiVolt I/O interface feature, which allows ACEX 1K devices in all packages to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

*Table 26. Interconnect Timing Microparameters*    *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{DIN2IOE}$ | Delay from dedicated input pin to IOE control input | *(7)* |
| $t_{DIN2LE}$ | Delay from dedicated input pin to LE or EAB control input | *(7)* |
| $t_{DIN2DATA}$ | Delay from dedicated input or clock to LE or EAB data | *(7)* |
| $t_{DCLK2IOE}$ | Delay from dedicated clock pin to IOE clock | *(7)* |
| $t_{DCLK2LE}$ | Delay from dedicated clock pin to LE or EAB clock | *(7)* |
| $t_{SAMELAB}$ | Routing delay for an LE driving another LE in the same LAB | *(7)* |
| $t_{SAMEROW}$ | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row | *(7)* |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column | *(7)* |
| $t_{DIFFROW}$ | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{TWOROWS}$ | Routing delay for a row IOE or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{LEPERIPH}$ | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus | *(7)* |
| $t_{LABCARRY}$ | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB | |
| $t_{LABCASC}$ | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB | |

*Notes to tables:*

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions:   $V_{CCIO}$ = 3.3 V ± 10% for commercial or industrial and extended use in ACEX 1K devices

(3) Operating conditions:   $V_{CCIO}$ = 2.5 V ± 5% for commercial or industrial and extended use in ACEX 1K devices.

(4) Operating conditions:   $V_{CCIO}$ = 2.5 V or 3.3 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

## Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.8 | | 1.9 | | 1.9 | ns |
| $t_{EABDATA2}$ | | 0.6 | | 0.7 | | 0.7 | ns |
| $t_{EABWE1}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{EABRE1}$ | | 0.9 | | 0.9 | | 0.9 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.3 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{EABSU}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{EABH}$ | 0.5 | | 0.4 | | 0.4 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.3 | | ns |
| $t_{AA}$ | | 3.4 | | 3.6 | | 3.6 | ns |
| $t_{WP}$ | 2.7 | | 2.8 | | 2.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.8 | | 1.9 | | 1.9 | | ns |
| $t_{WAH}$ | 1.9 | | 2.0 | | 2.0 | | ns |
| $t_{RASU}$ | 3.1 | | 3.5 | | 3.5 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.2 | | ns |
| $t_{WO}$ | | 2.7 | | 2.8 | | 2.8 | ns |
| $t_{DD}$ | | 2.7 | | 2.8 | | 2.8 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.0 | | ns |
| $t_{EABCL}$ | 2.7 | | 2.8 | | 2.8 | | ns |

### Table 37. EP1K30 Device LE Timing Microparameters  (Part 2 of 2) *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|--------|-----|-----|-----|-----|-----|-----|------|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{COMB}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.6 | | ns |
| $t_{H}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{PRE}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CLR}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 2.5 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 2.5 | | ns |

### Table 38. EP1K30 Device IOE Timing Microparameters  *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|--------|-----|-----|-----|-----|-----|-----|------|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 2.4 | | 2.8 | | 3.8 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 1.2 | | 1.4 | | 1.9 | | ns |
| $t_{IOH}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{OD1}$ | | 1.9 | | 2.3 | | 3.0 | ns |
| $t_{OD2}$ | | 1.4 | | 1.8 | | 2.5 | ns |
| $t_{OD3}$ | | 4.4 | | 5.2 | | 7.0 | ns |
| $t_{XZ}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX1}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX2}$ | | 2.2 | | 2.6 | | 3.8 | ns |
| $t_{ZX3}$ | | 5.2 | | 6.0 | | 8.3 | ns |
| $t_{INREG}$ | | 3.4 | | 4.1 | | 5.5 | ns |
| $t_{IOFD}$ | | 0.8 | | 1.3 | | 2.4 | ns |
| $t_{INCOMB}$ | | 0.8 | | 1.3 | | 2.4 | ns |

**Altera Corporation**

## Table 40. EP1K30 Device EAB Internal Timing Macroparameters    *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 6.4 | | 7.6 | | 8.8 | ns |
| $t_{EABRCOMB}$ | 6.4 | | 7.6 | | 8.8 | | ns |
| $t_{EABRCREG}$ | 4.4 | | 5.1 | | 6.0 | | ns |
| $t_{EABWP}$ | 2.5 | | 2.9 | | 3.3 | | ns |
| $t_{EABWCOMB}$ | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{EABWCREG}$ | 6.8 | | 7.8 | | 9.0 | | ns |
| $t_{EABDD}$ | | 5.7 | | 6.7 | | 7.7 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{EABDATASU}$ | 1.5 | | 1.7 | | 2.0 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.3 | | 1.4 | | 1.7 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.5 | | 1.7 | | 2.0 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.0 | | 3.6 | | 4.3 | | ns |
| $t_{EABWAH}$ | 0.5 | | 0.5 | | 0.4 | | ns |
| $t_{EABWO}$ | | 5.1 | | 6.0 | | 6.8 | ns |

## Table 44. EP1K50 Device LE Timing Microparameters  (Part 2 of 2)   *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{CO}$ | | 0.6 | | 0.6 | | 0.7 | ns |
| $t_{COMB}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PRE}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

## Table 45. EP1K50 Device IOE Timing Microparameters   *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.3 | | 1.9 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{IOCO}$ | | 1.7 | | 2.1 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.4 | ns |
| $t_{OD1}$ | | 1.2 | | 1.2 | | 1.9 | ns |
| $t_{OD2}$ | | 0.7 | | 0.8 | | 1.7 | ns |
| $t_{OD3}$ | | 2.7 | | 3.0 | | 4.3 | ns |
| $t_{XZ}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX1}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX2}$ | | 4.2 | | 5.3 | | 7.3 | ns |
| $t_{ZX3}$ | | 6.2 | | 7.5 | | 9.9 | ns |
| $t_{INREG}$ | | 3.5 | | 4.2 | | 5.6 | ns |
| $t_{IOFD}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{INCOMB}$ | | 1.1 | | 1.3 | | 1.8 | ns |

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

| Symbol | Speed Grade | | | | | | Unit |
|--------|-----|-----|-----|-----|-----|-----|------|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 1.0 | | 1.5 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_C$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_H$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

*Table 51. EP1K100 Device LE Timing Microparameters    Note (1)*

*Figure 31. ACEX 1K $I_{CCACTIVE}$ vs. Operating Frequency*

**EP1K30**

$I_{CC}$ Supply
Current (mA)

Frequency (MHz)

**EP1K50**

$I_{CC}$ Supply
Current (mA)

Frequency (MHz)

**EP1K100**

$I_{CC}$ Supply
Current (mA)

Frequency (MHz)
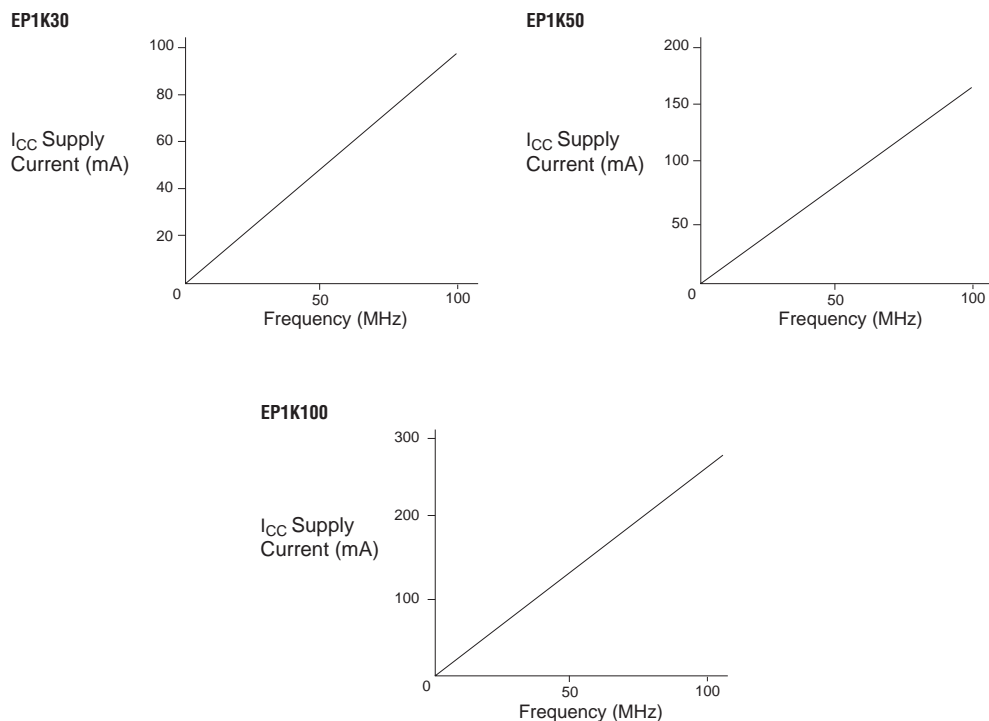
# Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

## Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as $V_{CC}$ rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50 μs.

☞ When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.