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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	72
Number of Logic Elements/Cells	576
Total RAM Bits	12288
Number of I/O	136
Number of Gates	56000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1k10fc256-3">https://www.e-xfl.com/product-detail/intel/ep1k10fc256-3</a>

- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Flexible package options are available in 100 to 484 pins, including the innovative FineLine BGA™ packages (see [Tables 2 and 3](#))
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplcity, VeriBest, and Viewlogic

**Table 2. ACEX 1K Package Options & I/O Pin Count** *Notes (1), (2)*

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	66	92	120	136	136 (3)
EP1K30		102	147	171	171 (3)
EP1K50		102	147	186	249
EP1K100			147	186	333

**Notes:**

- (1) ACEX 1K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and FineLine BGA packages.
- (2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
- (3) This option is supported with a 256-pin FineLine BGA package. By using SameFrame™ pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin and 484-pin FineLine BGA packages.

**Table 3. ACEX 1K Package Sizes**

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.0
Area (mm <sup>2</sup> )	256	484	936	289	529
Length × width (mm × mm)	16 × 16	22 × 22	30.6 × 30.6	17 × 17	23 × 23

Table 5 shows ACEX 1K device performance for more complex designs. These designs are available as Altera MegaCore™ functions.

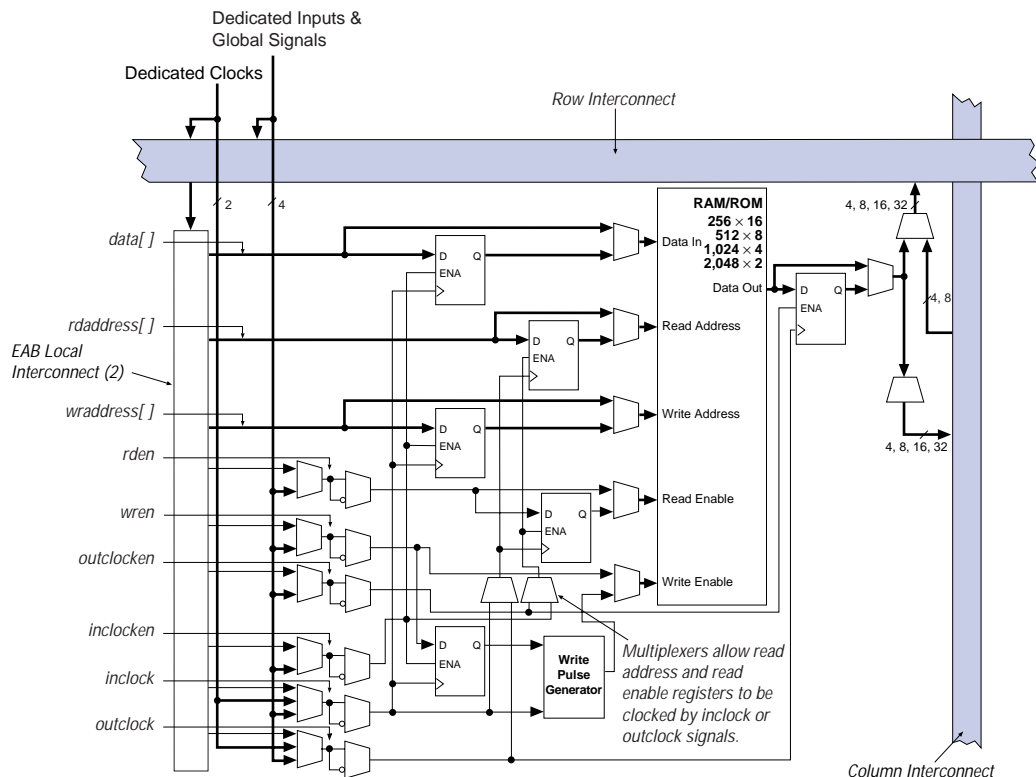
Table 5. ACEX 1K Device Performance for Complex Designs					
Application	LEs Used	Performance			
		Speed Grade			Units
		-1	-2	-3	
16-bit, 8-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point Fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	μs
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Each ACEX 1K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

ACEX 1K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers EPC16, EPC2, EPC1, and EPC1441 configuration devices, which configure ACEX 1K devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cables. After an ACEX 1K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 40 ms, real-time changes can be made during system operation.

ACEX 1K devices contain an interface that permits microprocessors to configure ACEX 1K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat an ACEX 1K device as memory and configure it by writing to a virtual memory location, simplifying device reconfiguration.

Figure 2. ACEX 1K Device in Dual-Port RAM Mode *Note (1)*



**Notes:**

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

Figure 3. ACEX 1K EAB in Dual-Port RAM Mode

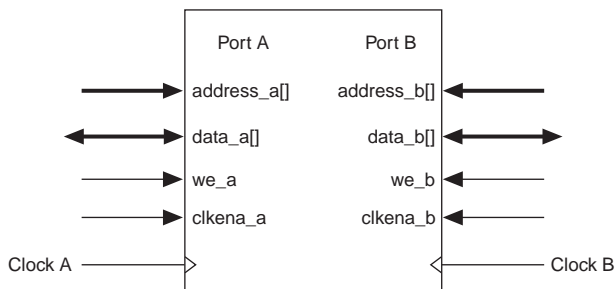
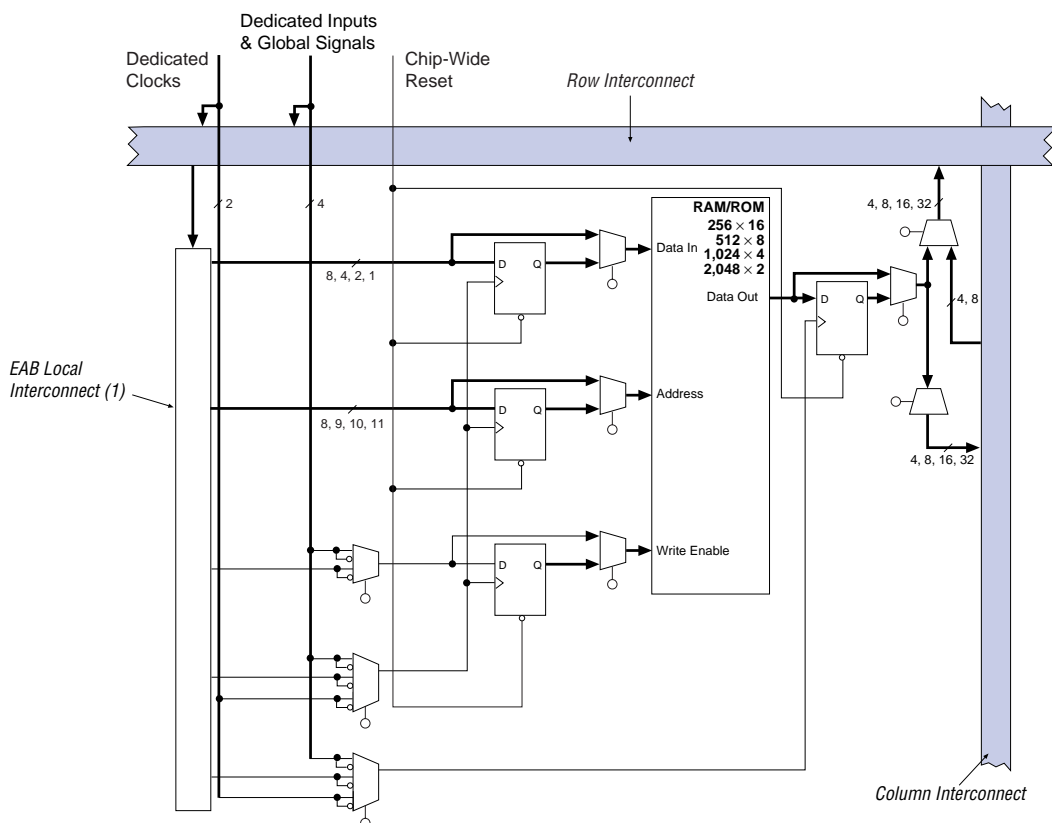


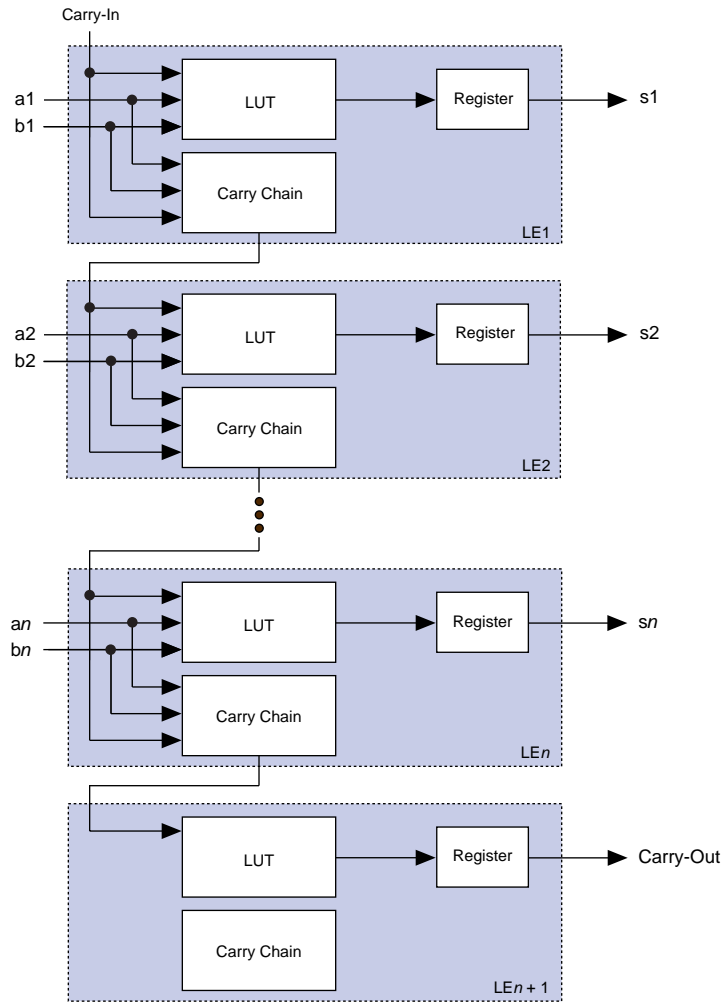
Figure 4. ACEX 1K Device in Single-Port RAM Mode



**Note:**

- (1) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)



## FastTrack Interconnect Routing Structure

In the ACEX 1K architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently. [Figure 13](#) shows the ACEX 1K LAB.

For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

**Table 6** summarizes the FastTrack Interconnect routing structure resources available in each ACEX 1K device.

<i>Table 6. ACEX 1K FastTrack Interconnect Resources</i>				
Device	Rows	Channels per Row	Columns	Channels per Column
EP1K10	3	144	24	24
EP1K30	6	216	36	24
EP1K50	10	216	36	24
EP1K100	12	312	52	24

In addition to general-purpose I/O pins, ACEX 1K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output-enable and clock-enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

**Figure 14** shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.



When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

**Table 7** lists the sources for each peripheral control signal and shows how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. **Table 7** also shows the rows that can drive global signals.

*Table 7. Peripheral Bus Sources for ACEX Devices*

Peripheral Control Signal	EP1K10	EP1K30	EP1K50	EP1K100
OE0	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C
OE2	Row B	Row C	Row D	Row E
OE3	Row B	Row D	Row F	Row L
OE4	Row C	Row E	Row H	Row I
OE5	Row C	Row F	Row J	Row K
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row F
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row C	Row D
CLKENA2/CLR0	Row B	Row C	Row E	Row B
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row G	Row H
CLKENA4/CLR1	Row C	Row E	Row I	Row J
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row J	Row G

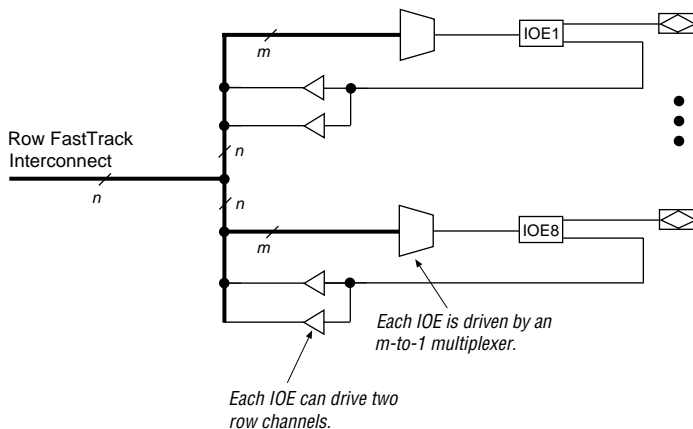
Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

The chip-wide output enable pin is an active-high pin that can be used to tri-state all pins on the device. This option can be set in the Altera software. The built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

### Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. ACEX 1K Row-to-IOE Connections *Note (1)*



**Note:**

(1) The values for  $m$  and  $n$  are shown in Table 8.

Table 8 lists the ACEX 1K row-to-IOE interconnect resources.

Table 8. ACEX 1K Row-to-IOE Interconnect Resources		
Device	Channels per Row ( $n$ )	Row Channels per Pin ( $m$ )
EP1K10	144	18
EP1K30	216	27
EP1K50	216	27
EP1K100	312	39

## PCI Pull-Up Clamping Diode Option

ACEX 1K devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the  $V_{CCIO}$  value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When  $V_{CCIO}$  is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When  $V_{CCIO}$  is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which allows a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

## Open-Drain Output Option

ACEX 1K devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## MultiVolt I/O Interface

The ACEX 1K device architecture supports the MultiVolt I/O interface feature, which allows ACEX 1K devices in all packages to interface with systems of differing supply voltages. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All ACEX 1K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. ACEX 1K devices can also be configured using the JTAG pins through the ByteBlasterMV or BitBlaster download cable, or via hardware that uses the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. ACEX 1K devices support the JTAG instructions shown in [Table 14](#).

**Table 14. ACEX 1K JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, allowing the BST data to pass synchronously through a selected device to adjacent devices during normal operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring an ACEX 1K device via JTAG ports using a MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor.

The instruction register length of ACEX 1K devices is 10 bits. The USERCODE register length in ACEX 1K devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. [Tables 15](#) and [16](#) show the boundary-scan register length and device IDCODE information for ACEX 1K devices.

**Table 15. ACEX 1K Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EP1K10	438
EP1K30	690
EP1K50	798
EP1K100	1,050

**Table 22. LE Timing Microparameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions
$t_{CASC}$	Cascade-in to cascade-out delay	
$t_C$	LE register control signal delay	
$t_{CO}$	LE register clock-to-output delay	
$t_{COMB}$	Combinatorial delay	
$t_{SU}$	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
$t_H$	LE register hold time for data and enable signals after clock	
$t_{PRE}$	LE register preset delay	
$t_{CLR}$	LE register clear delay	
$t_{CH}$	Minimum clock high time from clock pin	
$t_{CL}$	Minimum clock low time from clock pin	

**Table 23. IOE Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{IOD}$	IOE data delay	
$t_{IOC}$	IOE register control signal delay	
$t_{IOCO}$	IOE register clock-to-output delay	
$t_{IOCOMB}$	IOE combinatorial delay	
$t_{IOSU}$	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
$t_{IOH}$	IOE register hold time for data and enable signals after clock	
$t_{IOCLR}$	IOE register clear time	
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF (3)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
$t_{XZ}$	IOE output buffer disable delay	
$t_{ZX1}$	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF (2)
$t_{ZX2}$	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF (3)
$t_{ZX3}$	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
$t_{INREG}$	IOE input pad and buffer to IOE register delay	
$t_{OFD}$	IOE register feedback delay	
$t_{INCOMB}$	IOE input pad and buffer to FastTrack Interconnect delay	

Table 24. EAB Timing Microparameters <i>Note (1)</i>		
Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
$t_{EABWE1}$	Write enable delay to EAB for combinatorial input	
$t_{EABWE2}$	Write enable delay to EAB for registered input	
$t_{EABRE1}$	Read enable delay to EAB for combinatorial input	
$t_{EABRE2}$	Read enable delay to EAB for registered input	
$t_{EABCLK}$	EAB register clock delay	
$t_{EABCO}$	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
$t_{EABSU}$	EAB register setup time before clock	
$t_{EABH}$	EAB register hold time after clock	
$t_{EABCLR}$	EAB register asynchronous clear time to output delay	
$t_{AA}$	Address access delay (including the read enable to output delay)	
$t_{WP}$	Write pulse width	
$t_{RP}$	Read pulse width	
$t_{WDSU}$	Data setup time before falling edge of write pulse	(5)
$t_{WDH}$	Data hold time after falling edge of write pulse	(5)
$t_{WASU}$	Address setup time before rising edge of write pulse	(5)
$t_{WAH}$	Address hold time after falling edge of write pulse	(5)
$t_{RASU}$	Address setup time before rising edge of read pulse	
$t_{RAH}$	Address hold time after falling edge of read pulse	
$t_{WO}$	Write enable to data output valid delay	
$t_{DD}$	Data-in to data-out valid delay	
$t_{EABOUT}$	Data-out delay	
$t_{EABCH}$	Clock high time	
$t_{EABCL}$	Clock low time	

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
$t_{EABWE1}$		1.2		1.2		1.2	ns
$t_{EABWE2}$		0.4		0.4		0.4	ns
$t_{EABRE1}$		0.9		0.9		0.9	ns
$t_{EABRE2}$		0.4		0.4		0.4	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.3		0.3	ns
$t_{EABYPASS}$		0.5		0.6		0.6	ns
$t_{EABSU}$	1.0		1.0		1.0		ns
$t_{EABH}$	0.5		0.4		0.4		ns
$t_{EABCLR}$	0.3		0.3		0.3		ns
$t_{AA}$		3.4		3.6		3.6	ns
$t_{WP}$	2.7		2.8		2.8		ns
$t_{RP}$	1.0		1.0		1.0		ns
$t_{WDSU}$	1.0		1.0		1.0		ns
$t_{WDH}$	0.1		0.1		0.1		ns
$t_{WASU}$	1.8		1.9		1.9		ns
$t_{WAH}$	1.9		2.0		2.0		ns
$t_{RASU}$	3.1		3.5		3.5		ns
$t_{RAH}$	0.2		0.2		0.2		ns
$t_{WO}$		2.7		2.8		2.8	ns
$t_{DD}$		2.7		2.8		2.8	ns
$t_{EABOUT}$		0.5		0.6		0.6	ns
$t_{EABCH}$	1.5		2.0		2.0		ns
$t_{EABCL}$	2.7		2.8		2.8		ns

Table 36. EP1K10 External Bidirectional Timing Parameters *Notes (1), (3)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (2)	2.2		2.3		3.2		ns
t <sub>INHBIDIR</sub> (2)	0.0		0.0		0.0		ns
t <sub>OUTCOBIDIR</sub> (2)	2.0	6.6	2.0	7.8	2.0	9.6	ns
t <sub>XZBIDIR</sub> (2)		8.8		11.2		14.0	ns
t <sub>ZXBIDIR</sub> (2)		8.8		11.2		14.0	ns
t <sub>INSUBIDIR</sub> (4)	3.1		3.3		–	–	
t <sub>INHBIDIR</sub> (4)	0.0		0.0		–		
t <sub>OUTCOBIDIR</sub> (4)	0.5	5.1	0.5	6.4	–	–	ns
t <sub>XZBIDIR</sub> (4)		7.3		9.2		–	ns
t <sub>ZXBIDIR</sub> (4)		7.3		9.2		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 22 through 29 in this data sheet.  
 (2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.  
 (3) These parameters are specified by characterization.  
 (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.7		0.8		1.1	ns
$t_{CLUT}$		0.5		0.6		0.8	ns
$t_{RLUT}$		0.6		0.7		1.0	ns
$t_{PACKED}$		0.3		0.4		0.5	ns
$t_{EN}$		0.6		0.8		1.0	ns
$t_{CICO}$		0.1		0.1		0.2	ns
$t_{CGEN}$		0.4		0.5		0.7	ns
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.8		1.0	ns
$t_C$		0.0		0.0		0.0	ns
$t_{CO}$		0.3		0.4		0.5	ns



Table 40. EP1K30 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
$t_{EABWP}$	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
$t_{EABDD}$		5.7		6.7		7.7	ns
$t_{EABDATAO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
$t_{EABWAH}$	0.5		0.5		0.4		ns
$t_{EABWO}$		5.1		6.0		6.8	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATA CO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

Table 51. EP1K100 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.7		1.0		1.5	ns
$t_{CLUT}$		0.5		0.7		0.9	ns
$t_{RLUT}$		0.6		0.8		1.1	ns
$t_{PACKED}$		0.3		0.4		0.5	ns
$t_{EN}$		0.2		0.3		0.3	ns
$t_{CICO}$		0.1		0.1		0.2	ns
$t_{CGEN}$		0.4		0.5		0.7	ns
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.9		1.2	ns
$t_C$		0.8		1.0		1.4	ns
$t_{CO}$		0.6		0.8		1.1	ns
$t_{COMB}$		0.4		0.5		0.7	ns
$t_{SU}$	0.4		0.6		0.7		ns
$t_H$	0.5		0.7		0.9		ns
$t_{PRE}$		0.8		1.0		1.4	ns
$t_{CLR}$		0.8		1.0		1.4	ns
$t_{CH}$	1.5		2.0		2.5		ns
$t_{CL}$	1.5		2.0		2.5		ns

## Revision History

The information contained in the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4 supersedes information published in previous versions.

The following changes were made to the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4: added extended temperature support.



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
[www.altera.com](http://www.altera.com)  
**Applications Hotline:**  
(800) 800-EPLD  
**Literature Services:**  
[lit\\_req@altera.com](mailto:lit_req@altera.com)

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