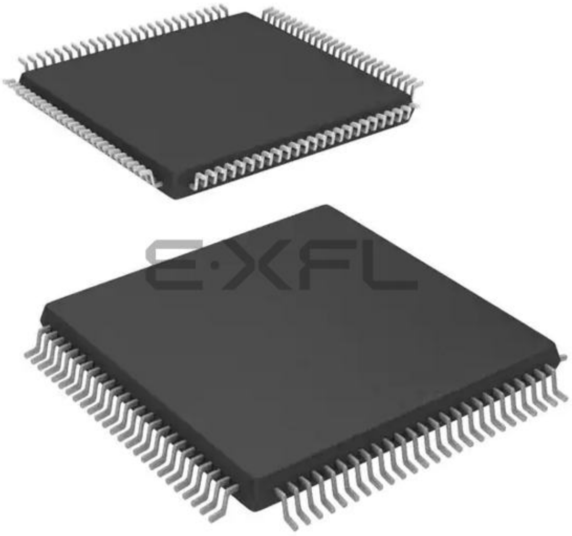
# Intel - EP1K10TC100-2 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

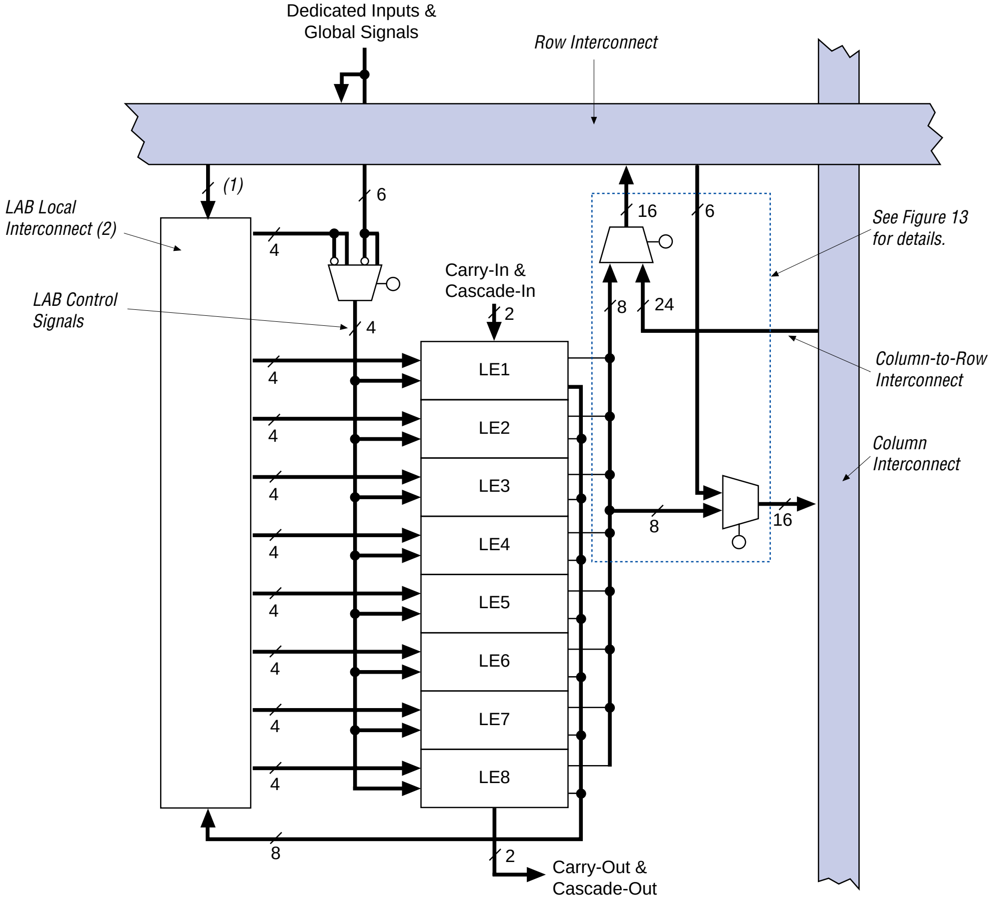
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 72 |
| Number of Logic Elements/Cells | 576 |
| Total RAM Bits | 12288 |
| Number of I/O | 66 |
| Number of Gates | 56000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1k10tc100-2 |

*Figure 7. ACEX 1K LAB*



***Notes:***

(1) EP1K10, EP1K30, and EP1K50 devices have 22 inputs to the LAB local interconnect channel from the row; EP1K100 devices have 26.

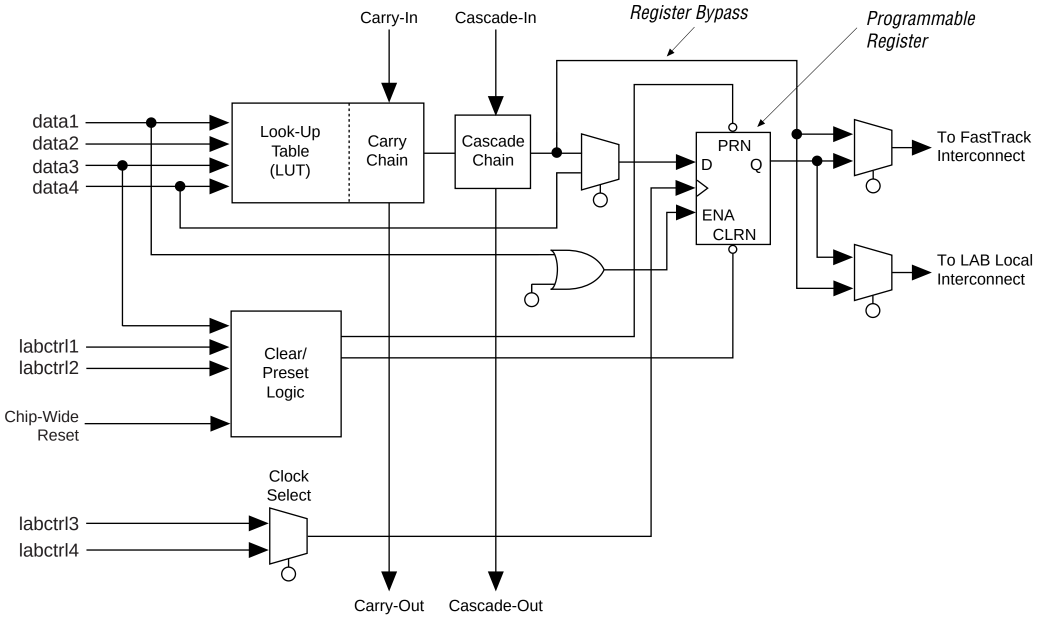
(2) EP1K10, EP1K30, and EP1K50 devices have 30 LAB local interconnect channels; EP1K100 devices have 34.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the ACEX 1K architecture, has a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure. Figure 8 shows the ACEX 1K LE.

*Figure 8. ACEX 1K Logic Element*



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the LUT's output drives the LE's output.

The LE has two outputs that drive the interconnect: one drives the local interconnect, and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The ACEX 1K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders, and the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

### *LE Operating Modes*

The ACEX 1K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 11 shows the ACEX 1K LE operating modes.

## FastTrack Interconnect Routing Structure

In the ACEX 1K architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

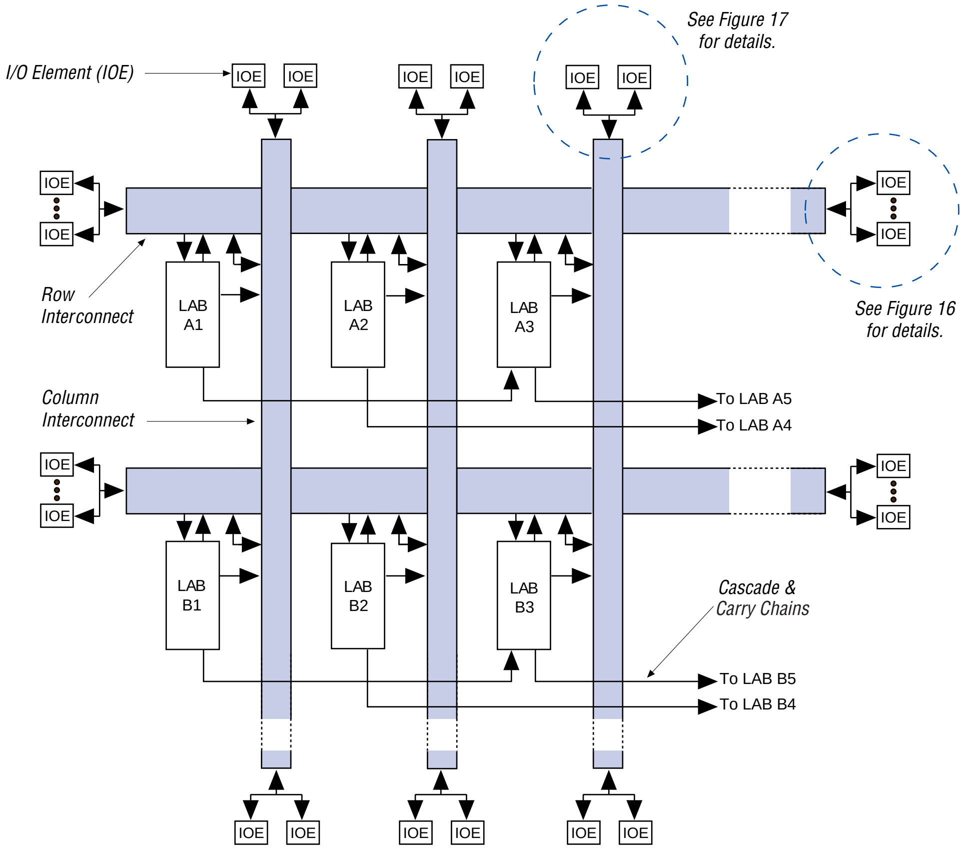
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row’s interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently. Figure 13 shows the ACEX 1K LAB.

*Figure 14. ACEX 1K Interconnect Resources*



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. For bidirectional registered I/O implementation, the output register should be in the IOE and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. Figure 15 shows the bidirectional I/O registers.

On all ACEX 1K devices, the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock-enable or eight output-enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock, and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on an LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All ACEX 1K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. ACEX 1K devices can also be configured using the JTAG pins through the ByteBlasterMV or BitBlaster download cable, or via hardware that uses the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. ACEX 1K devices support the JTAG instructions shown in Table 14.

*Table 14. ACEX 1K JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the `TDI` and `TDO` pins, allowing the BST data to pass synchronously through a selected device to adjacent devices during normal operation. |
| USERCODE | Selects the user electronic signature (USERCODE) register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`. |
| IDCODE | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| ICR Instructions | These instructions are used when configuring an ACEX 1K device via JTAG ports using a MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor. |

The instruction register length of ACEX 1K devices is 10 bits. The USERCODE register length in ACEX 1K devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. Tables 15 and 16 show the boundary-scan register length and device IDCODE information for ACEX 1K devices.

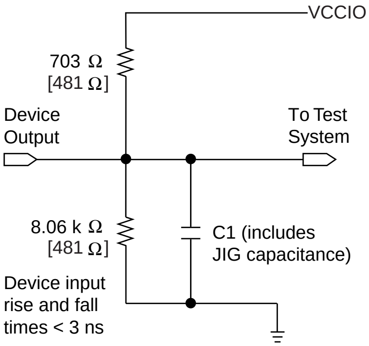
*Table 15. ACEX 1K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP1K10 | 438 |
| EP1K30 | 690 |
| EP1K50 | 798 |
| EP1K100 | 1,050 |

## Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. ACEX 1K AC Test Conditions***



*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.*

## Operating Conditions

Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

***Table 18. ACEX 1K Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, and BGA packages, under bias | | 135 | ° C |

***Table 19. ACEX 1K Device Recommended Operating Conditions***

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(2)*, *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | Commercial range | 0 | 70 | ° C |
| | | Industrial range | –40 | 85 | ° C |
| $T_J$ | Junction temperature | Commercial range | 0 | 85 | ° C |
| | | Industrial range | –40 | 100 | ° C |
| | | Extended range | –40 | 125 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

***Table 20. ACEX 1K Device DC Operating Conditions (Part 1 of 2)*** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, $0.5 \times V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, $0.3 \times V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V *(9)* | $V_{CCIO} - 0.2$ | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V *(9)* | 0.9 ×†$V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.375$ V *(9)* | 2.1 | | | V |
| | | $I_{OH} = -1$ mA DC, $V_{CCIO} = 2.375$ V *(9)* | 2.0 | | | V |
| | | $I_{OH} = -2$ mA DC, $V_{CCIO} = 2.375$ V *(9)* | 1.7 | | | V |

Figure 22 shows the required relationship between $V_{CCIO}$ and $V_{CCINT}$ to satisfy 3.3-V PCI compliance.

*Figure 22. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

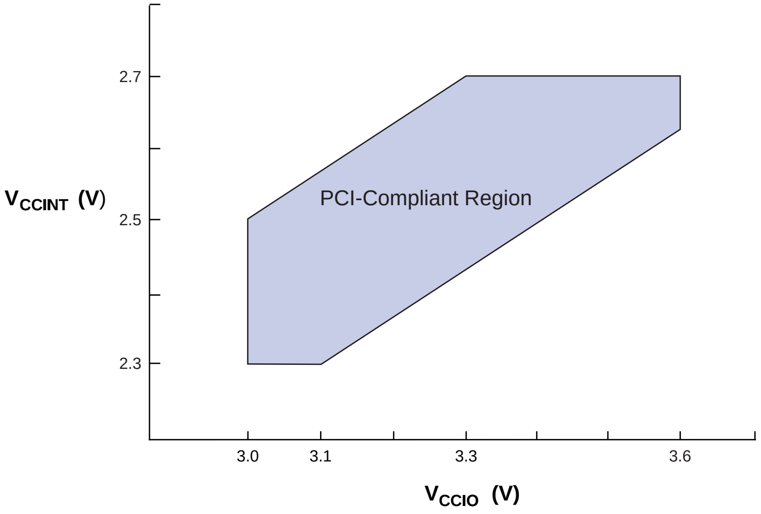
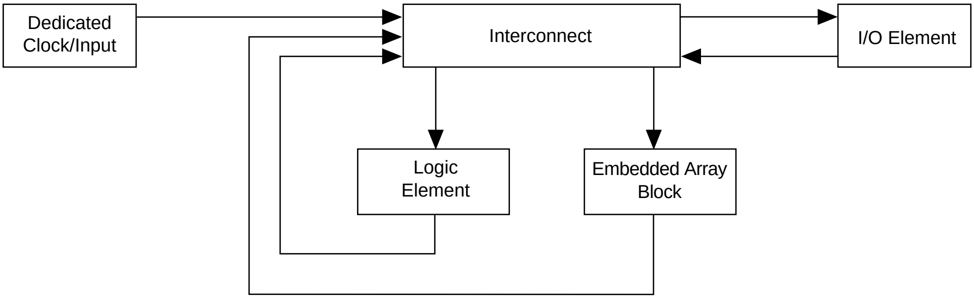


Figure 23 shows the typical output drive characteristics of ACEX 1K devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compliant to the 3.3-V ***PCI Local Bus Specification***, ***Revision 2.2*** (when `VCCIO` pins are connected to 3.3 V). ACEX 1K devices with a -1 speed grade also comply with the drive strength requirements of the ***PCI Local Bus Specification***, ***Revision 2.2*** (when `VCCINT` pins are powered with a minimum supply of 2.375 V, and `VCCIO` pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the ACEX 1K device.

**Figure 24. ACEX 1K Device Timing Model**



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

**Figure 25. ACEX 1K Device LE Timing Model**

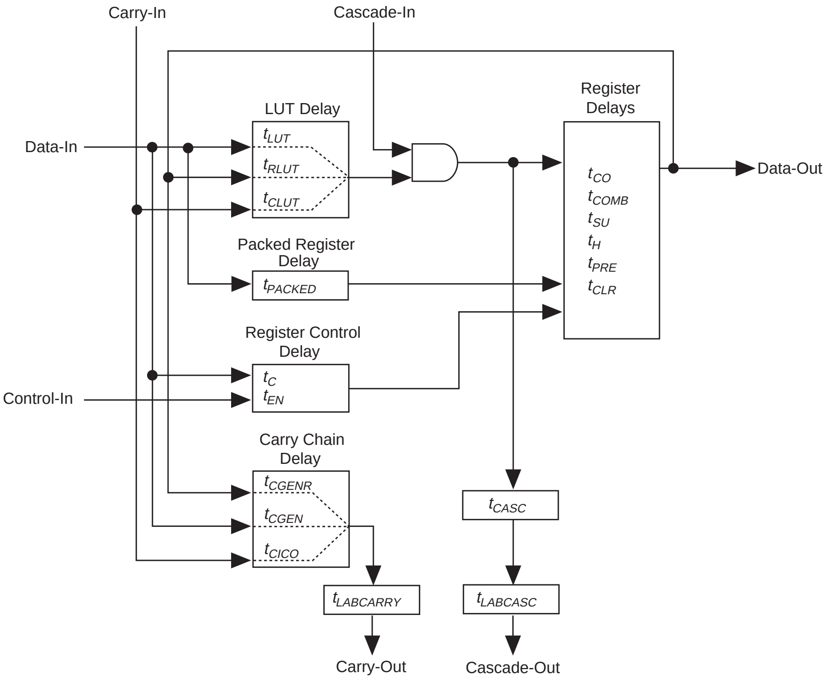


*Figure 26. ACEX 1K Device IOE Timing Model*

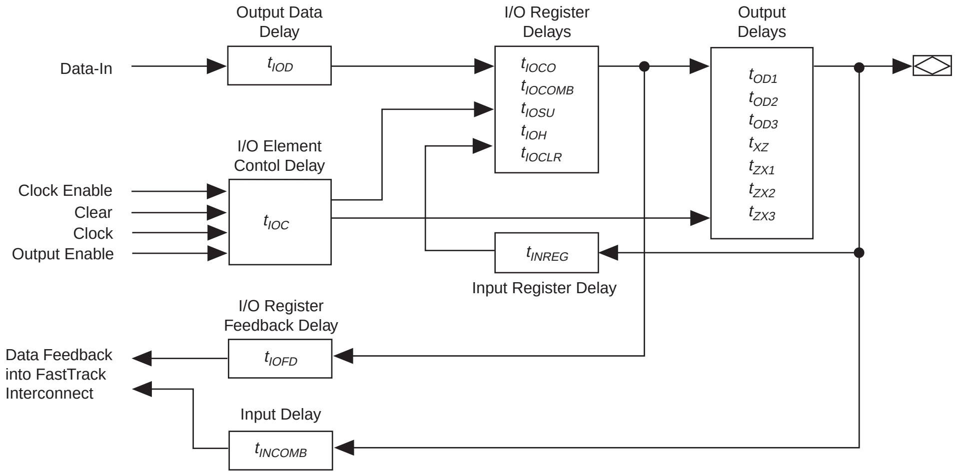


*Figure 27. ACEX 1K Device EAB Timing Model*

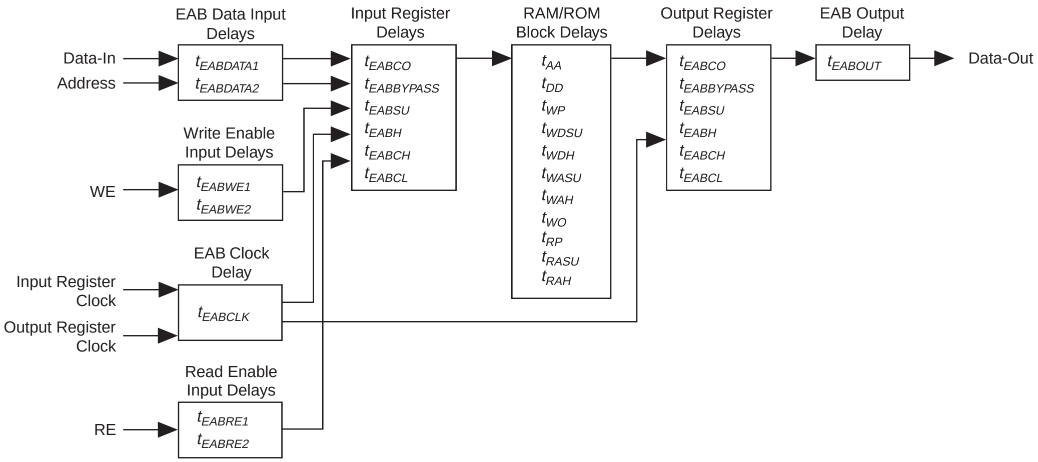
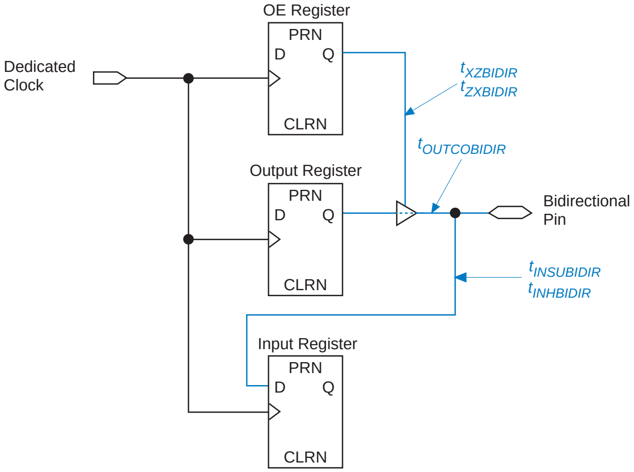


**Figure 28. Synchronous Bidirectional Pin External Timing Model**



Tables 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 24.

**Figure 29. EAB Asynchronous Timing Waveforms**

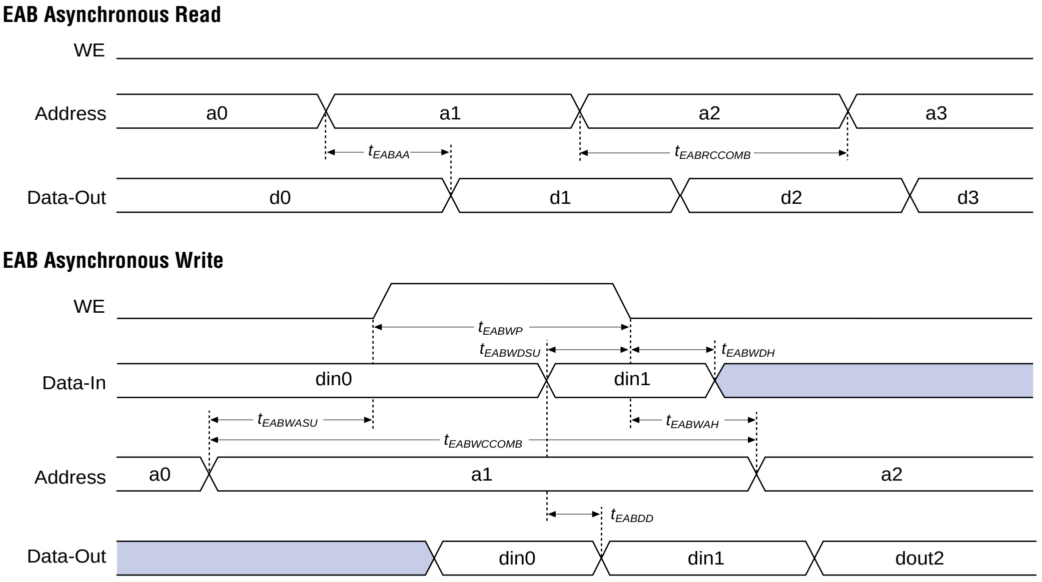


**Table 24. EAB Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{EABDATA1}$ | Data or address delay to EAB for combinatorial input | |
| $t_{EABDATA2}$ | Data or address delay to EAB for registered input | |
| $t_{EABWE1}$ | Write enable delay to EAB for combinatorial input | |
| $t_{EABWE2}$ | Write enable delay to EAB for registered input | |
| $t_{EABRE1}$ | Read enable delay to EAB for combinatorial input | |
| $t_{EABRE2}$ | Read enable delay to EAB for registered input | |
| $t_{EABCLK}$ | EAB register clock delay | |
| $t_{EABCO}$ | EAB register clock-to-output delay | |
| $t_{EABBYPASS}$ | Bypass register delay | |
| $t_{EABSU}$ | EAB register setup time before clock | |
| $t_{EABH}$ | EAB register hold time after clock | |
| $t_{EABCLR}$ | EAB register asynchronous clear time to output delay | |
| $t_{AA}$ | Address access delay (including the read enable to output delay) | |
| $t_{WP}$ | Write pulse width | |
| $t_{RP}$ | Read pulse width | |
| $t_{WDSU}$ | Data setup time before falling edge of write pulse | *(5)* |
| $t_{WDH}$ | Data hold time after falling edge of write pulse | *(5)* |
| $t_{WASU}$ | Address setup time before rising edge of write pulse | *(5)* |
| $t_{WAH}$ | Address hold time after falling edge of write pulse | *(5)* |
| $t_{RASU}$ | Address setup time before rising edge of read pulse | |
| $t_{RAH}$ | Address hold time after falling edge of read pulse | |
| $t_{WO}$ | Write enable to data output valid delay | |
| $t_{DD}$ | Data-in to data-out valid delay | |
| $t_{EABOUT}$ | Data-out delay | |
| $t_{EABCH}$ | Clock high time | |
| $t_{EABCL}$ | Clock low time | |

***Table 32. EP1K10 Device EAB Internal Microparameters*** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.8 | | 1.9 | | 1.9 | ns |
| $t_{EABDATA2}$ | | 0.6 | | 0.7 | | 0.7 | ns |
| $t_{EABWE1}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{EABRE1}$ | | 0.9 | | 0.9 | | 0.9 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.3 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{EABSU}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{EABH}$ | 0.5 | | 0.4 | | 0.4 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.3 | | ns |
| $t_{AA}$ | | 3.4 | | 3.6 | | 3.6 | ns |
| $t_{WP}$ | 2.7 | | 2.8 | | 2.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.8 | | 1.9 | | 1.9 | | ns |
| $t_{WAH}$ | 1.9 | | 2.0 | | 2.0 | | ns |
| $t_{RASU}$ | 3.1 | | 3.5 | | 3.5 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.2 | | ns |
| $t_{WO}$ | | 2.7 | | 2.8 | | 2.8 | ns |
| $t_{DD}$ | | 2.7 | | 2.8 | | 2.8 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.0 | | ns |
| $t_{EABCL}$ | 2.7 | | 2.8 | | 2.8 | | ns |

***Table 34. EP1K10 Device Interconnect Timing Microparameters*** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 2.3 | | 2.7 | | 3.6 | ns |
| $t_{DIN2LE}$ | | 0.8 | | 1.1 | | 1.4 | ns |
| $t_{DIN2DATA}$ | | 1.1 | | 1.4 | | 1.8 | ns |
| $t_{DCLK2IOE}$ | | 2.3 | | 2.7 | | 3.6 | ns |
| $t_{DCLK2LE}$ | | 0.8 | | 1.1 | | 1.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{SAMECOLUMN}$ | | 0.3 | | 0.4 | | 0.7 | ns |
| $t_{DIFFROW}$ | | 2.1 | | 2.5 | | 3.6 | ns |
| $t_{TWOROWS}$ | | 3.9 | | 4.6 | | 6.5 | ns |
| $t_{LEPERIPH}$ | | 3.3 | | 3.7 | | 4.8 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.9 | | 1.0 | | 1.4 | ns |

***Table 35. EP1K10 External Timing Parameters*** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 7.5 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2), (3)* | 2.4 | | 2.7 | | 3.6 | | ns |
| $t_{INH}$ *(2), (3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2), (3)* | 2.0 | 6.6 | 2.0 | 7.8 | 2.0 | 9.6 | ns |
| $t_{INSU}$ *(4), (3)* | 1.4 | | 1.7 | | – | | ns |
| $t_{INH}$ *(4), (3)* | 0.5 | 5.1 | 0.5 | 6.4 | – | – | ns |
| $t_{OUTCO}$ *(4), (3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{PCISU}$ *(3)* | 3.0 | | 4.2 | | 6.4 | | ns |
| $t_{PCIH}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ *(3)* | 2.0 | 6.0 | 2.0 | 7.5 | 2.0 | 10.2 | ns |

*Table 40. EP1K30 Device EAB Internal Timing Macroparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 6.4 | | 7.6 | | 8.8 | ns |
| $t_{EABRCOMB}$ | 6.4 | | 7.6 | | 8.8 | | ns |
| $t_{EABRCREG}$ | 4.4 | | 5.1 | | 6.0 | | ns |
| $t_{EABWP}$ | 2.5 | | 2.9 | | 3.3 | | ns |
| $t_{EABWCOMB}$ | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{EABWCREG}$ | 6.8 | | 7.8 | | 9.0 | | ns |
| $t_{EABDD}$ | | 5.7 | | 6.7 | | 7.7 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{EABDATASU}$ | 1.5 | | 1.7 | | 2.0 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.3 | | 1.4 | | 1.7 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.5 | | 1.7 | | 2.0 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.0 | | 3.6 | | 4.3 | | ns |
| $t_{EABWAH}$ | 0.5 | | 0.5 | | 0.4 | | ns |
| $t_{EABWO}$ | | 5.1 | | 6.0 | | 6.8 | ns |

**Table 50. EP1K50 External Bidirectional Timing Parameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (2) | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ (2) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (3) | 3.7 | | 4.2 | | – | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (2) | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ (2) | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ (2) | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ (3) | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ (3) | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ (3) | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 22 through 29.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow ACEX 1K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, re-initializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 40 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an ACEX 1K device can be loaded with one of five configuration schemes (see Table 59), chosen on the basis of the target application. An EPC16, EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a ACEX 1K device, allowing automatic configuration on system power-up.

Multiple ACEX 1K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional APEX 20K, APEX 20KE, FLEX 10K, FLEX 10KA, FLEX 10KE, ACEX 1K, and FLEX 6000 devices can be configured in the same serial chain.

*Table 59. Data Sources for ACEX 1K Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC16, EPC2, EPC1, or EPC1441 configuration device |
| Passive serial (PS) | BitBlaster or ByteBlasterMV download cables, or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL File or JBC File |

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Documentation Library*** for pin-out information.