



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	24576
Number of I/O	171
Number of Gates	119000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k30fc256-1n

...and More Features

- -1 speed grade devices are compliant with **PCI Local Bus Specification, Revision 2.2** for 5.0-V operation
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming additional device logic.
- Operate with a 2.5-V internal supply voltage
- In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay, clock skew, and clock multiplication
- Built-in, low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration
- Flexible interconnect
 - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Tri-state emulation that implements internal tri-state buses
 - Up to six global clock signals and four global clear signals
- Powerful I/O pins
 - Individual tri-state output enable control for each pin
 - Open-drain option on each I/O pin
 - Programmable output slew-rate control to reduce switching noise
 - Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
 - Supports hot-socketing

General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 4. ACEX 1K Device Performance

Application	Resources Used		Performance			
	LEs	EABs	Speed Grade			Units
			-1	-2	-3	
16-bit loadable counter	16	0	285	232	185	MHz
16-bit accumulator	16	0	285	232	185	MHz
16-to-1 multiplexer (1)	10	0	3.5	4.5	6.6	ns
16-bit multiplier with 3-stage pipeline (2)	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed (2)	0	1	278	196	143	MHz
256 × 16 RAM write cycle speed (2)	0	1	185	143	111	MHz

Notes:

- (1) This application uses combinatorial inputs and outputs.
- (2) This application uses registered inputs and outputs.

Embedded Array Block

The EAB is a flexible block of RAM, with registers on the input and output ports, that is used to implement common gate array megafunctions. Because it is large and flexible, the EAB is suitable for functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

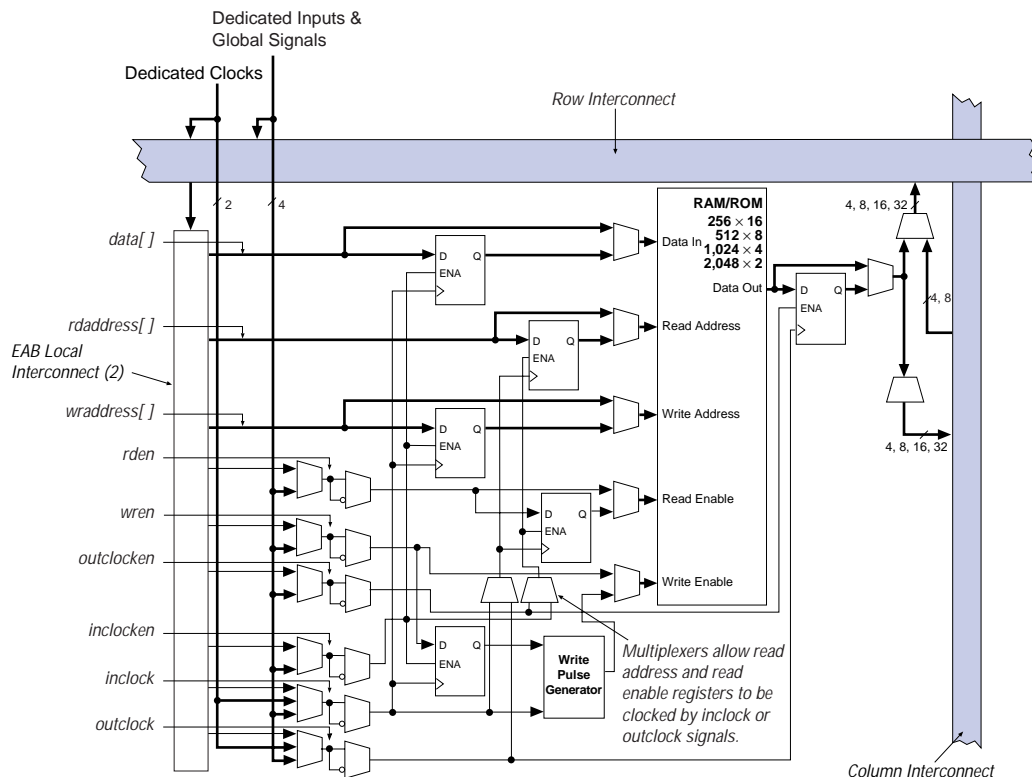
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in a single logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement any function with 8 inputs and 16 outputs. Parameterized functions, such as LPM functions, can take advantage of the EAB automatically.

The ACEX 1K enhanced EAB supports dual-port RAM. The dual-port structure is ideal for FIFO buffers with one or two clocks. The ACEX 1K EAB can also support up to 16-bit-wide RAM blocks. The ACEX 1K EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, allowing the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allow independent control of these sections.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous reads or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see [Figure 2](#)).

Figure 2. ACEX 1K Device in Dual-Port RAM Mode *Note (1)*

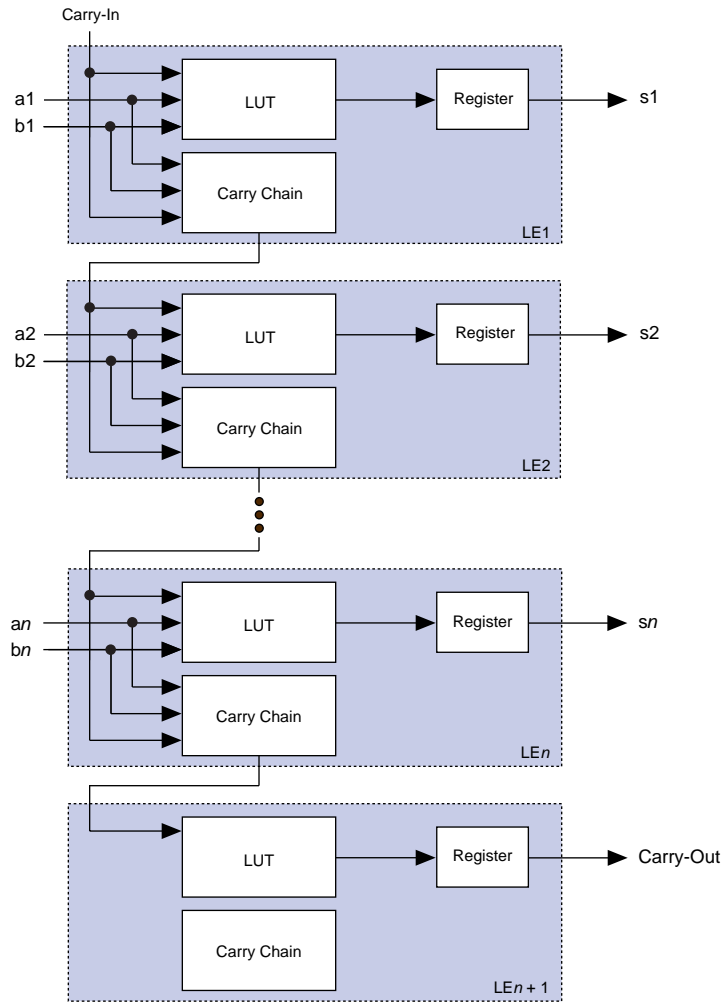


Notes:

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 11](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 6 summarizes the FastTrack Interconnect routing structure resources available in each ACEX 1K device.

<i>Table 6. ACEX 1K FastTrack Interconnect Resources</i>				
Device	Rows	Channels per Row	Columns	Channels per Column
EP1K10	3	144	24	24
EP1K30	6	216	36	24
EP1K50	10	216	36	24
EP1K100	12	312	52	24

In addition to general-purpose I/O pins, ACEX 1K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output-enable and clock-enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

On all ACEX 1K devices, the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock-enable or eight output-enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock, and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on an LAB-by-LAB basis.

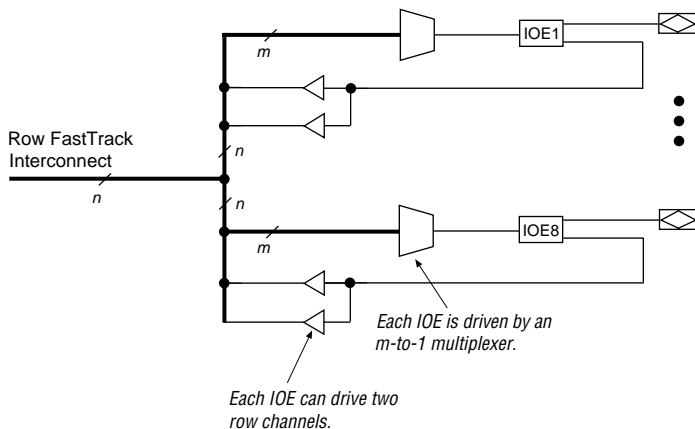
The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. ACEX 1K Row-to-IOE Connections *Note (1)*



Note:

- (1) The values for m and n are shown in Table 8.

Table 8 lists the ACEX 1K row-to-IOE interconnect resources.

Table 8. ACEX 1K Row-to-IOE Interconnect Resources		
Device	Channels per Row (n)	Row Channels per Pin (m)
EP1K10	144	18
EP1K30	216	27
EP1K50	216	27
EP1K100	312	39

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 11. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the Altera software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250 (4)	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Table 12. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		80	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		40	MHz
f_{CLKDEV}	Input deviation from user specification in the software (1)				25,000	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250 (4)	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes to tables:

- (1) To implement the ClockLock and ClockBoost circuitry with the Altera software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.
- (4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

I/O Configuration

This section discusses the PCI pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for ACEX 1K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT} . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All ACEX 1K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. ACEX 1K devices can also be configured using the JTAG pins through the ByteBlasterMV or BitBlaster download cable, or via hardware that uses the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. ACEX 1K devices support the JTAG instructions shown in [Table 14](#).

Table 14. ACEX 1K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, allowing the BST data to pass synchronously through a selected device to adjacent devices during normal operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring an ACEX 1K device via JTAG ports using a MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor.

The instruction register length of ACEX 1K devices is 10 bits. The USERCODE register length in ACEX 1K devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. [Tables 15](#) and [16](#) show the boundary-scan register length and device IDCODE information for ACEX 1K devices.

Table 15. ACEX 1K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1K10	438
EP1K30	690
EP1K50	798
EP1K100	1,050

Table 16. 32-Bit IDCODE for ACEX 1K Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) <i>(2)</i>
EP1K10	0001	0001 0000 0001 0000	000011011110	1
EP1K30	0001	0001 0000 0011 0000	000011011110	1
EP1K50	0001	0001 0000 0101 0000	000011011110	1
EP1K100	0010	0000 0001 0000 0000	000011011110	1

Notes to tables:

- (1) The most significant bit (MSB) is on the left.
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

ACEX 1K devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 20 shows the timing requirements for the JTAG signals.

Table 24. EAB Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABRE1}	Read enable delay to EAB for combinatorial input	
t_{EABRE2}	Read enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCLR}	EAB register asynchronous clear time to output delay	
t_{AA}	Address access delay (including the read enable to output delay)	
t_{WP}	Write pulse width	
t_{RP}	Read pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	(5)
t_{WDH}	Data hold time after falling edge of write pulse	(5)
t_{WASU}	Address setup time before rising edge of write pulse	(5)
t_{WAH}	Address hold time after falling edge of write pulse	(5)
t_{RASU}	Address setup time before rising edge of read pulse	
t_{RAH}	Address hold time after falling edge of read pulse	
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	

Table 25. EAB Timing Macroparameters *Notes (1), (6)*

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB \overline{WE} setup time before clock when using input register	
t_{EABWEH}	EAB \overline{WE} hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 39. EP1K30 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
t_{EABWE1}		1.1		1.3		1.4	ns
t_{EABWE2}		0.4		0.4		0.5	ns
t_{EABRE1}		0.8		0.9		1.0	ns
t_{EABRE2}		0.4		0.4		0.5	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.4	ns
$t_{EABYPASS}$		0.5		0.6		0.7	ns
t_{EABSU}	0.9		1.0		1.2		ns
t_{EABH}	0.4		0.4		0.5		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.2		3.8		4.4	ns
t_{WP}	2.5		2.9		3.3		ns
t_{RP}	0.9		1.1		1.2		ns
t_{WDSU}	0.9		1.0		1.1		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.7		2.0		2.3		ns
t_{WAH}	1.8		2.1		2.4		ns
t_{RASU}	3.1		3.7		4.2		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.5		2.9		3.3	ns
t_{DD}		2.5		2.9		3.3	ns
t_{EABOUT}		0.5		0.6		0.7	ns
t_{EABCH}	1.5		2.0		2.3		ns
t_{EABCL}	2.5		2.9		3.3		ns

Table 41. EP1K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 42. EP1K30 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t _{DDR}		8.0		9.5		12.5	ns
t _{INSU} (3)	2.1		2.5		3.9		ns
t _{INH} (3)	0.0		0.0		0.0		ns
t _{OUTCO} (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t _{INSU} (4)	1.1		1.5		–		ns
t _{INH} (4)	0.0		0.0		–		ns
t _{OUTCO} (4)	0.5	3.9	0.5	4.9	–	–	ns
t _{PCISU}	3.0		4.2		–		ns
t _{PCIH}	0.0		0.0		–		ns
t _{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 44. EP1K50 Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.6		0.6		0.7	ns
t_{COMB}		0.3		0.4		0.5	ns
t_{SU}	0.5		0.6		0.7		ns
t_H	0.5		0.6		0.8		ns
t_{PRE}		0.4		0.5		0.7	ns
t_{CLR}		0.8		1.0		1.2	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 45. EP1K50 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.3		1.9	ns
t_{IOC}		0.3		0.4		0.4	ns
t_{IOCO}		1.7		2.1		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.4		0.5		0.6		ns
t_{IOCLR}		0.2		0.2		0.4	ns
t_{OD1}		1.2		1.2		1.9	ns
t_{OD2}		0.7		0.8		1.7	ns
t_{OD3}		2.7		3.0		4.3	ns
t_{XZ}		4.7		5.7		7.5	ns
t_{ZX1}		4.7		5.7		7.5	ns
t_{ZX2}		4.2		5.3		7.3	ns
t_{ZX3}		6.2		7.5		9.9	ns
t_{INREG}		3.5		4.2		5.6	ns
t_{IOFD}		1.1		1.3		1.8	ns
t_{INCOMB}		1.1		1.3		1.8	ns

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow ACEX 1K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, re-initializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 40 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an ACEX 1K device can be loaded with one of five configuration schemes (see Table 59), chosen on the basis of the target application. An EPC16, EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a ACEX 1K device, allowing automatic configuration on system power-up.

Multiple ACEX 1K devices can be configured in any of the five configuration schemes by connecting the configuration enable (*nCE*) and configuration enable output (*nCEO*) pins on each device. Additional APEX 20K, APEX 20KE, FLEX 10K, FLEX 10KA, FLEX 10KE, ACEX 1K, and FLEX 6000 devices can be configured in the same serial chain.

Table 59. Data Sources for ACEX 1K Configuration	
Configuration Scheme	Data Source
Configuration device	EPC16, EPC2, EPC1, or EPC1441 configuration device
Passive serial (PS)	BitBlaster or ByteBlasterMV download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL File or JBC File

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Documentation Library* for pin-out information.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com

Copyright © 2003 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

