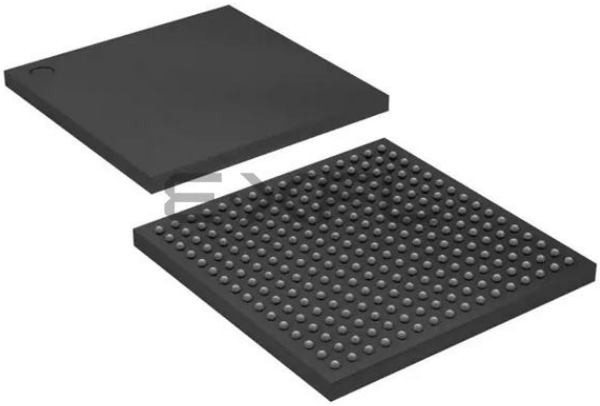

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 24576 |
| Number of I/O | 171 |
| Number of Gates | 119000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1k30fc256-3 |

## …and More Features

  - -1 speed grade devices are compliant with ***PCI Local Bus Specification, Revision 2.2*** for 5.0-V operation
  - Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming additional device logic.
  - Operate with a 2.5-V internal supply voltage
  - In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
  - ClockLock™ and ClockBoost™ options for reduced clock delay, clock skew, and clock multiplication
  - Built-in, low-skew clock distribution trees
  - 100% functional testing of all devices; test vectors or scan chains are not required
  - Pull-up on I/O pins before and during configuration
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - Clamp to $V_{CCIO}$ user-selectable on a pin-by-pin basis
  - Supports hot-socketing

## General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

*Table 4. ACEX 1K Device Performance*

| Application | Resources Used | | Performance | | | |
|---|---|---|---|---|---|---|
| | LEs | EABs | Speed Grade | | | Units |
| | | | -1 | -2 | -3 | |
| 16-bit loadable counter | 16 | 0 | 285 | 232 | 185 | MHz |
| 16-bit accumulator | 16 | 0 | 285 | 232 | 185 | MHz |
| 16-to-1 multiplexer *(1)* | 10 | 0 | 3.5 | 4.5 | 6.6 | ns |
| 16-bit multiplier with 3-stage pipeline*(2)* | 592 | 0 | 156 | 131 | 93 | MHz |
| 256 × 16 RAM read cycle speed *(2)* | 0 | 1 | 278 | 196 | 143 | MHz |
| 256 × 16 RAM write cycle speed *(2)* | 0 | 1 | 185 | 143 | 111 | MHz |

***Notes:***
(1) This application uses combinatorial inputs and outputs.
(2) This application uses registered inputs and outputs.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

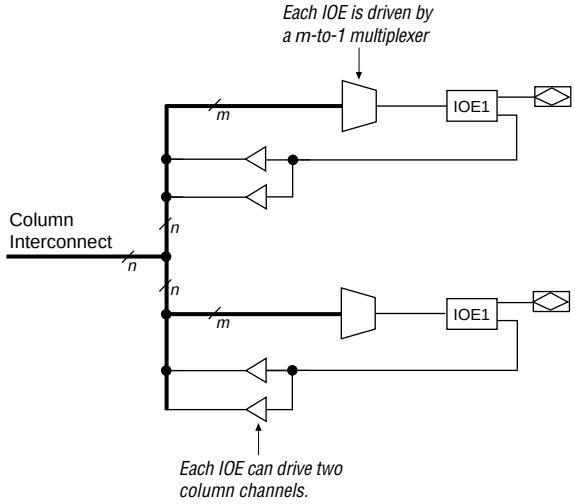
## Logic Element

The LE, the smallest unit of logic in the ACEX 1K architecture, has a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure. Figure 8 shows the ACEX 1K LE.

### Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

**Figure 17. ACEX 1K Column-to-IOE Connections** *Note (1)*




***Note:***
(1) The values for *m* and *n* are shown in Table 9.

Table 9 lists the ACEX 1K column-to-IOE interconnect resources.

**Table 9. ACEX 1K Column-to-IOE Interconnect Resources**

| Device | Channels per Column *(n)* | Column Channels per Pin *(m)* |
|---|---|---|
| EP1K10 | 24 | 16 |
| EP1K30 | 24 | 16 |
| EP1K50 | 24 | 16 |
| EP1K100 | 24 | 16 |

*Table 12. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 80 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 40 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the software *(1)* | | | | 25,000 | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB}$ < 100 | | | 250 *(4)* | ps |
| | | $t_{INCLKSTB}$ < 50 | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

***Notes to tables:***

(1) To implement the ClockLock and ClockBoost circuitry with the Altera software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation. The maximum value for $t_{JITTER}$ is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

## I/O Configuration

This section discusses the PCI pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for ACEX 1K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting $V_{CCIO}$ to a different voltage than $V_{CCINT}$. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All ACEX 1K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. ACEX 1K devices can also be configured using the JTAG pins through the ByteBlasterMV or BitBlaster download cable, or via hardware that uses the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. ACEX 1K devices support the JTAG instructions shown in Table 14.

*Table 14. ACEX 1K JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, allowing the BST data to pass synchronously through a selected device to adjacent devices during normal operation. |
| USERCODE | Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ICR Instructions | These instructions are used when configuring an ACEX 1K device via JTAG ports using a MasterBlaster, ByteBlasterMV, or BitBlaster download cable, or a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor. |

The instruction register length of ACEX 1K devices is 10 bits. The USERCODE register length in ACEX 1K devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. Tables 15 and 16 show the boundary-scan register length and device IDCODE information for ACEX 1K devices.

*Table 15. ACEX 1K Boundary-Scan Register Length*

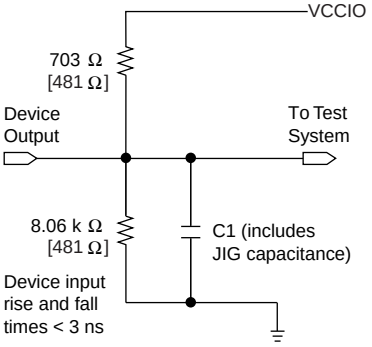
| Device | Boundary-Scan Register Length |
|---|---|
| EP1K10 | 438 |
| EP1K30 | 690 |
| EP1K50 | 798 |
| EP1K100 | 1,050 |

## Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. ACEX 1K AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.*




## Operating Conditions

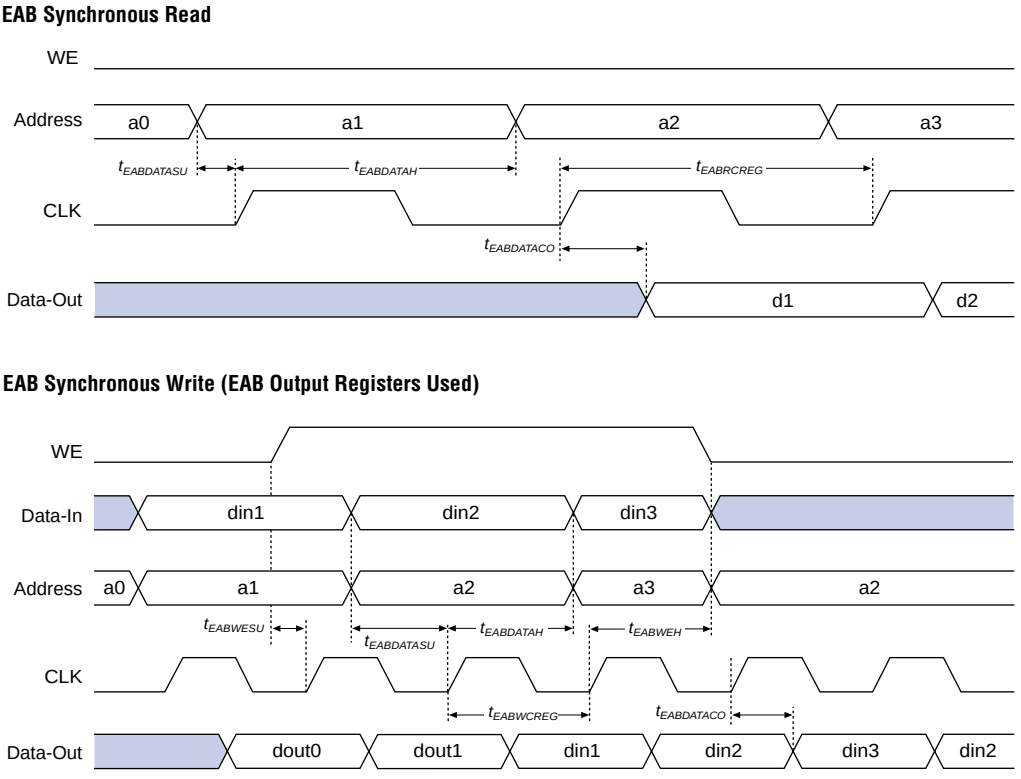
Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

***Table 18. ACEX 1K Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, and BGA packages, under bias | | 135 | ° C |

| *Table 20. ACEX 1K Device DC Operating Conditions (Part 2 of 2)* *Notes (6), (7)* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.375 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.375 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.375 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.3 to –0.3 V *(11)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.3 to –0.3 V *(11)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(13)* | 30 | | 80 | kΩ |

*Figure 30. EAB Synchronous Timing Waveforms*




Tables 22 through 26 describe the ACEX 1K device internal timing parameters.

*Table 22. LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{LUT}$ | LUT delay for data-in | |
| $t_{CLUT}$ | LUT delay for carry-in | |
| $t_{RLUT}$ | LUT delay for LE register feedback | |
| $t_{PACKED}$ | Data-in to packed register delay | |
| $t_{EN}$ | LE register enable delay | |
| $t_{CICO}$ | Carry-in to carry-out delay | |
| $t_{CGEN}$ | Data-in to carry-out delay | |
| $t_{CGENR}$ | LE register feedback to carry-out delay | |

| *Table 24. EAB Timing Microparameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{EABDATA1}$ | Data or address delay to EAB for combinatorial input | |
| $t_{EABDATA2}$ | Data or address delay to EAB for registered input | |
| $t_{EABWE1}$ | Write enable delay to EAB for combinatorial input | |
| $t_{EABWE2}$ | Write enable delay to EAB for registered input | |
| $t_{EABRE1}$ | Read enable delay to EAB for combinatorial input | |
| $t_{EABRE2}$ | Read enable delay to EAB for registered input | |
| $t_{EABCLK}$ | EAB register clock delay | |
| $t_{EABCO}$ | EAB register clock-to-output delay | |
| $t_{EABBYPASS}$ | Bypass register delay | |
| $t_{EABSU}$ | EAB register setup time before clock | |
| $t_{EABH}$ | EAB register hold time after clock | |
| $t_{EABCLR}$ | EAB register asynchronous clear time to output delay | |
| $t_{AA}$ | Address access delay (including the read enable to output delay) | |
| $t_{WP}$ | Write pulse width | |
| $t_{RP}$ | Read pulse width | |
| $t_{WDSU}$ | Data setup time before falling edge of write pulse | *(5)* |
| $t_{WDH}$ | Data hold time after falling edge of write pulse | *(5)* |
| $t_{WASU}$ | Address setup time before rising edge of write pulse | *(5)* |
| $t_{WAH}$ | Address hold time after falling edge of write pulse | *(5)* |
| $t_{RASU}$ | Address setup time before rising edge of read pulse | |
| $t_{RAH}$ | Address hold time after falling edge of read pulse | |
| $t_{WO}$ | Write enable to data output valid delay | |
| $t_{DD}$ | Data-in to data-out valid delay | |
| $t_{EABOUT}$ | Data-out delay | |
| $t_{EABCH}$ | Clock high time | |
| $t_{EABCL}$ | Clock low time | |

**Table 26. Interconnect Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{DIN2IOE}$ | Delay from dedicated input pin to IOE control input | *(7)* |
| $t_{DIN2LE}$ | Delay from dedicated input pin to LE or EAB control input | *(7)* |
| $t_{DIN2DATA}$ | Delay from dedicated input or clock to LE or EAB data | *(7)* |
| $t_{DCLK2IOE}$ | Delay from dedicated clock pin to IOE clock | *(7)* |
| $t_{DCLK2LE}$ | Delay from dedicated clock pin to LE or EAB clock | *(7)* |
| $t_{SAMELAB}$ | Routing delay for an LE driving another LE in the same LAB | *(7)* |
| $t_{SAMEROW}$ | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row | *(7)* |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column | *(7)* |
| $t_{DIFFROW}$ | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{TWOROWS}$ | Routing delay for a row IOE or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{LEPERIPH}$ | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus | *(7)* |
| $t_{LABCARRY}$ | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB | |
| $t_{LABCASC}$ | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB | |

***Notes to tables:***

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial or industrial and extended use in ACEX 1K devices
(3) Operating conditions: $V_{CCIO}$ = 2.5 V ± 5% for commercial or industrial and extended use in ACEX 1K devices.
(4) Operating conditions: $V_{CCIO}$ = 2.5 V or 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

| *Table 33. EP1K10 Device EAB Internal Timing Macroparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABAA}$ | | 6.7 | | 7.3 | | 7.3 | ns |
| $t_{EABRCCOMB}$ | 6.7 | | 7.3 | | 7.3 | | ns |
| $t_{EABRCREG}$ | 4.7 | | 4.9 | | 4.9 | | ns |
| $t_{EABWP}$ | 2.7 | | 2.8 | | 2.8 | | ns |
| $t_{EABWCCOMB}$ | 6.4 | | 6.7 | | 6.7 | | ns |
| $t_{EABWCREG}$ | 7.4 | | 7.6 | | 7.6 | | ns |
| $t_{EABDD}$ | | 6.0 | | 6.5 | | 6.5 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 0.9 | ns |
| $t_{EABDATASU}$ | 1.6 | | 1.7 | | 1.7 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.4 | | 1.4 | | 1.4 | | ns |
| $t_{EABWEH}$ | 0.1 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.6 | | 1.7 | | 1.7 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.1 | | 3.4 | | 3.4 | | ns |
| $t_{EABWAH}$ | 0.6 | | 0.5 | | 0.5 | | ns |
| $t_{EABWO}$ | | 5.4 | | 5.8 | | 5.8 | ns |

*Table 36. EP1K10 External Bidirectional Timing Parameters* *Notes (1), (3)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (2) | 2.2 | | 2.3 | | 3.2 | | ns |
| $t_{INHBIDIR}$ (2) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ (2) | 2.0 | 6.6 | 2.0 | 7.8 | 2.0 | 9.6 | ns |
| $t_{XZBIDIR}$ (2) | | 8.8 | | 11.2 | | 14.0 | ns |
| $t_{ZXBIDIR}$ (2) | | 8.8 | | 11.2 | | 14.0 | ns |
| $t_{INSUBIDIR}$ (4) | 3.1 | | 3.3 | | – | – | |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 5.1 | 0.5 | 6.4 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 7.3 | | 9.2 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 7.3 | | 9.2 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 22 through 29 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) These parameters are specified by characterization.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

*Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{C}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |

*Table 43. EP1K30 External Bidirectional Timing Parameters* *Notes (1), (2)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (3) | 2.8 | | 3.9 | | 5.2 | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (4) | 3.8 | | 4.9 | | – | | ns |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (3) | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| $t_{XZBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{ZXBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 3.9 | 0.5 | 4.9 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 22 through 29 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 44 through 50 show EP1K50 device external timing parameters.

*Table 44. EP1K50 Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{PACKED}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{EN}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{CASC}$ | | 0.5 | | 0.8 | | 1.0 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |

| Table 44. EP1K50 Device LE Timing Microparameters (Part 2 of 2) Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | Speed Grade | | | | | | Unit |
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{CO}$ | | 0.6 | | 0.6 | | 0.7 | ns |
| $t_{COMB}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PRE}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

| Table 45. EP1K50 Device IOE Timing Microparameters Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | Speed Grade | | | | | | Unit |
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.3 | | 1.9 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{IOCO}$ | | 1.7 | | 2.1 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.4 | ns |
| $t_{OD1}$ | | 1.2 | | 1.2 | | 1.9 | ns |
| $t_{OD2}$ | | 0.7 | | 0.8 | | 1.7 | ns |
| $t_{OD3}$ | | 2.7 | | 3.0 | | 4.3 | ns |
| $t_{XZ}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX1}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX2}$ | | 4.2 | | 5.3 | | 7.3 | ns |
| $t_{ZX3}$ | | 6.2 | | 7.5 | | 9.9 | ns |
| $t_{INREG}$ | | 3.5 | | 4.2 | | 5.6 | ns |
| $t_{IOFD}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{INCOMB}$ | | 1.1 | | 1.3 | | 1.8 | ns |

*Table 46. EP1K50 Device EAB Internal Microparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA2}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.0 | | 1.4 | | 1.9 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0.0 | | 0.0 | | 0.0 | |
| $t_{EABRE2}$ | | 0.4 | | 0.6 | | 0.8 | |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABSU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABCLR}$ | 0.8 | | 1.1 | | 1.5 | | |
| $t_{AA}$ | | 2.0 | | 2.8 | | 3.8 | ns |
| $t_{WP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.4 | | 1.9 | | |
| $t_{WDSU}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.0 | | 1.4 | | 1.9 | | ns |
| $t_{WAH}$ | 1.5 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 1.5 | | 2.1 | | 2.8 | | |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | |
| $t_{WO}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{DD}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

*Table 47. EP1K50 Device EAB Internal Timing Macroparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 3.7 | | 5.2 | | 7.0 | ns |
| $t_{EABRCCOMB}$ | 3.7 | | 5.2 | | 7.0 | | ns |
| $t_{EABRCREG}$ | 3.5 | | 4.9 | | 6.6 | | ns |
| $t_{EABWP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{EABWCCOMB}$ | 4.5 | | 6.3 | | 8.6 | | ns |
| $t_{EABWCREG}$ | 5.6 | | 7.8 | | 10.6 | | ns |
| $t_{EABDD}$ | | 3.8 | | 5.3 | | 7.2 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABDATASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABWEH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABWDSU}$ | 1.2 | | 1.7 | | 2.2 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 1.6 | | 2.3 | | 3.0 | | ns |
| $t_{EABWAH}$ | 0.9 | | 1.2 | | 1.8 | | ns |
| $t_{EABWO}$ | | 3.1 | | 4.3 | | 5.9 | ns |

| *Table 52. EP1K100 Device IOE Timing Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

| *Table 53. EP1K100 Device EAB Internal Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABDATA1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABDATA1}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABWE1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABWE2}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{EABSU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{AA}$ | | 4.0 | | 5.1 | | 6.6 | ns |
| $t_{WP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{RP}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WASU}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{WAH}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{RASU}$ | 3.0 | | 3.9 | | 5.2 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{DD}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABOUT}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.7 | | 3.5 | | 4.7 | | ns |

| *Table 54. EP1K100 Device EAB Internal Timing Macroparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABAA}$ | | 5.9 | | 7.6 | | 9.9 | ns |
| $t_{EABRCOMB}$ | 5.9 | | 7.6 | | 9.9 | | ns |
| $t_{EABRCREG}$ | 5.1 | | 6.5 | | 8.5 | | ns |
| $t_{EABWP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{EABWCOMB}$ | 5.9 | | 7.7 | | 10.3 | | ns |
| $t_{EABWCREG}$ | 5.4 | | 7.0 | | 9.4 | | ns |
| $t_{EABDD}$ | | 3.4 | | 4.5 | | 5.9 | ns |
| $t_{EABDATACO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{EABDATASU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABDATAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{EABWESU}$ | 1.1 | | 1.4 | | 1.9 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{EABWDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{EABWASU}$ | 4.1 | | 5.2 | | 6.8 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 3.4 | | 4.5 | | 5.9 | ns |