Intel - **EP1K30TC144-2N Datasheet**

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	24576
Number of I/O	102
Number of Gates	119000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k30tc144-2n

Table 5 shows ACEX 1K device performance for more complex designs. These designs are available as Altera MegaCore™ functions.

Table 5. ACEX 1K Device Performance for Complex Designs

Application	LEs Used	Performance			Units
		Speed Grade			
		-1	-2	-3	
16-bit, 8-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point Fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	µs
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Each ACEX 1K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

ACEX 1K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers EPC16, EPC2, EPC1, and EPC1441 configuration devices, which configure ACEX 1K devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cables. After an ACEX 1K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 40 ms, real-time changes can be made during system operation.

ACEX 1K devices contain an interface that permits microprocessors to configure ACEX 1K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat an ACEX 1K device as memory and configure it by writing to a virtual memory location, simplifying device reconfiguration.

Figure 1. ACEX 1K Device Block Diagram
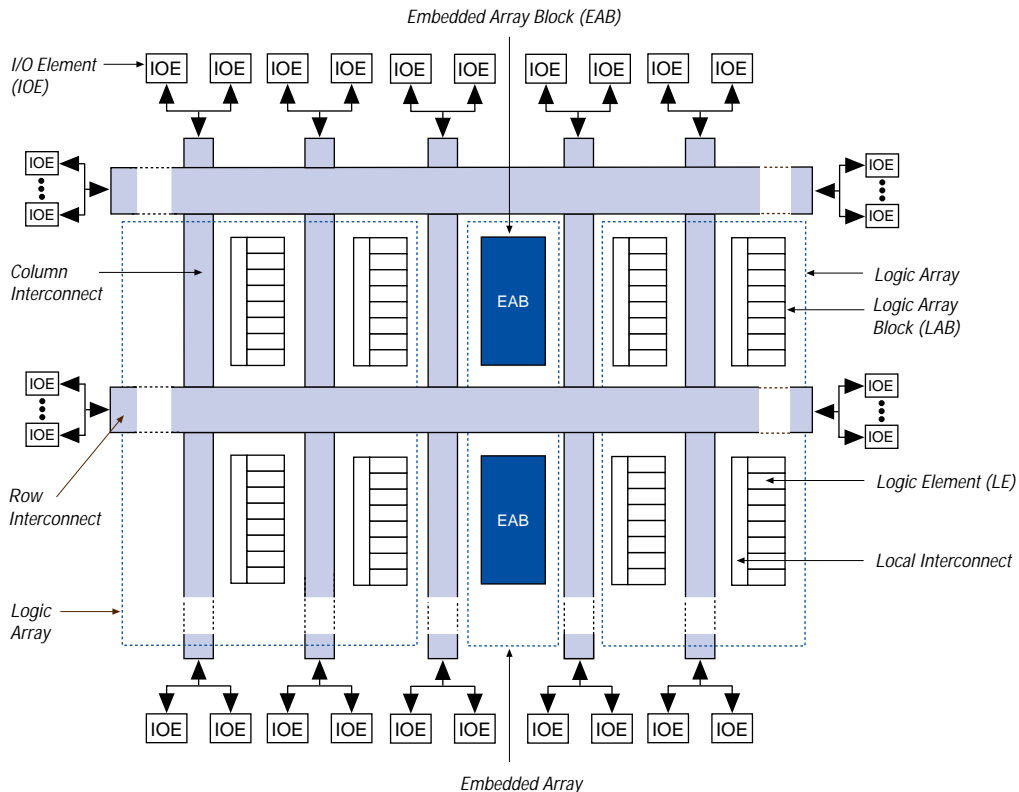
ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

*Figure 2. ACEX 1K Device in Dual-Port RAM Mode*   *Note (1)*
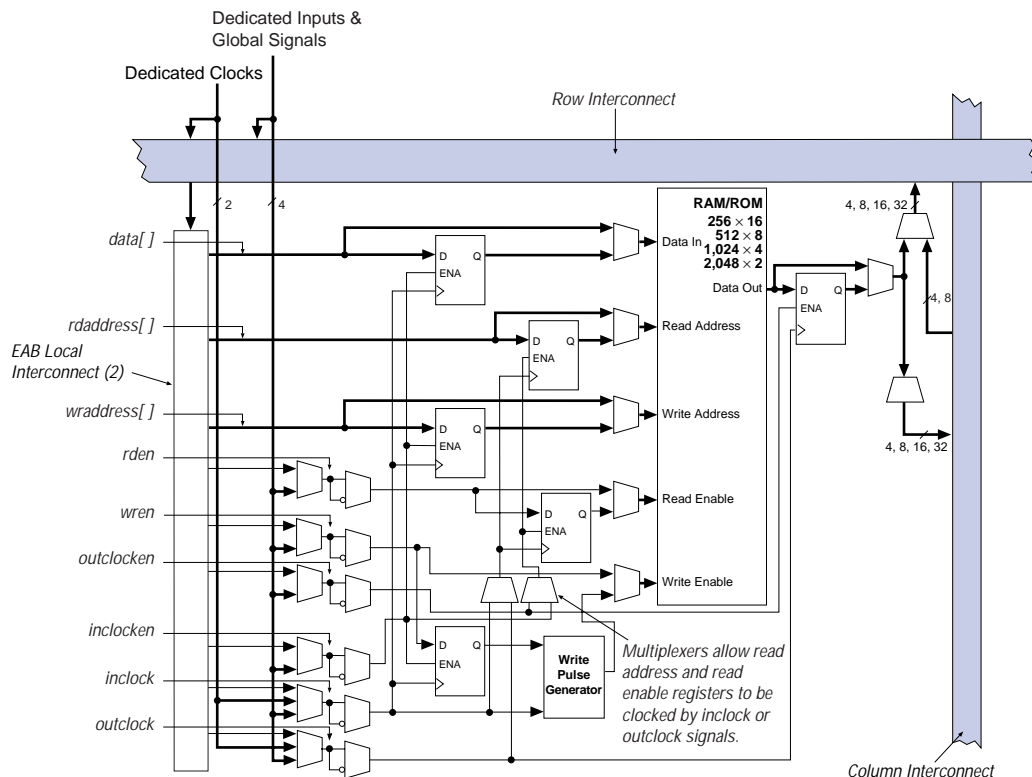
Notes:
(1)   All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
(2)   EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256×16; 512×8; $1,024 \times 4$; or $2,048 \times 2$. Figure 5 shows the ACEX 1K EAB memory configurations.

Figure 5. ACEX 1K EAB Memory Configurations
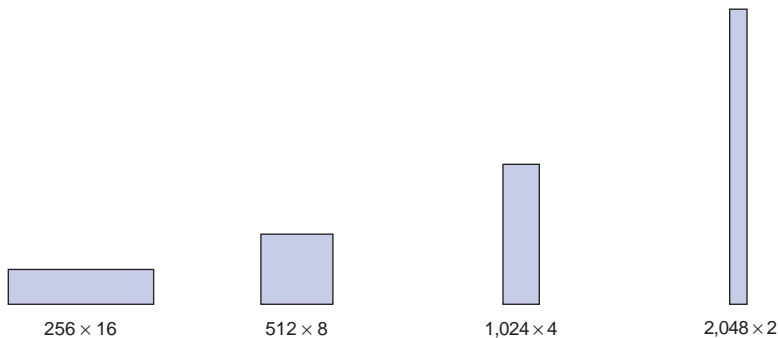
Larger blocks of RAM are created by combining multiple EABs. For example, two 256×16 RAM blocks can be combined to form a 256×32 block, and two 512×8 RAM blocks can be combined to form a 512×16 block. Figure 6 shows examples of multiple EAB combination.

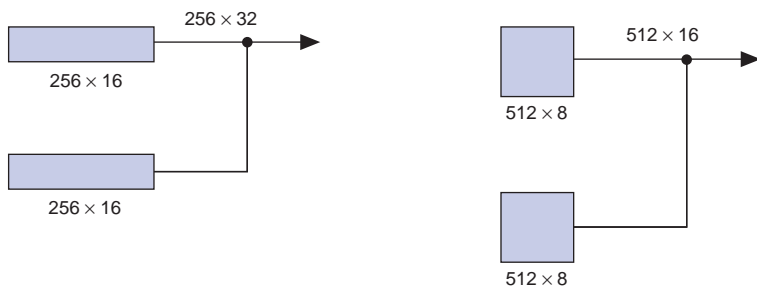*Figure 6. Examples of Combining ACEX 1K EABs*

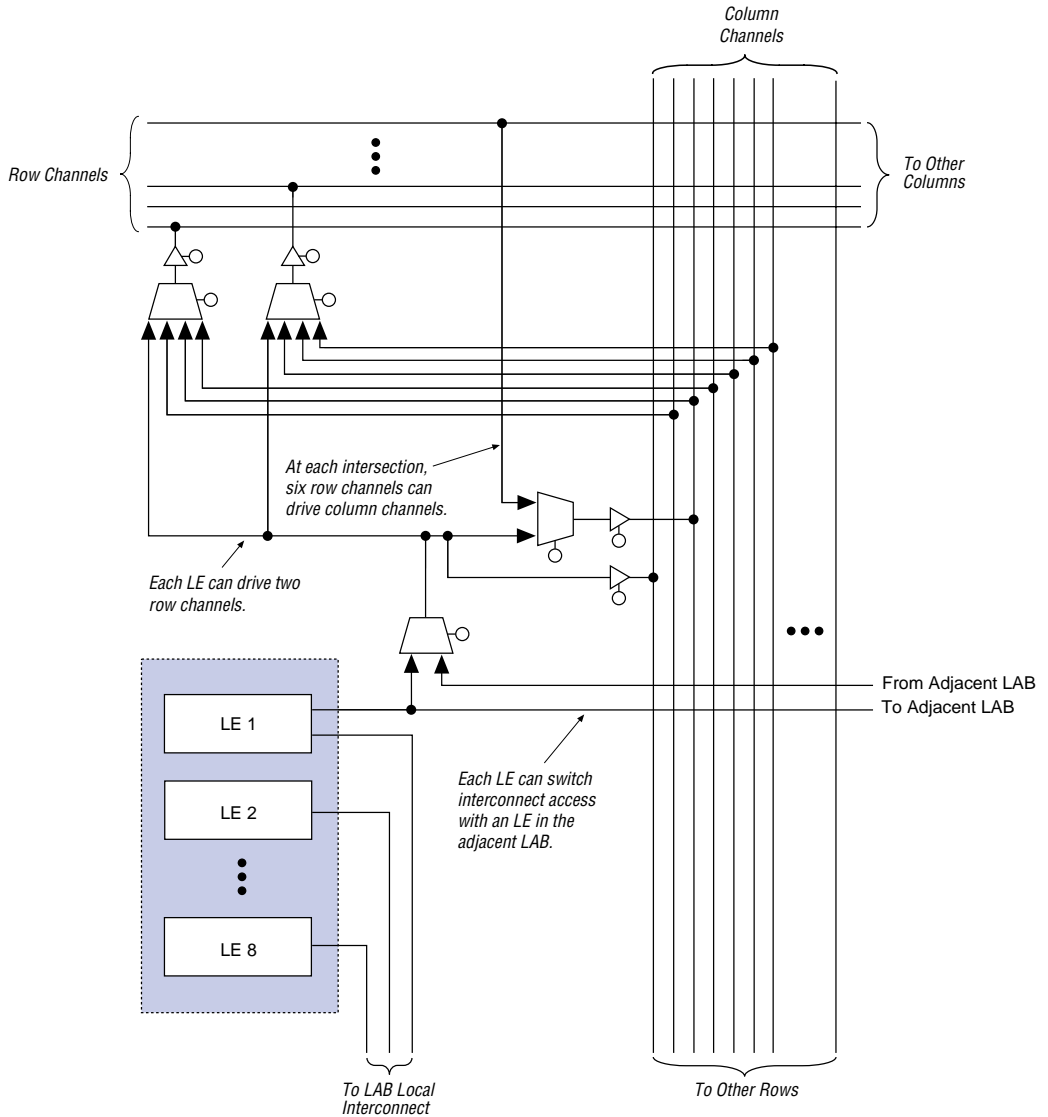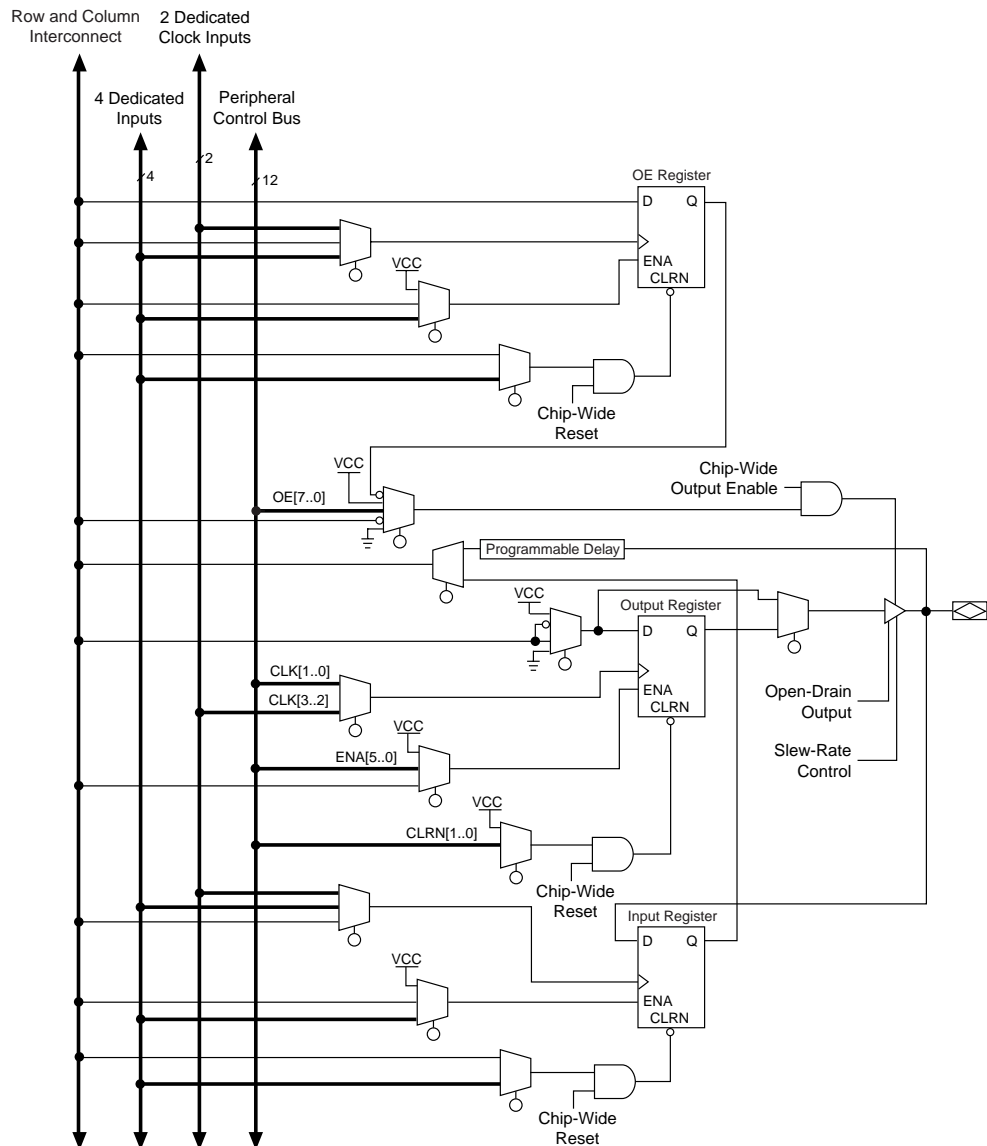*Figure 13. ACEX 1K LAB Connections to Row & Column Interconnect*

Figure 15. ACEX 1K Bidirectional I/O Registers

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

Figure 17. ACEX 1K Column-to-IOE Connections   *Note (1)*
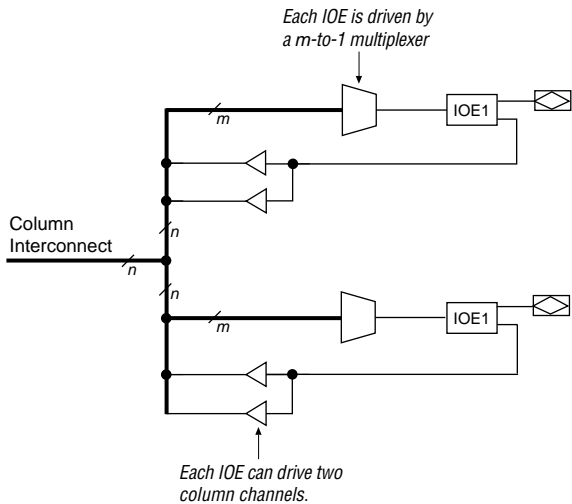
Note:
(1)   The values for *m* and *n* are shown in Table 9.

Table 9 lists the ACEX 1K column-to-IOE interconnect resources.

Table 9. ACEX 1K Column-to-IOE Interconnect Resources		
Device	Channels per Column (n)	Column Channels per Pin (m)
EP1K10	24	16
EP1K30	24	16
EP1K50	24	16
EP1K100	24	16

Table 16. 32-Bit IDCODE for ACEX 1K Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EP1K10	0001	0001 0000 0001 0000	00001101110	1
EP1K30	0001	0001 0000 0011 0000	00001101110	1
EP1K50	0001	0001 0000 0101 0000	00001101110	1
EP1K100	0010	0000 0001 0000 0000	00001101110	1

Notes to tables:
(1)   The most significant bit (MSB) is on the left.
(2)   The least significant bit (LSB) for all JTAG IDCODEs is 1.

ACEX 1K devices include weak pull-up resistors on the JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 20 shows the timing requirements for the JTAG signals.

Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. ACEX 1K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.
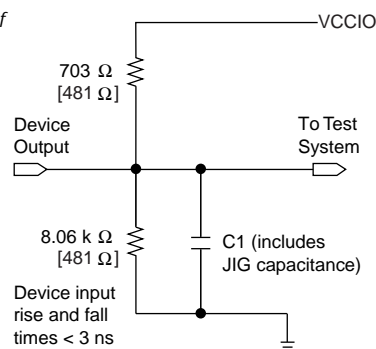
Operating Conditions

Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

Table 18. ACEX 1K Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	−0.5	3.6	V
V_{CCIO}			−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	° C

Table 19. ACEX 1K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	(2), (5)	−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range	−40	85	° C
T_J	Junction temperature	Commercial range	0	85	° C
		Industrial range	−40	100	° C
		Extended range	−40	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 20. ACEX 1K Device DC Operating Conditions (Part 1 of 2)   Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (8)		5.75	V
V_{IL}	Low-level input voltage		−0.5		0.8, $0.3 \times V_{CCIO}$ (8)	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = −8 mA DC, V_{CCIO} = 3.00 V (9)	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 3.00 V (9)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	I_{OH} = −0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V (9)	$0.9 \times†V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 2.375 V (9)	2.1			V
		I_{OH} = −1 mA DC, V_{CCIO} = 2.375 V (9)	2.0			V
		I_{OH} = −2 mA DC, V_{CCIO} = 2.375 V (9)	1.7			V

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Table 21. ACEX 1K Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial- and extended-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the ACEX 1K Recommended Operating Conditions shown in Table 19 on page 46.
(8) The ACEX 1K input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 22.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed grade commercial temperature devices and -2 speed grade industrial and extended temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
(14) Capacitance is sample-tested only.

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Figure 26. ACEX 1K Device IOE Timing Model

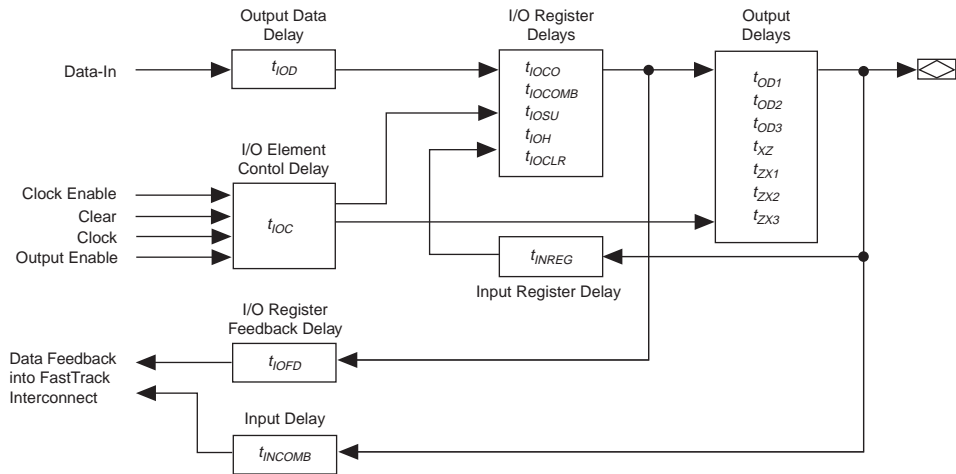*Figure 27. ACEX 1K Device EAB Timing Model*
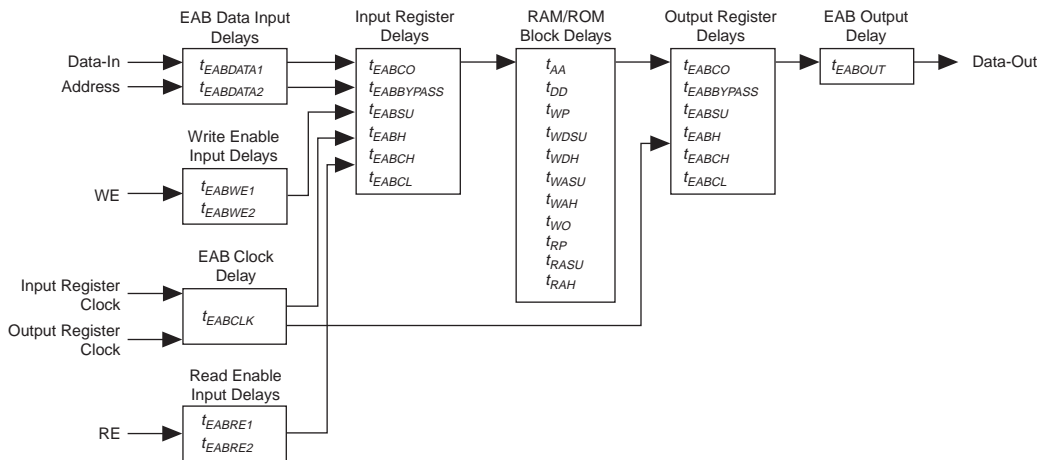
Table 22. LE Timing Microparameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Conditions
t_{CASC}	Cascade-in to cascade-out delay	
t_C	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_H	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 23. IOE Timing Microparameters   Note (1)

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 26. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	*(7)*
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial and extended use in ACEX 1K devices

(3) Operating conditions: V_{CCIO} = 2.5 V ± 5% for commercial or industrial and extended use in ACEX 1K devices.

(4) Operating conditions: V_{CCIO} = 2.5 V or 3.3 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 36. EP1K10 External Bidirectional Timing Parameters							Notes (1), (3)
Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$ (2)	2.2		2.3		3.2		ns
t$_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
t$_{OUTCOBIDIR}$ (2)	2.0	6.6	2.0	7.8	2.0	9.6	ns
t$_{XZBIDIR}$ (2)		8.8		11.2		14.0	ns
t$_{ZXBIDIR}$ (2)		8.8		11.2		14.0	ns
t$_{INSUBIDIR}$ (4)	3.1		3.3		–	–	
t$_{INHBIDIR}$ (4)	0.0		0.0		–		
t$_{OUTCOBIDIR}$ (4)	0.5	5.1	0.5	6.4	–	–	ns
t$_{XZBIDIR}$ (4)		7.3		9.2		–	ns
t$_{ZXBIDIR}$ (4)		7.3		9.2		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 22 through 29 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) These parameters are specified by characterization.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2)							Note (1)
Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t$_{LUT}$		0.7		0.8		1.1	ns
t$_{CLUT}$		0.5		0.6		0.8	ns
t$_{RLUT}$		0.6		0.7		1.0	ns
t$_{PACKED}$		0.3		0.4		0.5	ns
t$_{EN}$		0.6		0.8		1.0	ns
t$_{CICO}$		0.1		0.1		0.2	ns
t$_{CGEN}$		0.4		0.5		0.7	ns
t$_{CGENR}$		0.1		0.1		0.2	ns
t$_{CASC}$		0.6		0.8		1.0	ns
t$_{C}$		0.0		0.0		0.0	ns
t$_{CO}$		0.3		0.4		0.5	ns

Table 41. EP1K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 42. EP1K30 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(3)*	2.1		2.5		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	4.9	2.0	5.9	2.0	7.6	ns
t_{INSU} *(4)*	1.1		1.5		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.9	0.5	4.9	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 53. EP1K100 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA1}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.1		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.1		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Figure 31. ACEX 1K $I_{CCACTIVE}$ vs. Operating Frequency

EP1K30

I_{CC} Supply Current (mA)

Frequency (MHz)

EP1K50

I_{CC} Supply Current (mA)

Frequency (MHz)

EP1K100

I_{CC} Supply Current (mA)

Frequency (MHz)
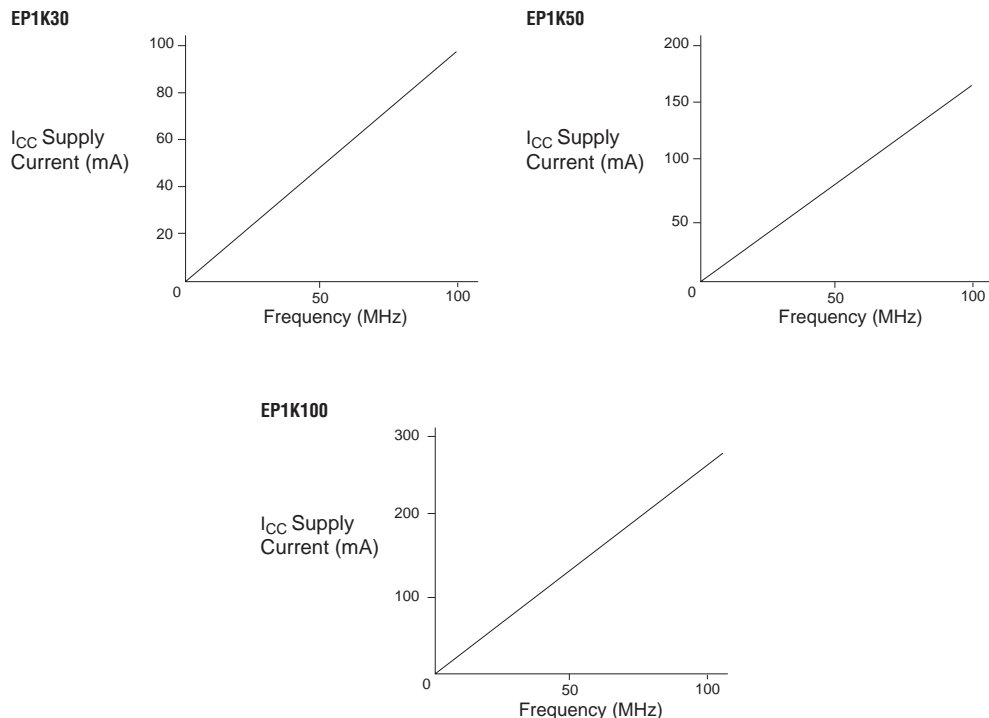
Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50 μs.

☞ When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow ACEX 1K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, re-initializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 40 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an ACEX 1K device can be loaded with one of five configuration schemes (see Table 59), chosen on the basis of the target application. An EPC16, EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a ACEX 1K device, allowing automatic configuration on system power-up.

Multiple ACEX 1K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional APEX 20K, APEX 20KE, FLEX 10K, FLEX 10KA, FLEX 10KE, ACEX 1K, and FLEX 6000 devices can be configured in the same serial chain.

Table 59. Data Sources for ACEX 1K Configuration

Configuration Scheme	Data Source
Configuration device	EPC16, EPC2, EPC1, or EPC1441 configuration device
Passive serial (PS)	BitBlaster or ByteBlasterMV download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL File or JBC File

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Documentation Library* for pin-out information.

Revision History

The information contained in the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4 supersedes information published in previous versions.

The following changes were made to the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4: added extended temperature support.