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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	24576
Number of I/O	102
Number of Gates	119000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k30ti144-2nga

…and More Features

  - -1 speed grade devices are compliant with ***PCI Local Bus Specification, Revision 2.2*** for 5.0-V operation
  - Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming additional device logic.
  - Operate with a 2.5-V internal supply voltage
  - In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
  - ClockLock™ and ClockBoost™ options for reduced clock delay, clock skew, and clock multiplication
  - Built-in, low-skew clock distribution trees
  - 100% functional testing of all devices; test vectors or scan chains are not required
  - Pull-up on I/O pins before and during configuration
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
  - Supports hot-socketing

- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Flexible package options are available in 100 to 484 pins, including the innovative FineLine BGA™ packages (see Tables 2 and 3)
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 2. ACEX 1K Package Options & I/O Pin Count *Notes (1), (2)*

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	66	92	120	136	136 *(3)*
EP1K30		102	147	171	171 *(3)*
EP1K50		102	147	186	249
EP1K100			147	186	333

Notes:

(1) ACEX 1K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and FineLine BGA packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 256-pin FineLine BGA package. By using SameFrame™ pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin and 484-pin FineLine BGA packages.

Table 3. ACEX 1K Package Sizes

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.0
Area (mm^2)	256	484	936	289	529
Length × width (mm × mm)	16 × 16	22 × 22	30.6 × 30.6	17 × 17	23 × 23

Table 5 shows ACEX 1K device performance for more complex designs. These designs are available as Altera MegaCore™ functions.

Table 5. ACEX 1K Device Performance for Complex Designs

Application	LEs Used	Performance			
		Speed Grade			Units
		-1	-2	-3	
16-bit, 8-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point Fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	µs
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Each ACEX 1K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

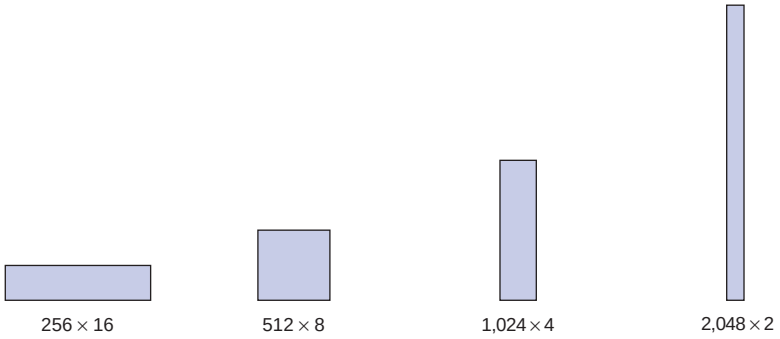
ACEX 1K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers EPC16, EPC2, EPC1, and EPC1441 configuration devices, which configure ACEX 1K devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cables. After an ACEX 1K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 40 ms, real-time changes can be made during system operation.

ACEX 1K devices contain an interface that permits microprocessors to configure ACEX 1K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat an ACEX 1K device as memory and configure it by writing to a virtual memory location, simplifying device reconfiguration.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

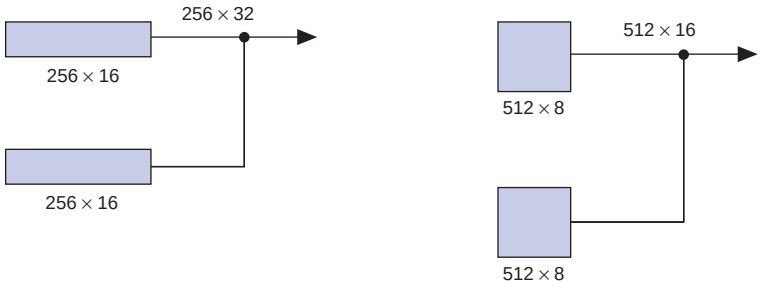
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16; 512 × 8; 1,024 × 4; or 2,048 × 2. Figure 5 shows the ACEX 1K EAB memory configurations.

Figure 5. ACEX 1K EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 block. Figure 6 shows examples of multiple EAB combination.

Figure 6. Examples of Combining ACEX 1K EABs



LE Operating Modes

The ACEX 1K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up / down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set DATA1 to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 11 shows the ACEX 1K LE operating modes.

Figure 11. ACEX 1K LE Operating Modes

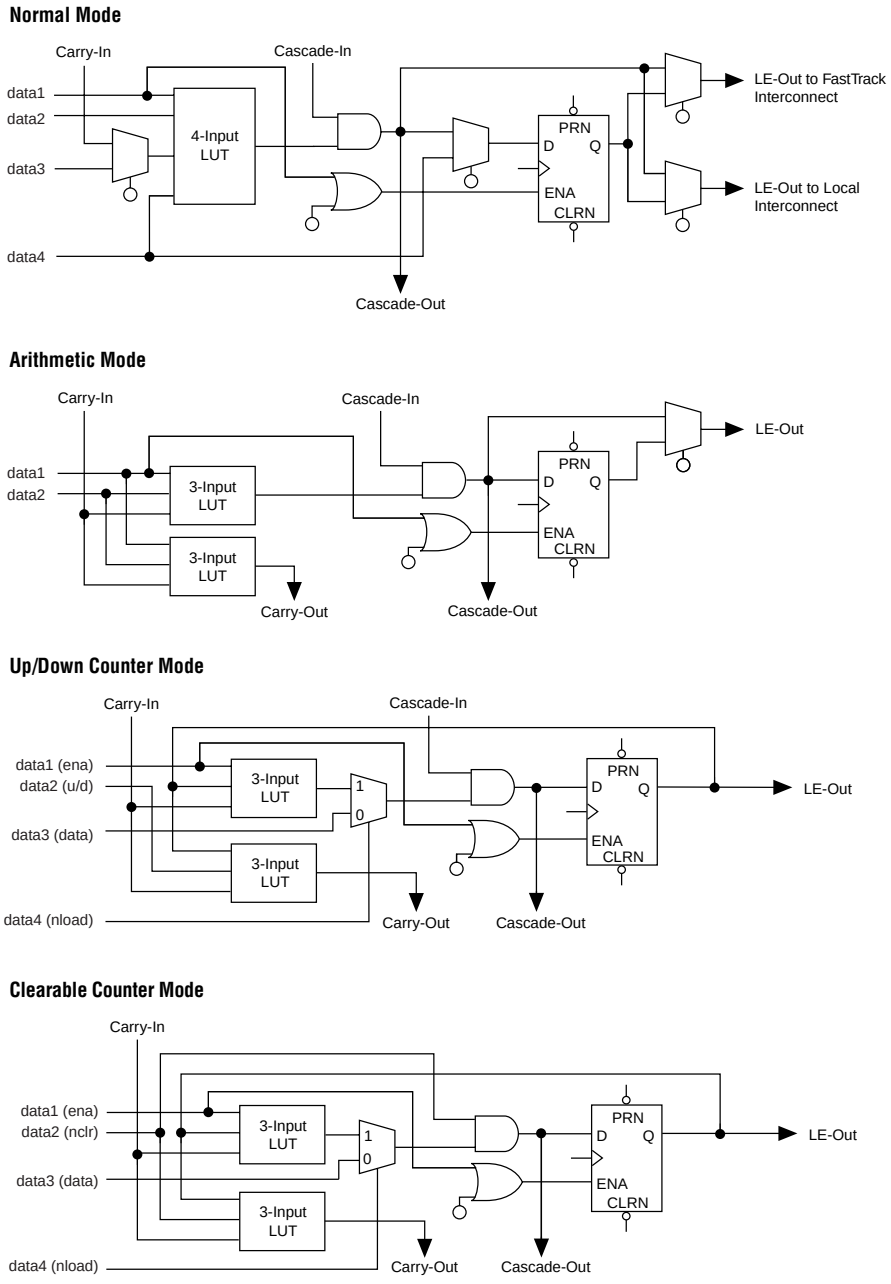
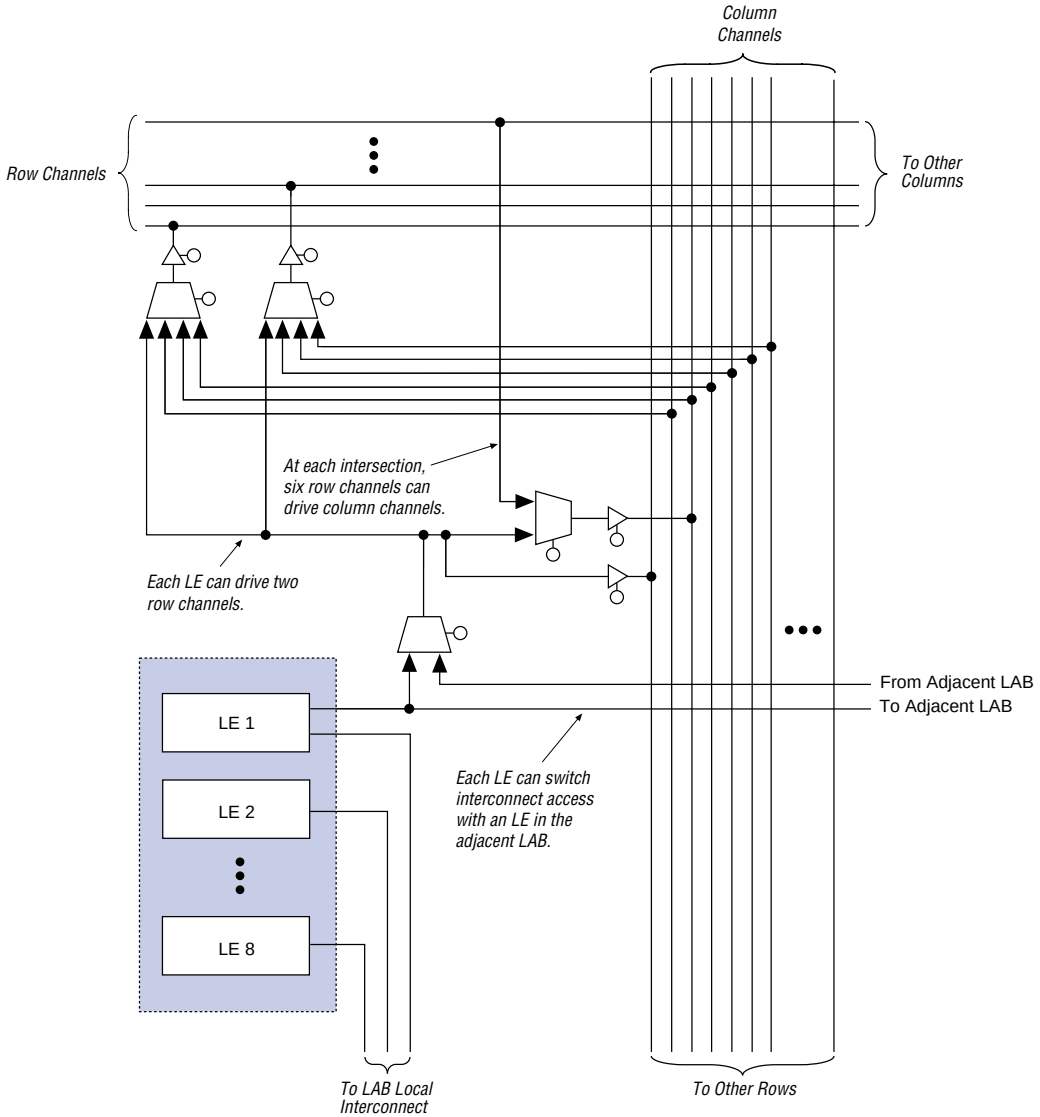


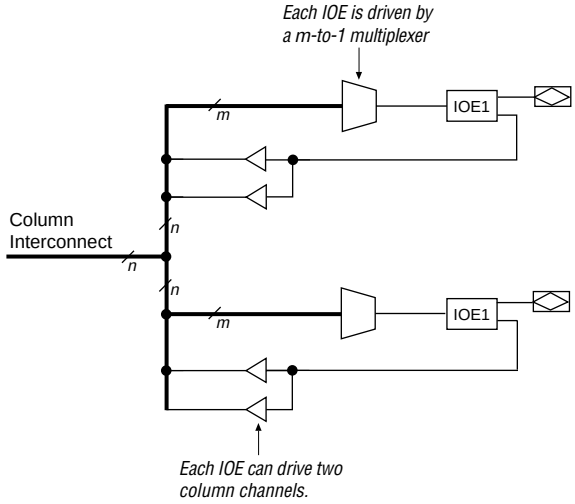
Figure 13. ACEX 1K LAB Connections to Row & Column Interconnect



Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

Figure 17. ACEX 1K Column-to-IOE Connections *Note (1)*



Note:
(1) The values for *m* and *n* are shown in Table 9.

Table 9 lists the ACEX 1K column-to-IOE interconnect resources.

Table 9. ACEX 1K Column-to-IOE Interconnect Resources

Device	Channels per Column *(n)*	Column Channels per Pin *(m)*
EP1K10	24	16
EP1K30	24	16
EP1K50	24	16
EP1K100	24	16

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0 V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 13 summarizes ACEX 1K MultiVolt I/O support.

Table 13. ACEX 1K MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled on an input which is driven with a voltage higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an ACEX 1K device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on ACEX 1K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a higher V_{IH} than LVTTL. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting the CMOS V_{OH} requirement. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot-Socketing

Because ACEX 1K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into ACEX 1K devices before and during power up without damaging the device. Additionally, ACEX 1K devices do not drive out during power up. Once operating conditions are reached, ACEX 1K devices operate as specified by the user.

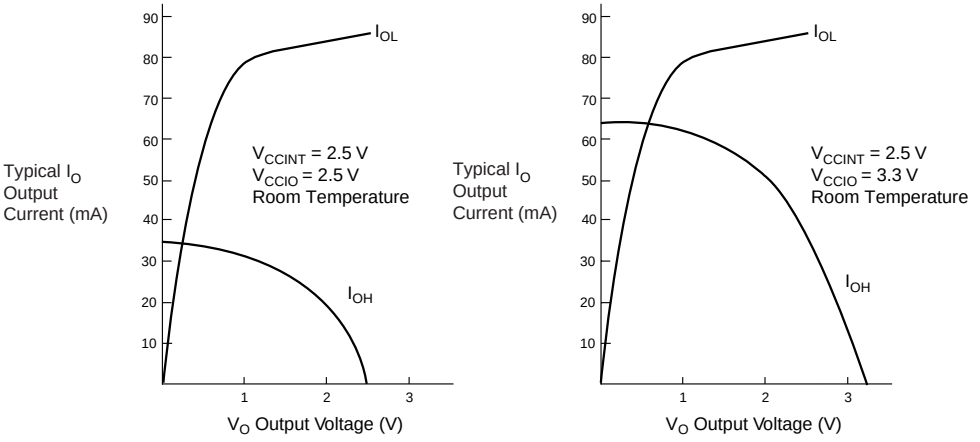
Table 21. ACEX 1K Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial- and extended-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the ACEX 1K Recommended Operating Conditions shown in Table 19 on page 46.
(8) The ACEX 1K input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 22.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed grade commercial temperature devices and -2 speed grade industrial and extended temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
(14) Capacitance is sample-tested only.

Figure 23. Output Drive Characteristics of ACEX 1K Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure accurate simulation and timing analysis as well as predictable performance. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and, therefore, have an unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay (t_{CO})
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Table 24. EAB Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABRE1}	Read enable delay to EAB for combinatorial input	
t_{EABRE2}	Read enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCLR}	EAB register asynchronous clear time to output delay	
t_{AA}	Address access delay (including the read enable to output delay)	
t_{WP}	Write pulse width	
t_{RP}	Read pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*(5)*
t_{WDH}	Data hold time after falling edge of write pulse	*(5)*
t_{WASU}	Address setup time before rising edge of write pulse	*(5)*
t_{WAH}	Address hold time after falling edge of write pulse	*(5)*
t_{RASU}	Address setup time before rising edge of read pulse	
t_{RAH}	Address hold time after falling edge of read pulse	
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	

Table 25. EAB Timing Macroparameters *Notes (1), (6)*		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Tables 27 through 29 describe the ACEX 1K external timing parameters and their symbols.

Table 27. External Reference Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(2)*

Table 28. External Timing Parameters

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	*(3)*
t_{INH}	Hold time with global clock at IOE register	*(3)*
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	*(3)*
t_{PCISU}	Setup time with global clock for registers used in PCI designs	*(3)*, *(4)*
t_{PCIH}	Hold time with global clock for registers used in PCI designs	*(3)*, *(4)*
t_{PCICO}	Clock-to-output delay with global clock for registers used in PCI designs	*(3)*, *(4)*

Table 29. External Bidirectional Timing Parameters *Note (3)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	CI = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	CI = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	CI = 35 pF

Notes to tables:

(1) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(2) Contact Altera Applications for test circuit specifications and test conditions.
(3) These timing parameters are sample-tested only.
(4) This parameter is measured with the measurement and test conditions, including load, specified in the ***PCI Local Bus Specification, Revision 2.2.***

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABBYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

Table 33. EP1K10 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		6.7		7.3		7.3	ns
$t_{EABRCCOMB}$	6.7		7.3		7.3		ns
$t_{EABRCREG}$	4.7		4.9		4.9		ns
t_{EABWP}	2.7		2.8		2.8		ns
$t_{EABWCCOMB}$	6.4		6.7		6.7		ns
$t_{EABWCREG}$	7.4		7.6		7.6		ns
t_{EABDD}		6.0		6.5		6.5	ns
$t_{EABDATACO}$		0.8		0.9		0.9	ns
$t_{EABDATASU}$	1.6		1.7		1.7		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.4		1.4		1.4		ns
t_{EABWEH}	0.1		0.0		0.0		ns
$t_{EABWDSU}$	1.6		1.7		1.7		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.1		3.4		3.4		ns
t_{EABWAH}	0.6		0.5		0.5		ns
t_{EABWO}		5.4		5.8		5.8	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
t_{EABWP}	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
t_{EABDD}		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
t_{EABWEH}	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
t_{EABWAH}	0.9		1.2		1.8		ns
t_{EABWO}		3.1		4.3		5.9	ns

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

Table 51. EP1K100 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		1.0		1.5	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		0.6		0.8		1.1	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.2		0.3		0.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.9		1.2	ns
t_{C}		0.8		1.0		1.4	ns
t_{CO}		0.6		0.8		1.1	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.4		0.6		0.7		ns
t_{H}	0.5		0.7		0.9		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.8		1.0		1.4	ns
t_{CH}	1.5		2.0		2.5		ns
t_{CL}	1.5		2.0		2.5		ns

Table 52. EP1K100 Device IOE Timing Microparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.7		2.0		2.6	ns
t_{IOC}		0.0		0.0		0.0	ns
t_{IOCO}		1.4		1.6		2.1	ns
t_{IOCOMB}		0.5		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.7		0.9		1.2		ns
t_{IOCLR}		0.5		0.7		0.9	ns
t_{OD1}		3.0		4.2		5.6	ns
t_{OD2}		3.0		4.2		5.6	ns
t_{OD3}		4.0		5.5		7.3	ns
t_{XZ}		3.5		4.6		6.1	ns
t_{ZX1}		3.5		4.6		6.1	ns
t_{ZX2}		3.5		4.6		6.1	ns
t_{ZX3}		4.5		5.9		7.8	ns
t_{INREG}		2.0		2.6		3.5	ns
t_{IOFD}		0.5		0.8		1.2	ns
t_{INCOMB}		0.5		0.8		1.2	ns

Table 54. EP1K100 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns