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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	186
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k50fc256-2

General Description

Altera® ACEX 1K devices provide a die-efficient, low-cost architecture by combining look-up table (LUT) architecture with EABs. LUT-based logic provides optimized performance and efficiency for data-path, register intensive, mathematical, or digital signal processing (DSP) designs, while EABs implement RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. These elements make ACEX 1K suitable for complex logic functions and memory functions such as digital signal processing, wide data-path manipulation, data transformation and microcontrollers, as required in high-performance communications applications. Based on reconfigurable CMOS SRAM elements, the ACEX 1K architecture incorporates all features necessary to implement common gate array megafunctions, along with a high pin count to enable an effective interface with system components. The advanced process and the low voltage requirement of the 2.5-V core allow ACEX 1K devices to meet the requirements of low-cost, high-volume applications ranging from DSL modems to low-cost switches.

The ability to reconfigure ACEX 1K devices enables complete testing prior to shipment and allows the designer to focus on simulation and design verification. ACEX 1K device reconfigurability eliminates inventory management for gate array designs and test vector generation for fault coverage.

Table 4 shows ACEX 1K device performance for some common designs. All performance results were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 4. ACEX 1K Device Performance

Application	Resources Used		Performance			
	LEs	EABs	Speed Grade			Units
			-1	-2	-3	
16-bit loadable counter	16	0	285	232	185	MHz
16-bit accumulator	16	0	285	232	185	MHz
16-to-1 multiplexer (1)	10	0	3.5	4.5	6.6	ns
16-bit multiplier with 3-stage pipeline (2)	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed (2)	0	1	278	196	143	MHz
256 × 16 RAM write cycle speed (2)	0	1	185	143	111	MHz

Notes:

- (1) This application uses combinatorial inputs and outputs.
- (2) This application uses registered inputs and outputs.



For more information on the configuration of ACEX 1K devices, see the following documents:

- [*Configuration Devices for ACEX, APEX, FLEX, & Mercury Devices Data Sheet*](#)
- [*MasterBlaster Serial/USB Communications Cable Data Sheet*](#)
- [*ByteBlasterMV Parallel Port Download Cable Data Sheet*](#)
- [*BitBlaster Serial Download Cable Data Sheet*](#)

ACEX 1K devices are supported by Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the ACEX 1K device architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information, see the [*MAX+PLUS II Programmable Logic Development System & Software Data Sheet*](#) and the [*Quartus Programmable Logic Development System & Software Data Sheet*](#).

Functional Description

Each ACEX 1K device contains an enhanced embedded array that implements memory and specialized logic functions, and a logic array that implements general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input LUT, a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable logic gates.

Signal interconnections within ACEX 1K devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.1 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 2.5 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the ACEX 1K device architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Embedded Array Block

The EAB is a flexible block of RAM, with registers on the input and output ports, that is used to implement common gate array megafunctions. Because it is large and flexible, the EAB is suitable for functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

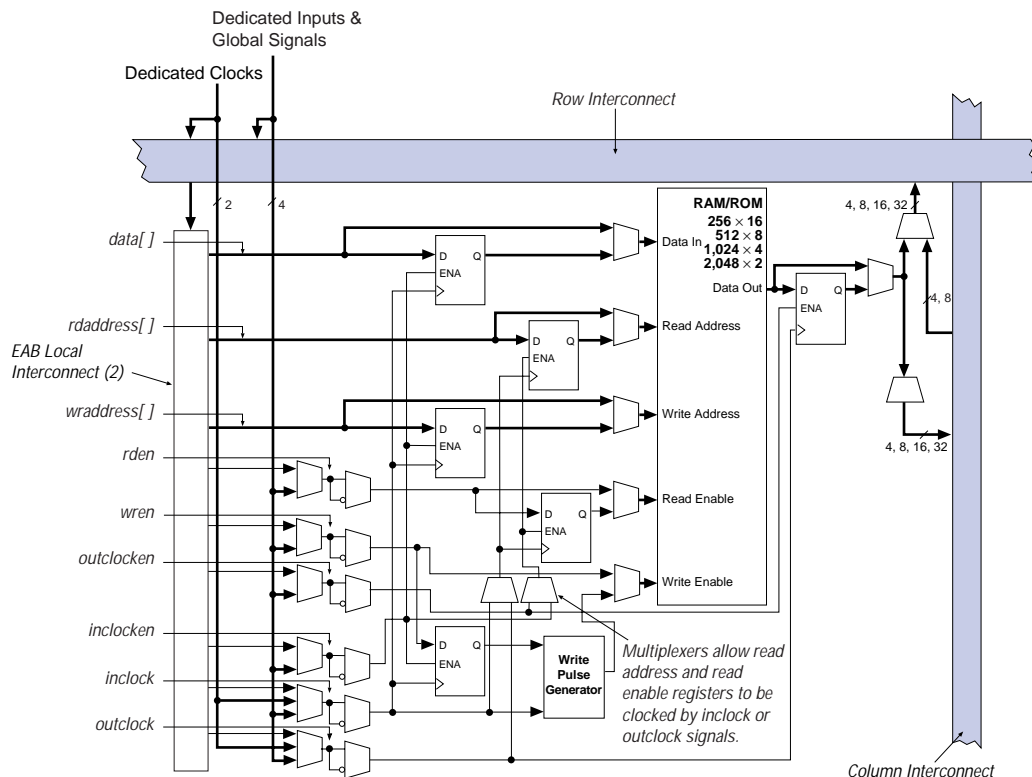
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in a single logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement any function with 8 inputs and 16 outputs. Parameterized functions, such as LPM functions, can take advantage of the EAB automatically.

The ACEX 1K enhanced EAB supports dual-port RAM. The dual-port structure is ideal for FIFO buffers with one or two clocks. The ACEX 1K EAB can also support up to 16-bit-wide RAM blocks. The ACEX 1K EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, allowing the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allow independent control of these sections.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous reads or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see [Figure 2](#)).

Figure 2. ACEX 1K Device in Dual-Port RAM Mode *Note (1)*



Notes:

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafuncions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the ACEX 1K architecture, has a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure. [Figure 8](#) shows the ACEX 1K LE.

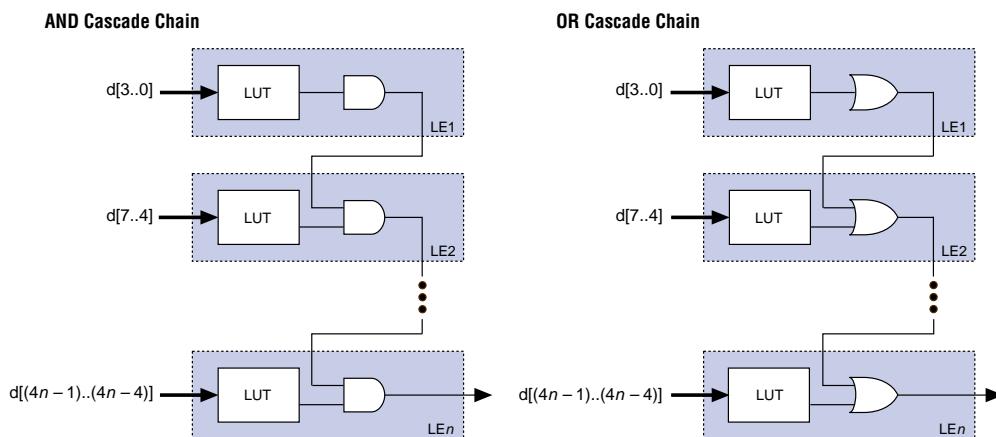
Cascade Chain

With the cascade chain, the ACEX 1K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. With a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EP1K50 device, the cascade chain stops at the eighteenth LAB, and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. The LE delay is 1.3 ns; the cascade chain delay is 0.6 ns. With the cascade chain, decoding a 16-bit address requires 3.1 ns.

Figure 10. ACEX 1K Cascade Chain Operation



LE Operating Modes

The ACEX 1K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

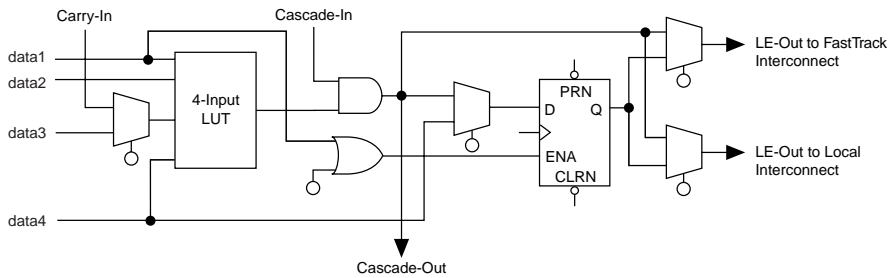
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

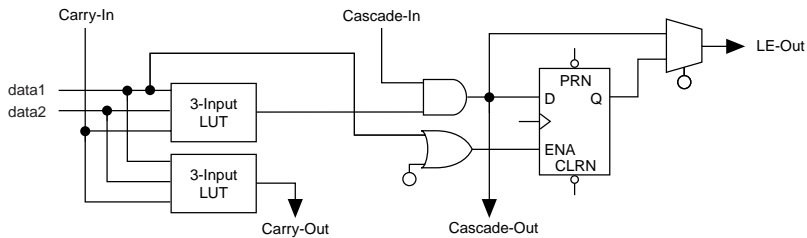
Figure 11 shows the ACEX 1K LE operating modes.

Figure 11. ACEX 1K LE Operating Modes

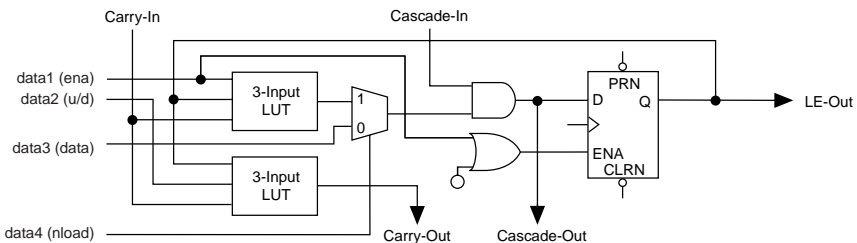
Normal Mode



Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode

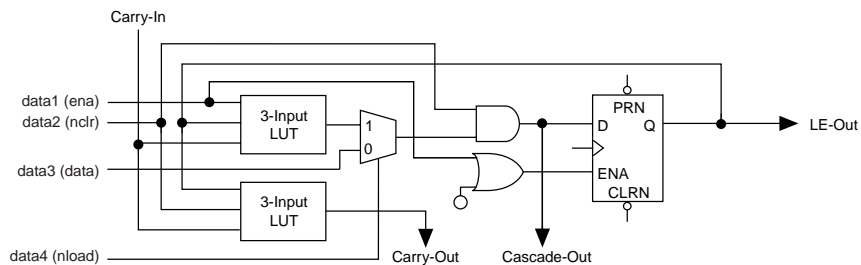
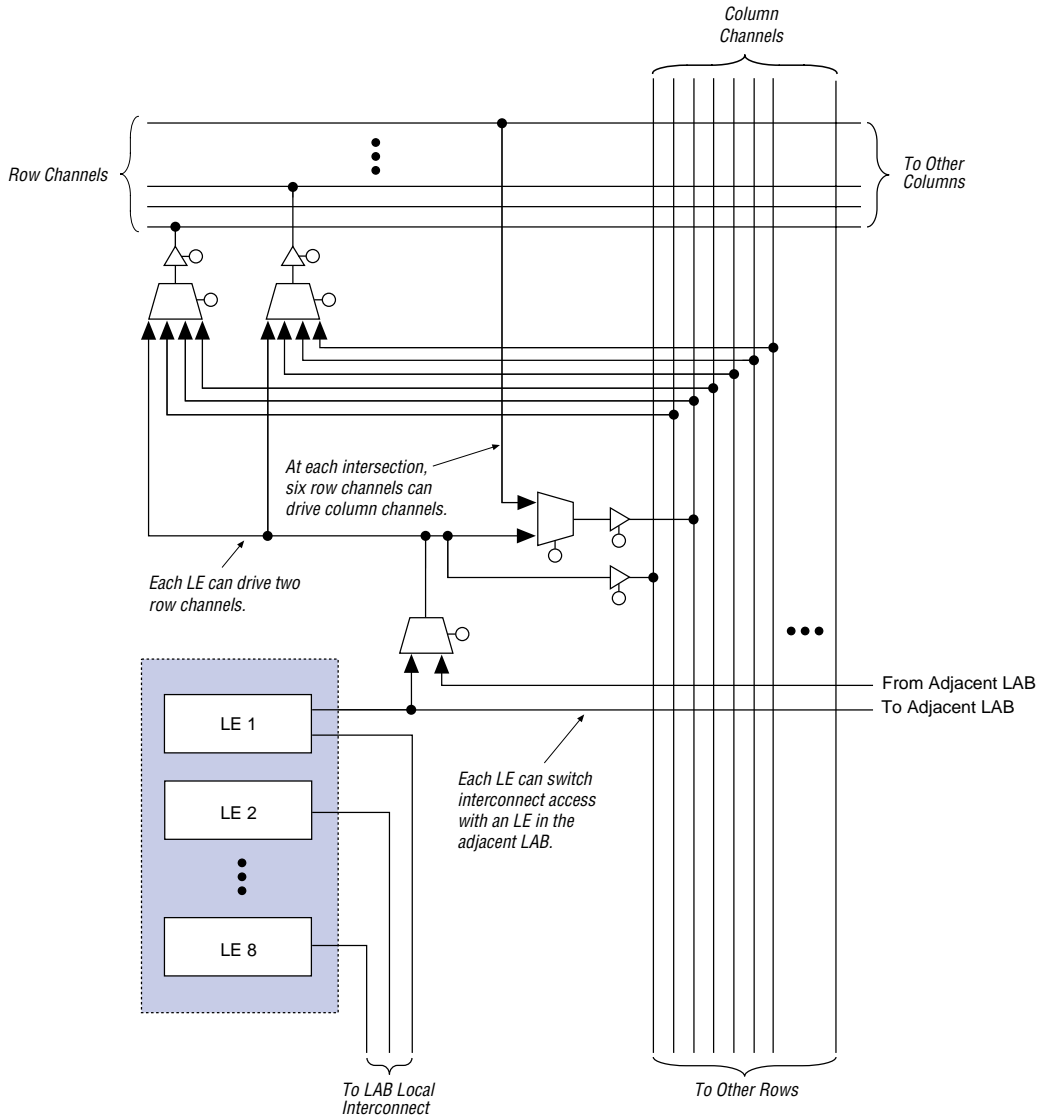


Figure 13. ACEX 1K LAB Connections to Row & Column Interconnect



When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Table 7 lists the sources for each peripheral control signal and shows how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. **Table 7** also shows the rows that can drive global signals.

Table 7. Peripheral Bus Sources for ACEX Devices

Peripheral Control Signal	EP1K10	EP1K30	EP1K50	EP1K100
OE0	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C
OE2	Row B	Row C	Row D	Row E
OE3	Row B	Row D	Row F	Row L
OE4	Row C	Row E	Row H	Row I
OE5	Row C	Row F	Row J	Row K
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row F
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row C	Row D
CLKENA2/CLR0	Row B	Row C	Row E	Row B
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row G	Row H
CLKENA4/CLR1	Row C	Row E	Row I	Row J
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row J	Row G

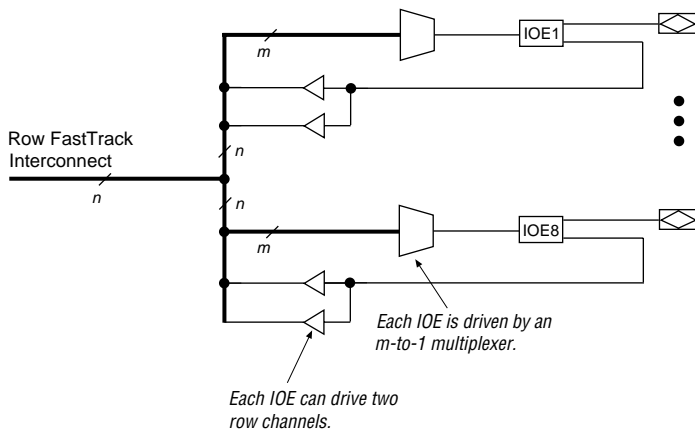
Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

The chip-wide output enable pin is an active-high pin that can be used to tri-state all pins on the device. This option can be set in the Altera software. The built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. ACEX 1K Row-to-IOE Connections *Note (1)*



Note:

(1) The values for m and n are shown in Table 8.

Table 8 lists the ACEX 1K row-to-IOE interconnect resources.

Table 8. ACEX 1K Row-to-IOE Interconnect Resources		
Device	Channels per Row (n)	Row Channels per Pin (m)
EP1K10	144	18
EP1K30	216	27
EP1K50	216	27
EP1K100	312	39

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 11. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the Altera software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250 (4)	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Table 12. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		80	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		40	MHz
f_{CLKDEV}	Input deviation from user specification in the software (1)				25,000	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250 (4)	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes to tables:

- (1) To implement the ClockLock and ClockBoost circuitry with the Altera software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.
- (4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

I/O Configuration

This section discusses the PCI pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for ACEX 1K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT} . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

Table 34. EP1K10 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.3		2.7		3.6	ns
t_{DIN2LE}		0.8		1.1		1.4	ns
$t_{DIN2DATA}$		1.1		1.4		1.8	ns
$t_{DCLK2IOE}$		2.3		2.7		3.6	ns
$t_{DCLK2LE}$		0.8		1.1		1.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.8		2.1		2.9	ns
$t_{SAMECOLUMN}$		0.3		0.4		0.7	ns
$t_{DIFFROW}$		2.1		2.5		3.6	ns
$t_{TROWROWS}$		3.9		4.6		6.5	ns
$t_{LEPERIPH}$		3.3		3.7		4.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.0		1.4	ns

Table 35. EP1K10 External Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t _{DDR}		7.5		9.5		12.5	ns
t _{INSU} (2), (3)	2.4		2.7		3.6		ns
t _{INH} (2), (3)	0.0		0.0		0.0		ns
t _{OUTCO} (2), (3)	2.0	6.6	2.0	7.8	2.0	9.6	ns
t _{INSU} (4), (3)	1.4		1.7		–		ns
t _{INH} (4), (3)	0.5	5.1	0.5	6.4	–	–	ns
t _{OUTCO} (4), (3)	0.0		0.0		–		ns
t _{PCISU} (3)	3.0		4.2		6.4		ns
t _{PCIH} (3)	0.0		0.0		–		ns
t _{PCICO} (3)	2.0	6.0	2.0	7.5	2.0	10.2	ns

Table 41. EP1K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 42. EP1K30 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t _{DDR}		8.0		9.5		12.5	ns
t _{INSU} (3)	2.1		2.5		3.9		ns
t _{INH} (3)	0.0		0.0		0.0		ns
t _{OUTCO} (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t _{INSU} (4)	1.1		1.5		–		ns
t _{INH} (4)	0.0		0.0		–		ns
t _{OUTCO} (4)	0.5	3.9	0.5	4.9	–	–	ns
t _{PCISU}	3.0		4.2		–		ns
t _{PCIH}	0.0		0.0		–		ns
t _{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
t_{EABWP}	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
t_{EABDD}		3.8		5.3		7.2	ns
$t_{EABDATAO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
t_{EABWEH}	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
t_{EABWAH}	0.9		1.2		1.8		ns
t_{EABWO}		3.1		4.3		5.9	ns

Table 54. EP1K100 Device EAB Internal Timing Macroparameters

Note (1)

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATA CO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Revision History

The information contained in the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4 supersedes information published in previous versions.

The following changes were made to the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4: added extended temperature support.