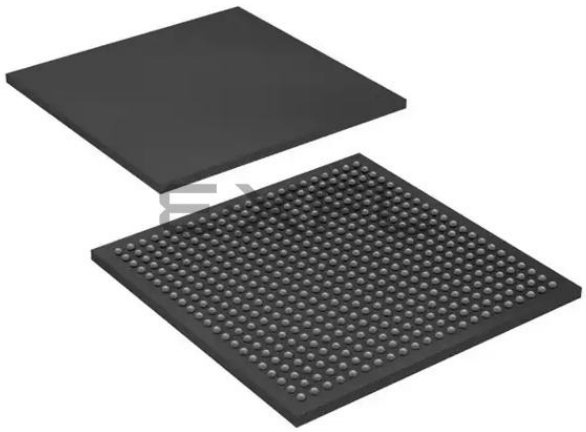

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	249
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k50fc484-2

Table 5 shows ACEX 1K device performance for more complex designs. These designs are available as Altera MegaCore™ functions.

Table 5. ACEX 1K Device Performance for Complex Designs

Application	LEs Used	Performance			
		Speed Grade			Units
		-1	-2	-3	
16-bit, 8-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point Fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	µs
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Each ACEX 1K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

ACEX 1K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers EPC16, EPC2, EPC1, and EPC1441 configuration devices, which configure ACEX 1K devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cables. After an ACEX 1K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 40 ms, real-time changes can be made during system operation.

ACEX 1K devices contain an interface that permits microprocessors to configure ACEX 1K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat an ACEX 1K device as memory and configure it by writing to a virtual memory location, simplifying device reconfiguration.

If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write-enable, read-enable, and clock-enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write-enable, read-enable, clear, clock, and clock-enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

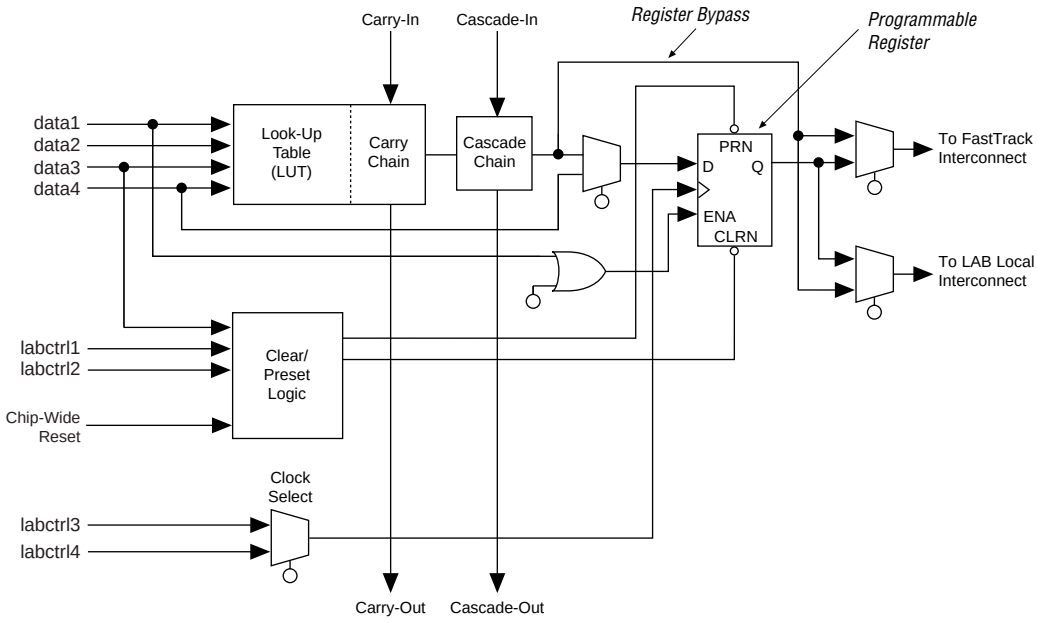
An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the ACEX 1K architecture, facilitating efficient routing with optimum device utilization and high performance. Figure 7 shows the ACEX 1K LAB.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the ACEX 1K architecture, has a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure. Figure 8 shows the ACEX 1K LE.

Figure 8. ACEX 1K Logic Element



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the LUT's output drives the LE's output.

The LE has two outputs that drive the interconnect: one drives the local interconnect, and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The ACEX 1K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders, and the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the register's input and output. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset, and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect Routing Structure

In the ACEX 1K architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

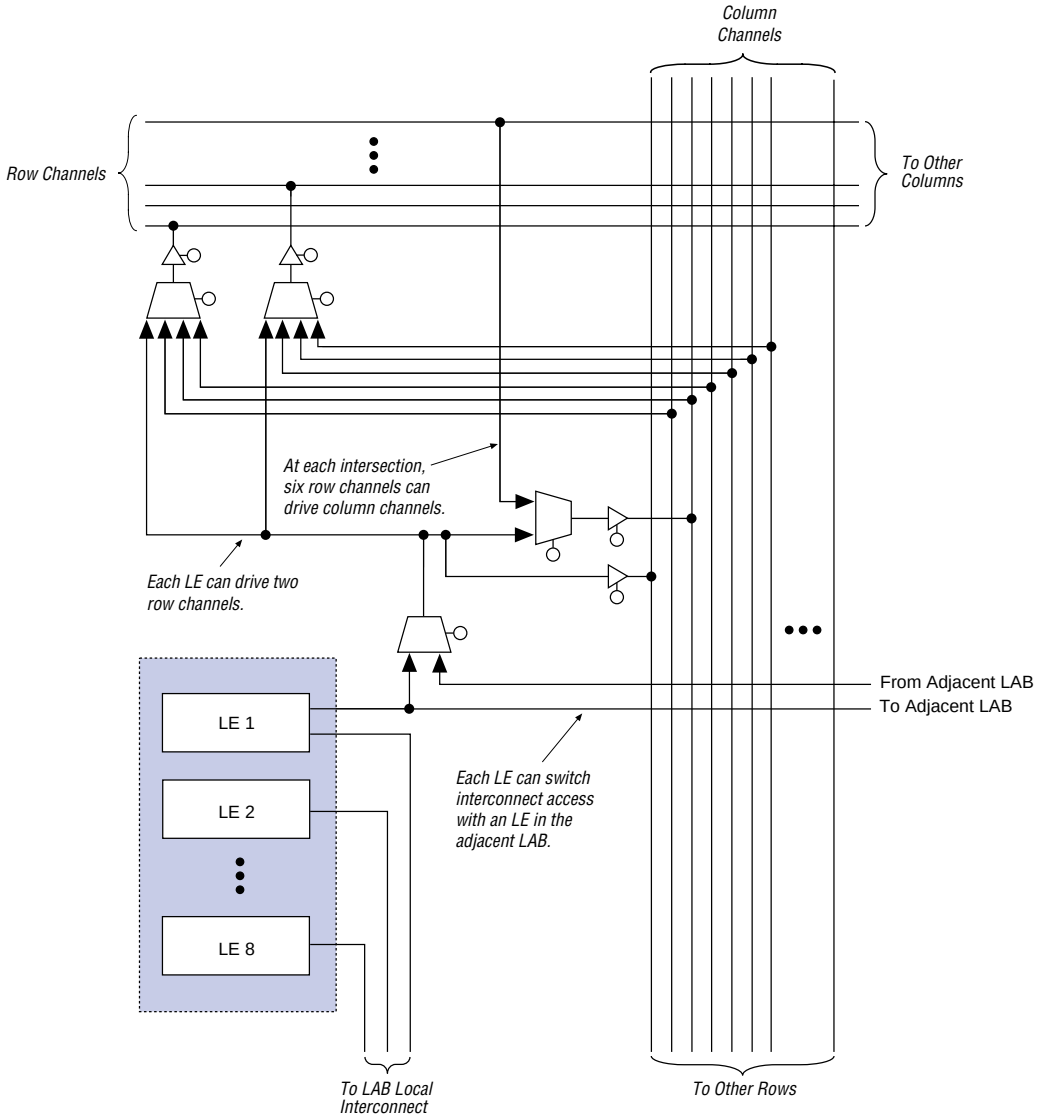
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently. Figure 13 shows the ACEX 1K LAB.

Figure 13. ACEX 1K LAB Connections to Row & Column Interconnect



When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Table 7 lists the sources for each peripheral control signal and shows how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. Table 7 also shows the rows that can drive global signals.

Table 7. Peripheral Bus Sources for ACEX Devices

Peripheral Control Signal	EP1K10	EP1K30	EP1K50	EP1K100
OE0	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C
OE2	Row B	Row C	Row D	Row E
OE3	Row B	Row D	Row F	Row L
OE4	Row C	Row E	Row H	Row I
OE5	Row C	Row F	Row J	Row K
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row F
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row C	Row D
CLKENA2/CLR0	Row B	Row C	Row E	Row B
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row G	Row H
CLKENA4/CLR1	Row C	Row E	Row I	Row J
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row J	Row G

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

The chip-wide output enable pin is an active-high pin that can be used to tri-state all pins on the device. This option can be set in the Altera software. The built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

For more information, search for “SameFrame” in MAX+PLUS II Help.

Table 10. ACEX 1K SameFrame Pin-Out Support

Device	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	✓	*(1)*
EP1K30	✓	*(1)*
EP1K50	✓	✓
EP1K100	✓	✓

Note:
(1) This option is supported with a 256-pin FineLine BGA package and SameFrame migration.

ClockLock & ClockBoost Features

To support high-speed designs, -1 and -2 speed grade ACEX 1K devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in ACEX 1K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry lock onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

PCI Pull-Up Clamping Diode Option

ACEX 1K devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When V_{CCIO} is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which allows a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

Open-Drain Output Option

ACEX 1K devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

MultiVolt I/O Interface

The ACEX 1K device architecture supports the MultiVolt I/O interface feature, which allows ACEX 1K devices in all packages to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0 V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 13 summarizes ACEX 1K MultiVolt I/O support.

Table 13. ACEX 1K MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled on an input which is driven with a voltage higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an ACEX 1K device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on ACEX 1K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a higher V_{IH} than LVTTL. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting the CMOS V_{OH} requirement. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot-Socketing

Because ACEX 1K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into ACEX 1K devices before and during power up without damaging the device. Additionally, ACEX 1K devices do not drive out during power up. Once operating conditions are reached, ACEX 1K devices operate as specified by the user.

Table 25. EAB Timing Macroparameters *Notes (1), (6)*		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Tables 30 through 36 show EP1K10 device internal and external timing parameters.

Table 30. EP1K10 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		0.9		1.0		1.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.7		0.9		1.1	ns
t_{C}		1.1		1.3		1.7	ns
t_{CO}		0.5		0.7		0.9	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.7		0.8		1.0		ns
t_{H}	0.9		1.0		1.1		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABBYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

Table 36. EP1K10 External Bidirectional Timing Parameters *Notes (1), (3)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (2)	2.2		2.3		3.2		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	2.0	6.6	2.0	7.8	2.0	9.6	ns
$t_{XZBIDIR}$ (2)		8.8		11.2		14.0	ns
$t_{ZXBIDIR}$ (2)		8.8		11.2		14.0	ns
$t_{INSUBIDIR}$ (4)	3.1		3.3		–	–	
$t_{INHBIDIR}$ (4)	0.0		0.0		–		
$t_{OUTCOBIDIR}$ (4)	0.5	5.1	0.5	6.4	–	–	ns
$t_{XZBIDIR}$ (4)		7.3		9.2		–	ns
$t_{ZXBIDIR}$ (4)		7.3		9.2		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 22 through 29 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) These parameters are specified by characterization.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.8		1.0	ns
t_{C}		0.0		0.0		0.0	ns
t_{CO}		0.3		0.4		0.5	ns

Table 41. EP1K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 42. EP1K30 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(3)*	2.1		2.5		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	4.9	2.0	5.9	2.0	7.6	ns
t_{INSU} *(4)*	1.1		1.5		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.9	0.5	4.9	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 48. EP1K50 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
t_{DIN2LE}		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

Table 49. EP1K50 External Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(2)*	2.4		2.9		3.9		ns
t_{INH} *(2)*	0.0		0.0		0.0		ns
t_{OUTCO} *(2)*	2.0	4.3	2.0	5.2	2.0	7.3	ns
t_{INSU} *(3)*	2.4		2.9		–		ns
t_{INH} *(3)*	0.0		0.0		–		ns
t_{OUTCO} *(3)*	0.5	3.3	0.5	4.1	–	–	ns
t_{PCISU}	2.4		2.9		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.7	–	–	ns

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

Table 51. EP1K100 Device LE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		1.0		1.5	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		0.6		0.8		1.1	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.2		0.3		0.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.9		1.2	ns
t_{C}		0.8		1.0		1.4	ns
t_{CO}		0.6		0.8		1.1	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.4		0.6		0.7		ns
t_{H}	0.5		0.7		0.9		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.8		1.0		1.4	ns
t_{CH}	1.5		2.0		2.5		ns
t_{CL}	1.5		2.0		2.5		ns

Table 54. EP1K100 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 55. EP1K100 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.6		4.4	ns
t_{DIN2LE}		0.3		0.4		0.5	ns
$t_{DIN2DATA}$		1.6		1.8		2.0	ns
$t_{DCLK2IOE}$		0.8		1.1		1.4	ns
$t_{DCLK2LE}$		0.3		0.4		0.5	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		2.5		3.4	ns
$t_{SAMECOLUMN}$		0.4		1.0		1.6	ns
$t_{DIFFROW}$		1.9		3.5		5.0	ns
$t_{TWOROWS}$		3.4		6.0		8.4	ns
$t_{LEPERIPH}$		4.3		5.4		6.5	ns
$t_{LABCARRY}$		0.5		0.7		0.9	ns
$t_{LABCASC}$		0.8		1.0		1.4	ns

Table 56. EP1K100 External Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	2.0		2.5		3.3		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t_{INSU} *(4)*	2.0		2.2		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns