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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	147
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1k50qc208-1n

- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations
- Flexible package options are available in 100 to 484 pins, including the innovative FineLine BGA™ packages (see [Tables 2 and 3](#))
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplcity, VeriBest, and Viewlogic

Table 2. ACEX 1K Package Options & I/O Pin Count *Notes (1), (2)*

Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
EP1K10	66	92	120	136	136 (3)
EP1K30		102	147	171	171 (3)
EP1K50		102	147	186	249
EP1K100			147	186	333

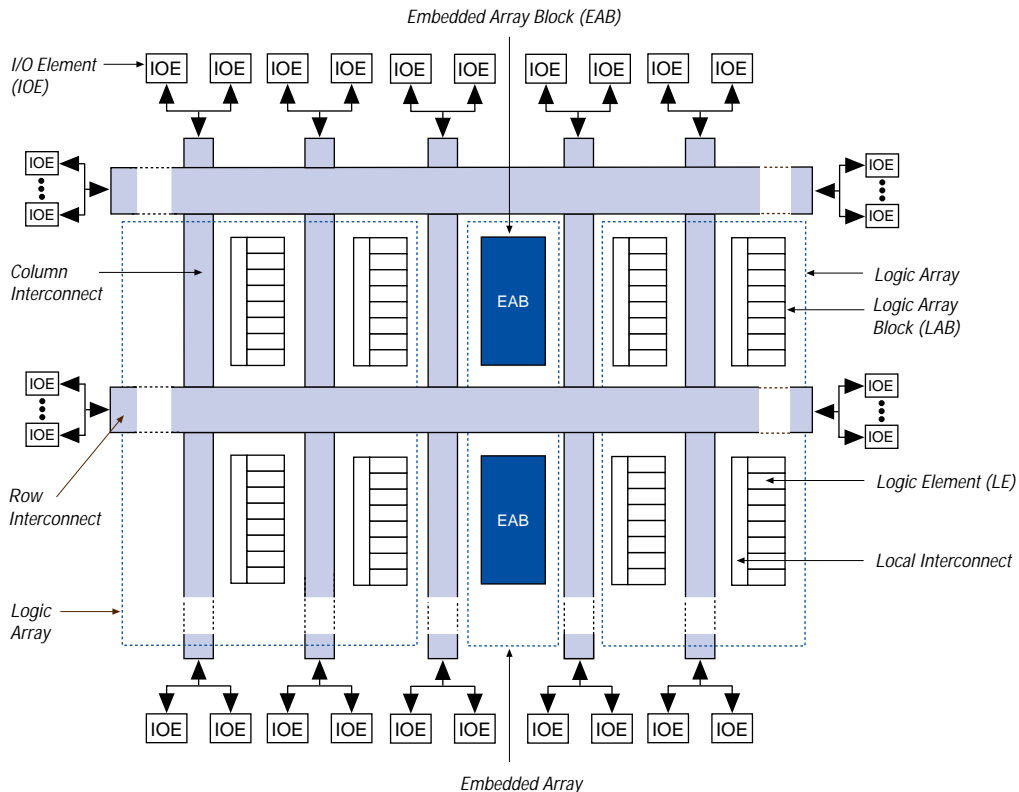
Notes:

- (1) ACEX 1K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and FineLine BGA packages.
- (2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
- (3) This option is supported with a 256-pin FineLine BGA package. By using SameFrame™ pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin and 484-pin FineLine BGA packages.

Table 3. ACEX 1K Package Sizes

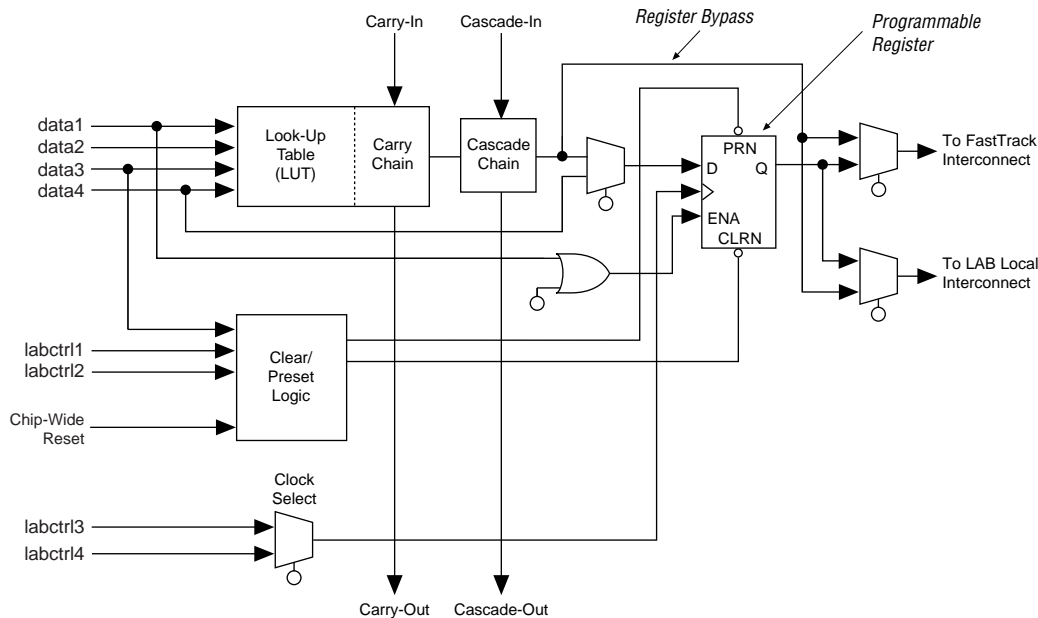
Device	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.0
Area (mm ²)	256	484	936	289	529
Length × width (mm × mm)	16 × 16	22 × 22	30.6 × 30.6	17 × 17	23 × 23

Figure 1. ACEX 1K Device Block Diagram



ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Figure 8. ACEX 1K Logic Element



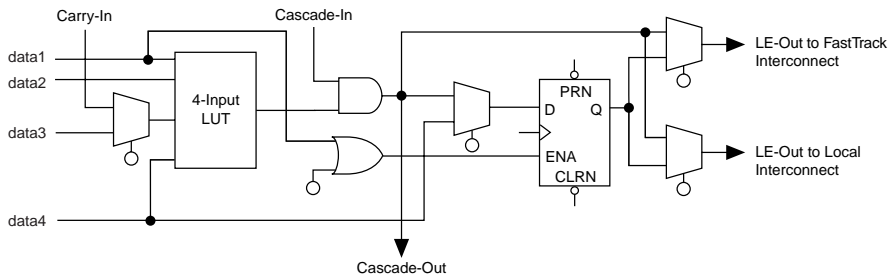
The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinational functions, the flipflop is bypassed and the LUT's output drives the LE's output.

The LE has two outputs that drive the interconnect: one drives the local interconnect, and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

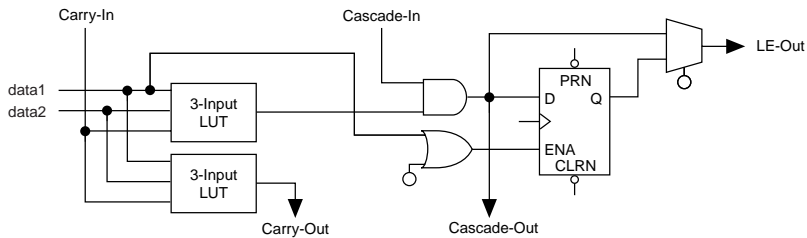
The ACEX 1K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders, and the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

Figure 11. ACEX 1K LE Operating Modes

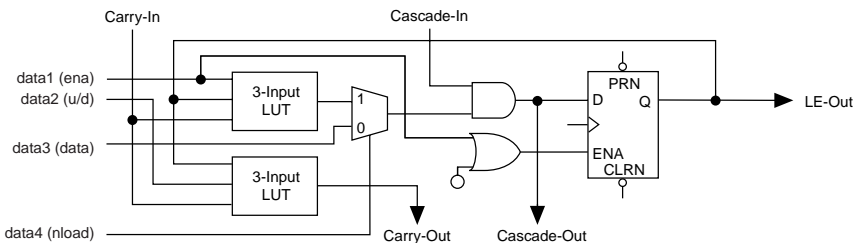
Normal Mode



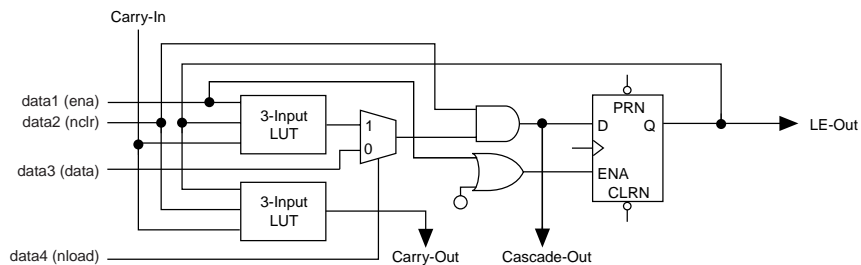
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 11](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but it supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

On all ACEX 1K devices, the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock-enable or eight output-enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock, and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on an LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

Figure 20. ACEX 1K JTAG Waveforms

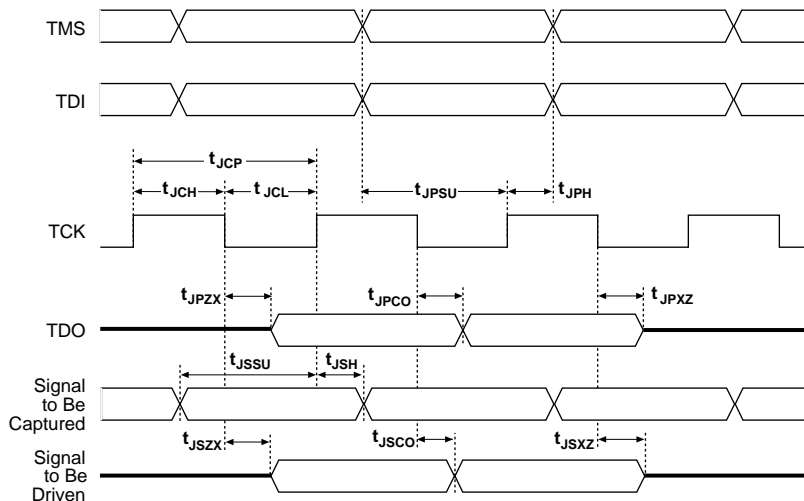


Table 17 shows the timing parameters and values for ACEX 1K devices.

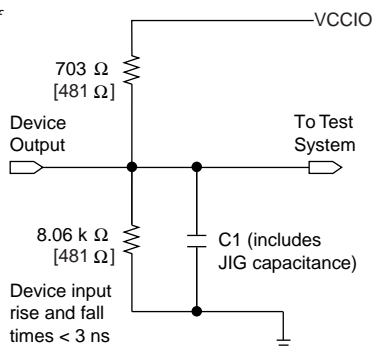
Table 17. ACEX 1K JTAG Timing Parameters & Values				
Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in [Figure 21](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. ACEX 1K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



Operating Conditions

[Tables 18](#) through [21](#) provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

Table 18. ACEX 1K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I			–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	°C

Table 20. ACEX 1K Device DC Operating Conditions (Part 2 of 2) Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 12 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (10)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (10)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (10)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 2.375 \text{ V}$ (10)			0.2	V
		$I_{OL} = 1 \text{ mA DC}$, $V_{CCIO} = 2.375 \text{ V}$ (10)			0.4	V
		$I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 2.375 \text{ V}$ (10)			0.7	V
I_I	Input pin leakage current	$V_I = 5.3 \text{ to } -0.3 \text{ V}$ (11)	-10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.3 \text{ to } -0.3 \text{ V}$ (11)	-10		10	μA
I_{CC0}	V_{CC} supply current (standby)	$V_I = \text{ground}$, no load, no toggling inputs		5		mA
		$V_I = \text{ground}$, no load, no toggling inputs (12)		10		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0 \text{ V}$ (13)	20		50	$\text{k}\Omega$
		$V_{CCIO} = 2.375 \text{ V}$ (13)	30		80	$\text{k}\Omega$

Table 25. EAB Timing Macroparameters *Notes (1), (6)*

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB \overline{WE} setup time before clock when using input register	
t_{EABWEH}	EAB \overline{WE} hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 26. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	(7)
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TROWROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial or industrial and extended use in ACEX 1K devices
- (3) Operating conditions: $V_{CCIO} = 2.5\text{ V} \pm 5\%$ for commercial or industrial and extended use in ACEX 1K devices.
- (4) Operating conditions: $V_{CCIO} = 2.5\text{ V}$ or 3.3 V .
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 31. EP1K10 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.6		3.1		4.0	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		0.9		1.0		1.4	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.3		1.5		2.0		ns
t_{IOH}	0.9		1.0		1.4		ns
t_{IOCLR}		1.1		1.3		1.7	ns
t_{OD1}		3.1		3.7		4.1	ns
t_{OD2}		2.6		3.3		3.9	ns
t_{OD3}		5.8		6.9		8.3	ns
t_{XZ}		3.8		4.5		5.9	ns
t_{ZX1}		3.8		4.5		5.9	ns
t_{ZX2}		3.3		4.1		5.7	ns
t_{ZX3}		6.5		7.7		10.1	ns
t_{INREG}		3.7		4.3		5.7	ns
t_{IOFD}		0.9		1.0		1.4	ns
t_{INCOMB}		1.9		2.3		3.0	ns

Table 32. EP1K10 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		1.9		1.9	ns
$t_{EABDATA2}$		0.6		0.7		0.7	ns
t_{EABWE1}		1.2		1.2		1.2	ns
t_{EABWE2}		0.4		0.4		0.4	ns
t_{EABRE1}		0.9		0.9		0.9	ns
t_{EABRE2}		0.4		0.4		0.4	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.3	ns
$t_{EABYPASS}$		0.5		0.6		0.6	ns
t_{EABSU}	1.0		1.0		1.0		ns
t_{EABH}	0.5		0.4		0.4		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.4		3.6		3.6	ns
t_{WP}	2.7		2.8		2.8		ns
t_{RP}	1.0		1.0		1.0		ns
t_{WDSU}	1.0		1.0		1.0		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.8		1.9		1.9		ns
t_{WAH}	1.9		2.0		2.0		ns
t_{RASU}	3.1		3.5		3.5		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.7		2.8		2.8	ns
t_{DD}		2.7		2.8		2.8	ns
t_{EABOUT}		0.5		0.6		0.6	ns
t_{EABCH}	1.5		2.0		2.0		ns
t_{EABCL}	2.7		2.8		2.8		ns

Table 36. EP1K10 External Bidirectional Timing Parameters *Notes (1), (3)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR} (2)	2.2		2.3		3.2		ns
t _{INHBIDIR} (2)	0.0		0.0		0.0		ns
t _{OUTCOBIDIR} (2)	2.0	6.6	2.0	7.8	2.0	9.6	ns
t _{XZBIDIR} (2)		8.8		11.2		14.0	ns
t _{ZXBIDIR} (2)		8.8		11.2		14.0	ns
t _{INSUBIDIR} (4)	3.1		3.3		–	–	
t _{INHBIDIR} (4)	0.0		0.0		–		
t _{OUTCOBIDIR} (4)	0.5	5.1	0.5	6.4	–	–	ns
t _{XZBIDIR} (4)		7.3		9.2		–	ns
t _{ZXBIDIR} (4)		7.3		9.2		–	ns

Notes to tables:

- (1) All timing parameters are described in Tables 22 through 29 in this data sheet.
 (2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
 (3) These parameters are specified by characterization.
 (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 37 through 43 show EP1K30 device internal and external timing parameters.

Table 37. EP1K30 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.8		1.0	ns
t_C		0.0		0.0		0.0	ns
t_{CO}		0.3		0.4		0.5	ns

Table 40. EP1K30 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
t_{EABWP}	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
t_{EABDD}		5.7		6.7		7.7	ns
$t_{EABDATAO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
t_{EABWAH}	0.5		0.5		0.4		ns
t_{EABWO}		5.1		6.0		6.8	ns

Table 44. EP1K50 Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.6		0.6		0.7	ns
t_{COMB}		0.3		0.4		0.5	ns
t_{SU}	0.5		0.6		0.7		ns
t_H	0.5		0.6		0.8		ns
t_{PRE}		0.4		0.5		0.7	ns
t_{CLR}		0.8		1.0		1.2	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 45. EP1K50 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.3		1.9	ns
t_{IOC}		0.3		0.4		0.4	ns
t_{IOCO}		1.7		2.1		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.4		0.5		0.6		ns
t_{IOCLR}		0.2		0.2		0.4	ns
t_{OD1}		1.2		1.2		1.9	ns
t_{OD2}		0.7		0.8		1.7	ns
t_{OD3}		2.7		3.0		4.3	ns
t_{XZ}		4.7		5.7		7.5	ns
t_{ZX1}		4.7		5.7		7.5	ns
t_{ZX2}		4.2		5.3		7.3	ns
t_{ZX3}		6.2		7.5		9.9	ns
t_{INREG}		3.5		4.2		5.6	ns
t_{IOFD}		1.1		1.3		1.8	ns
t_{INCOMB}		1.1		1.3		1.8	ns

Table 47. EP1K50 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
t_{EABWP}	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
t_{EABDD}		3.8		5.3		7.2	ns
$t_{EABDATA CO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
t_{EABWEH}	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
t_{EABWAH}	0.9		1.2		1.8		ns
t_{EABWO}		3.1		4.3		5.9	ns

Table 53. EP1K100 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA1}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.1		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.1		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \text{ (}\mu\text{A)}$$

Where:

- f_{MAX} = Maximum operating frequency in MHz
- N = Total number of LEs used in the device
- tog_{LC} = Average percent of LEs toggling at each clock (typically 12.5%)
- K = Constant

Table 58 provides the constant (K) values for ACEX 1K devices.

Table 58. ACEX 1K Constant Values	
Device	K Value
EP1K10	4.5
EP1K30	4.5
EP1K50	4.5
EP1K100	4.5

This supply power calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect ACEX 1K devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of ACEX 1K devices. For information on other ACEX 1K devices, contact Altera Applications at (800) 800-EPLD.