



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	147
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1k50qc208-2n">https://www.e-xfl.com/product-detail/intel/ep1k50qc208-2n</a>

## ...and More Features

- -1 speed grade devices are compliant with **PCI Local Bus Specification, Revision 2.2** for 5.0-V operation
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming additional device logic.
- Operate with a 2.5-V internal supply voltage
- In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay, clock skew, and clock multiplication
- Built-in, low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - Clamp to  $V_{CCIO}$  user-selectable on a pin-by-pin basis
  - Supports hot-socketing



For more information on the configuration of ACEX 1K devices, see the following documents:

- [\*Configuration Devices for ACEX, APEX, FLEX, & Mercury Devices Data Sheet\*](#)
- [\*MasterBlaster Serial/USB Communications Cable Data Sheet\*](#)
- [\*ByteBlasterMV Parallel Port Download Cable Data Sheet\*](#)
- [\*BitBlaster Serial Download Cable Data Sheet\*](#)

ACEX 1K devices are supported by Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the ACEX 1K device architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information, see the [\*MAX+PLUS II Programmable Logic Development System & Software Data Sheet\*](#) and the [\*Quartus Programmable Logic Development System & Software Data Sheet\*](#).

## Functional Description

Each ACEX 1K device contains an enhanced embedded array that implements memory and specialized logic functions, and a logic array that implements general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

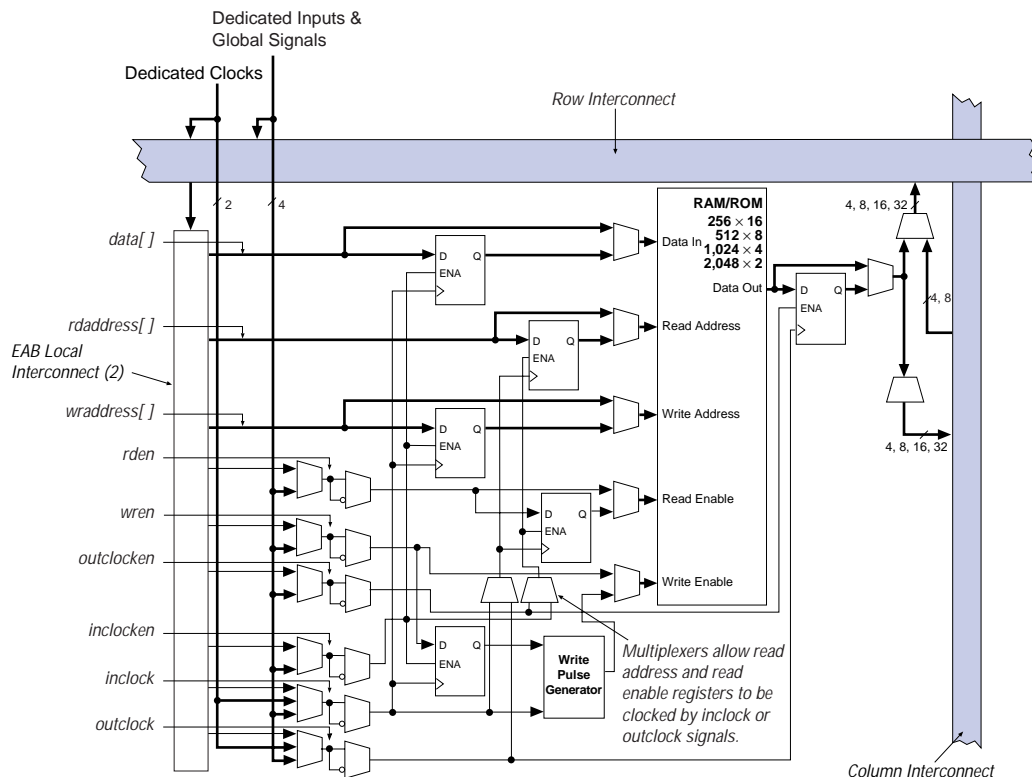
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input LUT, a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable logic gates.

Signal interconnections within ACEX 1K devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.1 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 2.5 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

**Figure 1** shows a block diagram of the ACEX 1K device architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 2. ACEX 1K Device in Dual-Port RAM Mode *Note (1)*



**Notes:**

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

The EAB can use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3. The ACEX 1K EAB can also be used in a single-port mode (see Figure 4).

Figure 3. ACEX 1K EAB in Dual-Port RAM Mode

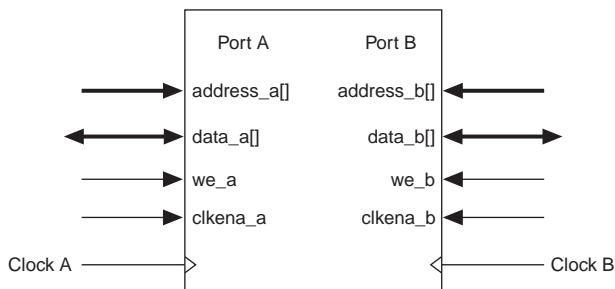
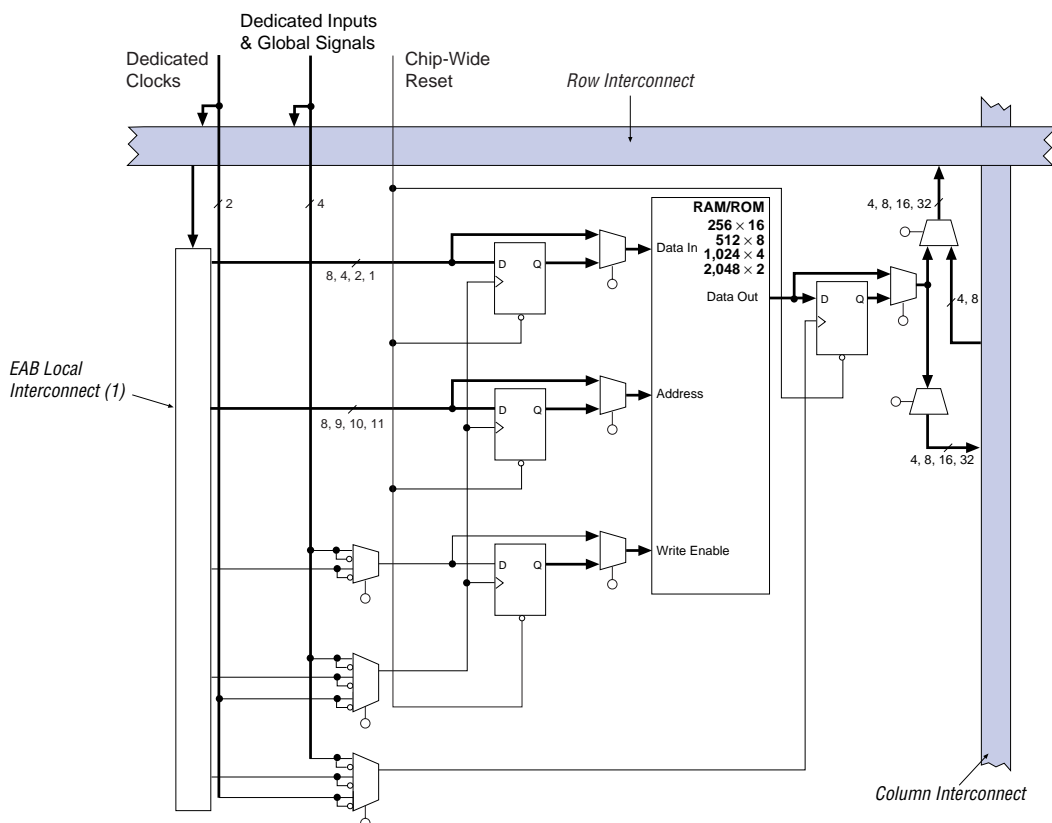


Figure 4. ACEX 1K Device in Single-Port RAM Mode



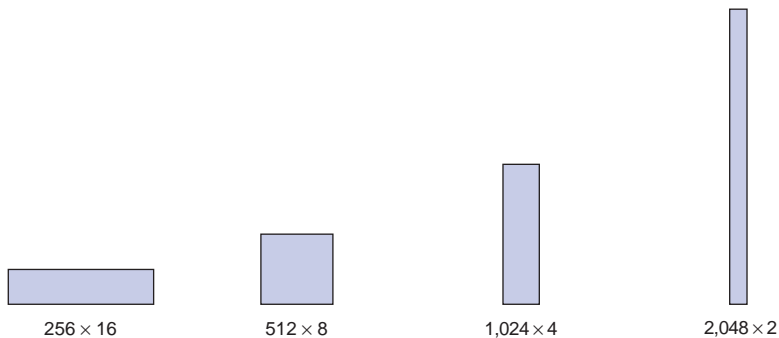
**Note:**

- (1) EP1K10, EP1K30, and EP1K50 devices have 88 EAB local interconnect channels; EP1K100 devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

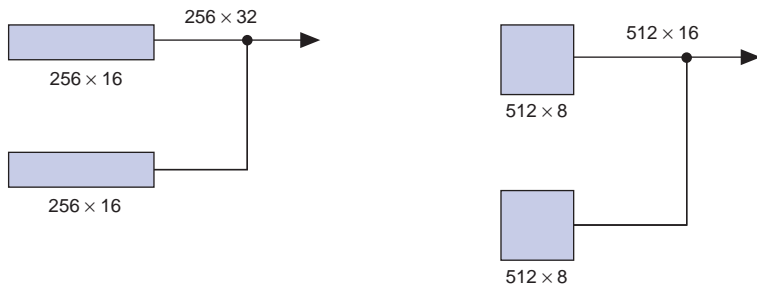
When used as RAM, each EAB can be configured in any of the following sizes:  $256 \times 16$ ;  $512 \times 8$ ;  $1,024 \times 4$ ; or  $2,048 \times 2$ . Figure 5 shows the ACEX 1K EAB memory configurations.

Figure 5. ACEX 1K EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two  $256 \times 16$  RAM blocks can be combined to form a  $256 \times 32$  block, and two  $512 \times 8$  RAM blocks can be combined to form a  $512 \times 16$  block. Figure 6 shows examples of multiple EAB combination.

Figure 6. Examples of Combining ACEX 1K EABs



### *LE Operating Modes*

The ACEX 1K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 11 shows the ACEX 1K LE operating modes.



### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but it supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

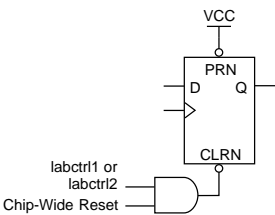
The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

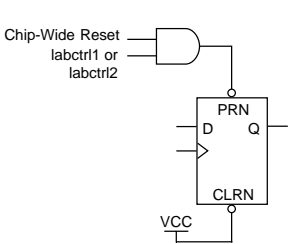
In addition to the six clear and preset modes, ACEX 1K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. ACEX 1K LE Clear & Preset Modes

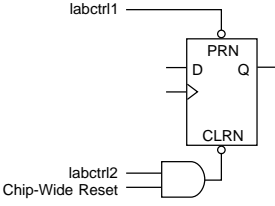
Asynchronous Clear



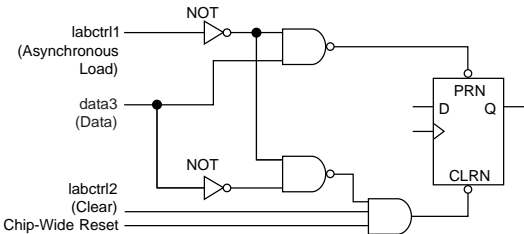
Asynchronous Preset



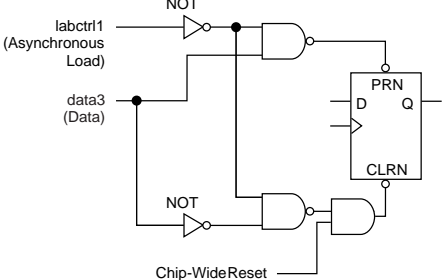
Asynchronous Preset & Clear



Asynchronous Load with Clear



Asynchronous Load without Clear or Preset



Asynchronous Load with Preset

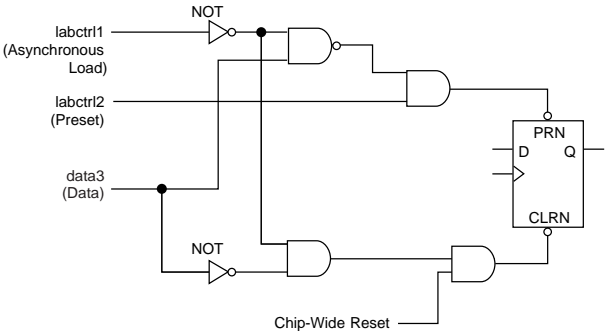
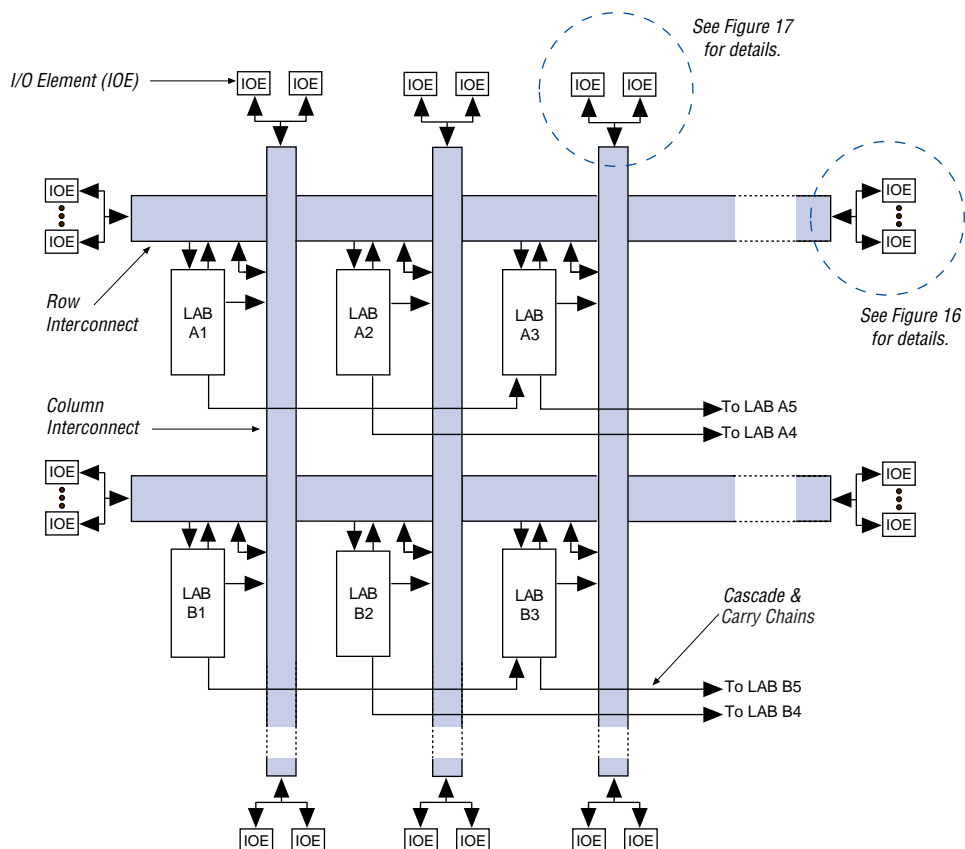


Figure 14. ACEX 1K Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. For bidirectional registered I/O implementation, the output register should be in the IOE and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. Figure 15 shows the bidirectional I/O registers.

On all ACEX 1K devices, the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock-enable or eight output-enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock, and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on an LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

The  $V_{CCINT}$  pins must always be connected to a 2.5-V power supply. With a 2.5-V  $V_{CCINT}$  level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The  $V_{CCIO}$  pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels higher than 3.0 V achieve a faster timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

**Table 13** summarizes ACEX 1K MultiVolt I/O support.

<i>Table 13. ACEX 1K MultiVolt I/O Support</i>						
$V_{CCIO}$ (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

**Notes:**

- (1) The PCI clamping diode must be disabled on an input which is driven with a voltage higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 3.3$  V, an ACEX 1K device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on ACEX 1K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a higher  $V_{IH}$  than LVTTL. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting the CMOS  $V_{OH}$  requirement. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Power Sequencing & Hot-Socketing

Because ACEX 1K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

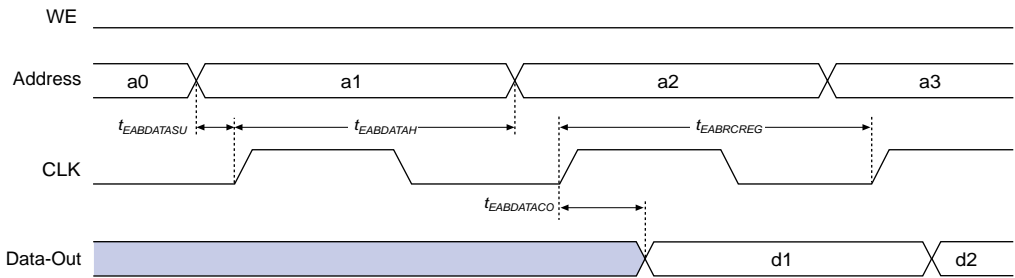
Signals can be driven into ACEX 1K devices before and during power up without damaging the device. Additionally, ACEX 1K devices do not drive out during power up. Once operating conditions are reached, ACEX 1K devices operate as specified by the user.

Table 20. ACEX 1K Device DC Operating Conditions (Part 2 of 2) Notes (6), (7)

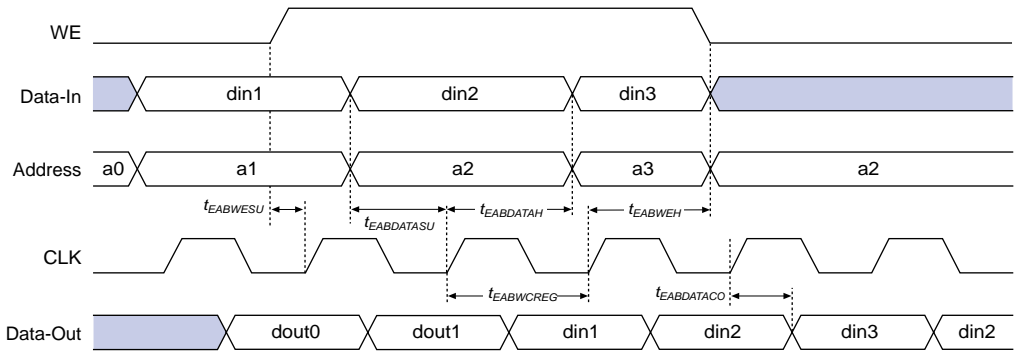
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 12 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (10)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (10)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (10)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 2.375 \text{ V}$ (10)			0.2	V
		$I_{OL} = 1 \text{ mA DC}$ , $V_{CCIO} = 2.375 \text{ V}$ (10)			0.4	V
		$I_{OL} = 2 \text{ mA DC}$ , $V_{CCIO} = 2.375 \text{ V}$ (10)			0.7	V
$I_I$	Input pin leakage current	$V_I = 5.3 \text{ to } -0.3 \text{ V}$ (11)	-10		10	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = 5.3 \text{ to } -0.3 \text{ V}$ (11)	-10		10	$\mu\text{A}$
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I = \text{ground}$ , no load, no toggling inputs		5		$\text{mA}$
		$V_I = \text{ground}$ , no load, no toggling inputs (12)		10		$\text{mA}$
$R_{CONF}$	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0 \text{ V}$ (13)	20		50	$\text{k}\Omega$
		$V_{CCIO} = 2.375 \text{ V}$ (13)	30		80	$\text{k}\Omega$

Figure 30. EAB Synchronous Timing Waveforms

EAB Synchronous Read



EAB Synchronous Write (EAB Output Registers Used)



Tables 22 through 26 describe the ACEX 1K device internal timing parameters.

Table 22. LE Timing Microparameters (Part 1 of 2) <span>Note (1)</span>		
Symbol	Parameter	Conditions
$t_{LUT}$	LUT delay for data-in	
$t_{CLUT}$	LUT delay for carry-in	
$t_{RLUT}$	LUT delay for LE register feedback	
$t_{PACKED}$	Data-in to packed register delay	
$t_{EN}$	LE register enable delay	
$t_{CICO}$	Carry-in to carry-out delay	
$t_{CGEN}$	Data-in to carry-out delay	
$t_{CGENR}$	LE register feedback to carry-out delay	

Tables 27 through 29 describe the ACEX 1K external timing parameters and their symbols.

Table 27. External Reference Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{\text{DRR}}$	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	(2)

Table 28. External Timing Parameters

Symbol	Parameter	Conditions
$t_{\text{INSU}}$	Setup time with global clock at IOE register	(3)
$t_{\text{INH}}$	Hold time with global clock at IOE register	(3)
$t_{\text{OUTCO}}$	Clock-to-output delay with global clock at IOE register	(3)
$t_{\text{PCISU}}$	Setup time with global clock for registers used in PCI designs	(3), (4)
$t_{\text{PCIH}}$	Hold time with global clock for registers used in PCI designs	(3), (4)
$t_{\text{PCICO}}$	Clock-to-output delay with global clock for registers used in PCI designs	(3), (4)

Table 29. External Bidirectional Timing Parameters *Note (3)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{INHBIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	CI = 35 pF
$t_{\text{XZBIDIR}}$	Synchronous IOE output buffer disable delay	CI = 35 pF
$t_{\text{ZXBIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate = off	CI = 35 pF

**Notes to tables:**

- (1) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
- (2) Contact Altera Applications for test circuit specifications and test conditions.
- (3) These timing parameters are sample-tested only.
- (4) This parameter is measured with the measurement and test conditions, including load, specified in the *PCI Local Bus Specification, Revision 2.2*.



Table 31. EP1K10 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		2.6		3.1		4.0	ns
$t_{IOC}$		0.3		0.4		0.5	ns
$t_{IOCO}$		0.9		1.0		1.4	ns
$t_{IOCOMB}$		0.0		0.0		0.0	ns
$t_{IOSU}$	1.3		1.5		2.0		ns
$t_{IOH}$	0.9		1.0		1.4		ns
$t_{IOCLR}$		1.1		1.3		1.7	ns
$t_{OD1}$		3.1		3.7		4.1	ns
$t_{OD2}$		2.6		3.3		3.9	ns
$t_{OD3}$		5.8		6.9		8.3	ns
$t_{XZ}$		3.8		4.5		5.9	ns
$t_{ZX1}$		3.8		4.5		5.9	ns
$t_{ZX2}$		3.3		4.1		5.7	ns
$t_{ZX3}$		6.5		7.7		10.1	ns
$t_{INREG}$		3.7		4.3		5.7	ns
$t_{IOFD}$		0.9		1.0		1.4	ns
$t_{INCOMB}$		1.9		2.3		3.0	ns

Table 43. EP1K30 External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (3)	2.8		3.9		5.2		ns
t <sub>INHBIDIR</sub> (3)	0.0		0.0		0.0		ns
t <sub>INSUBIDIR</sub> (4)	3.8		4.9		–		ns
t <sub>INHBIDIR</sub> (4)	0.0		0.0		–		ns
t <sub>OUTCOBIDIR</sub> (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t <sub>XZBIDIR</sub> (3)		6.1		7.5		9.7	ns
t <sub>ZXBIDIR</sub> (3)		6.1		7.5		9.7	ns
t <sub>OUTCOBIDIR</sub> (4)	0.5	3.9	0.5	4.9	–	–	ns
t <sub>XZBIDIR</sub> (4)		5.1		6.5		–	ns
t <sub>ZXBIDIR</sub> (4)		5.1		6.5		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 22 through 29 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 44 through 50 show EP1K50 device external timing parameters.

Table 44. EP1K50 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.6		0.8		1.1	ns
$t_{CLUT}$		0.5		0.6		0.8	ns
$t_{RLUT}$		0.6		0.7		0.9	ns
$t_{PACKED}$		0.2		0.3		0.4	ns
$t_{EN}$		0.6		0.7		0.9	ns
$t_{CICO}$		0.1		0.1		0.1	ns
$t_{CGEN}$		0.4		0.5		0.6	ns
$t_{CGENR}$		0.1		0.1		0.1	ns
$t_{CASC}$		0.5		0.8		1.0	ns
$t_C$		0.5		0.6		0.8	ns

Table 48. EP1K50 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
$t_{DIN2LE}$		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

Table 49. EP1K50 External Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>DDR</sub>		8.0		9.5		12.5	ns
t <sub>INSU</sub> (2)	2.4		2.9		3.9		ns
t <sub>INH</sub> (2)	0.0		0.0		0.0		ns
t <sub>OUTCO</sub> (2)	2.0	4.3	2.0	5.2	2.0	7.3	ns
t <sub>INSU</sub> (3)	2.4		2.9		–		ns
t <sub>INH</sub> (3)	0.0		0.0		–		ns
t <sub>OUTCO</sub> (3)	0.5	3.3	0.5	4.1	–	–	ns
t <sub>PCISU</sub>	2.4		2.9		–		ns
t <sub>PCIH</sub>	0.0		0.0		–		ns
t <sub>PCICO</sub>	2.0	6.0	2.0	7.7	–	–	ns

The  $I_{CCACTIVE}$  value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} (\mu A)$$

Where:

- $f_{MAX}$  = Maximum operating frequency in MHz
- $N$  = Total number of LEs used in the device
- $\text{tog}_{LC}$  = Average percent of LEs toggling at each clock (typically 12.5%)
- $K$  = Constant

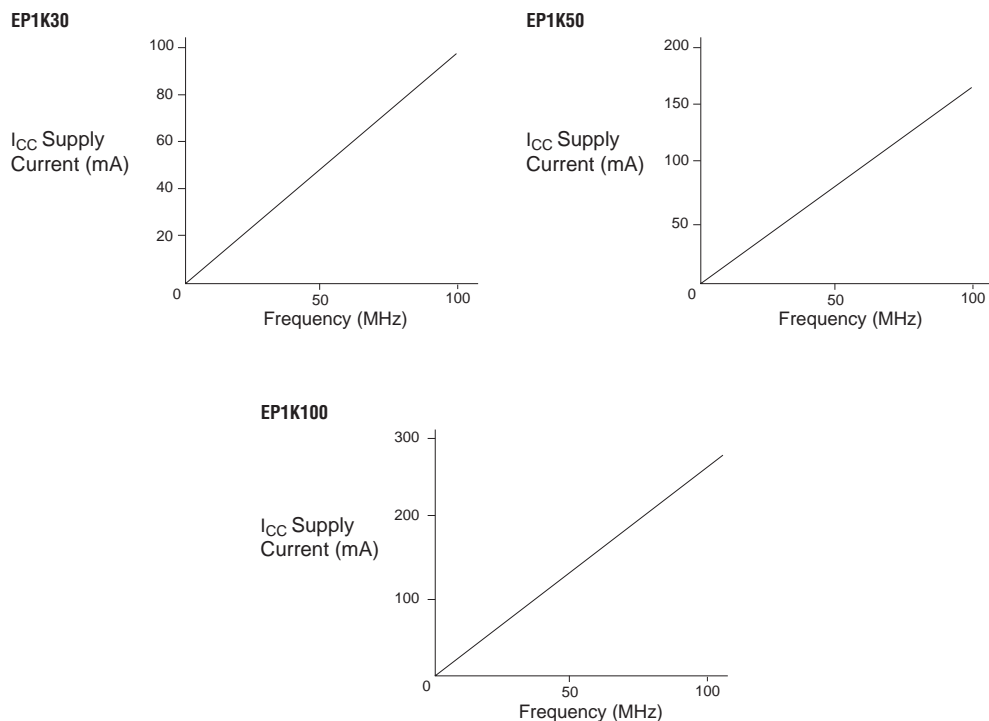
Table 58 provides the constant (K) values for ACEX 1K devices.

Table 58. ACEX 1K Constant Values	
Device	K Value
EP1K10	4.5
EP1K30	4.5
EP1K50	4.5
EP1K100	4.5

This supply power calculation provides an  $I_{CC}$  estimate based on typical conditions with no output load. The actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect ACEX 1K devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of ACEX 1K devices. For information on other ACEX 1K devices, contact Altera Applications at (800) 800-EPLD.

Figure 31. ACEX 1K  $I_{CCACTIVE}$  vs. Operating Frequency

## Configuration & Operation

The ACEX 1K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The ACEX 1K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as  $V_{CC}$  rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The ACEX 1K POR time does not exceed 50  $\mu$ s.



When configuring with a configuration device, refer to the relevant configuration device data sheet for POR timing information.