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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

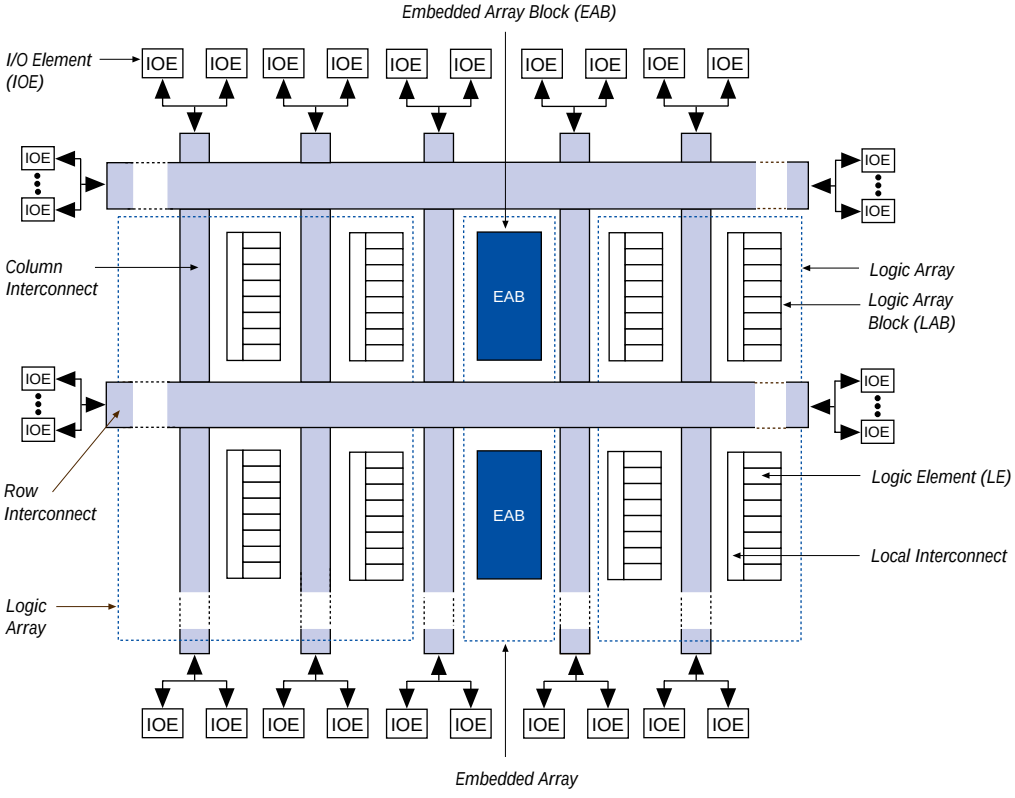
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 40960 |
| Number of I/O | 147 |
| Number of Gates | 199000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1k50qi208-2n |

***Figure 1. ACEX 1K Device Block Diagram***

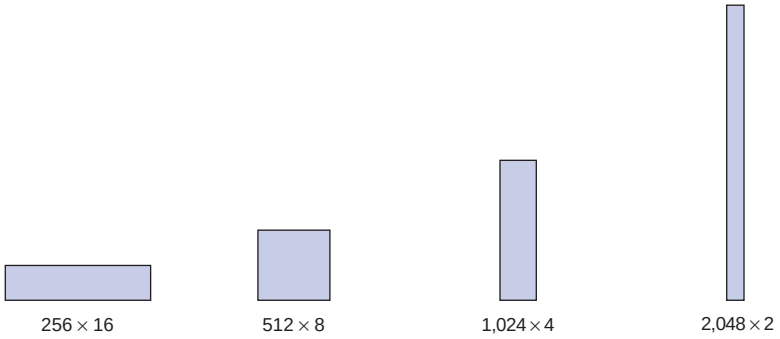



ACEX 1K devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.0 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16; 512 × 8; 1,024 × 4; or 2,048 × 2. Figure 5 shows the ACEX 1K EAB memory configurations.

*Figure 5. ACEX 1K EAB Memory Configurations*




Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 block. Figure 6 shows examples of multiple EAB combination.

*Figure 6. Examples of Combining ACEX 1K EABs*

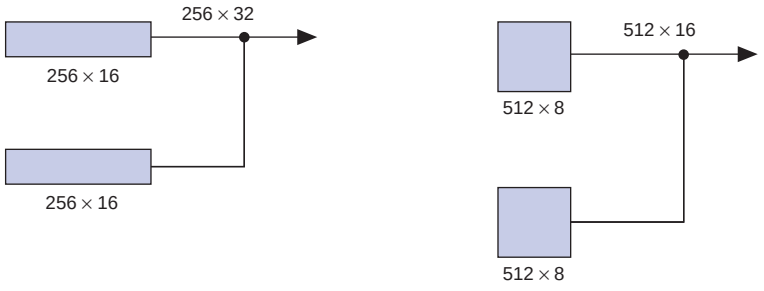
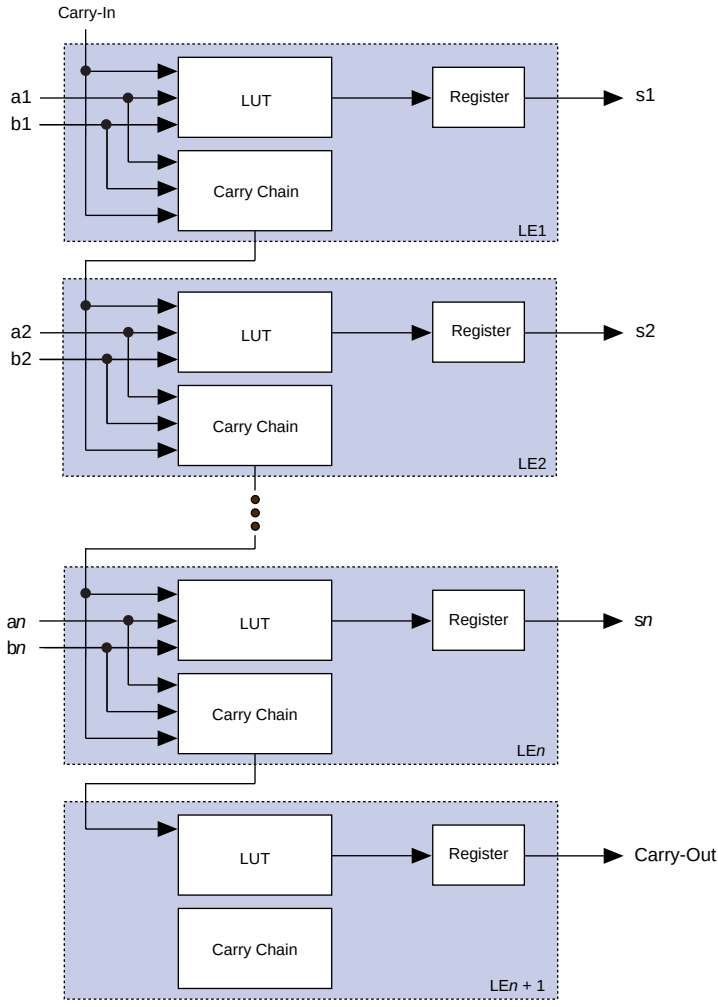


*Figure 9. ACEX 1K Carry Chain Operation (n-Bit Full Adder)*



### Clearable Counter Mode

The clearable counter mode is similar to the up / down counter mode, but it supports a synchronous clear instead of the up / down control. The clear function is substituted for the cascade-in signal in the up / down counter mode. Two 3-input LUTs are used; one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

#### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

#### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Table 7 lists the sources for each peripheral control signal and shows how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. Table 7 also shows the rows that can drive global signals.

*Table 7. Peripheral Bus Sources for ACEX Devices*

| Peripheral Control Signal | EP1K10 | EP1K30 | EP1K50 | EP1K100 |
|---|---|---|---|---|
| OE0 | Row A | Row A | Row A | Row A |
| OE1 | Row A | Row B | Row B | Row C |
| OE2 | Row B | Row C | Row D | Row E |
| OE3 | Row B | Row D | Row F | Row L |
| OE4 | Row C | Row E | Row H | Row I |
| OE5 | Row C | Row F | Row J | Row K |
| CLKENA0/CLK0/GLOBAL0 | Row A | Row A | Row A | Row F |
| CLKENA1/OE6/GLOBAL1 | Row A | Row B | Row C | Row D |
| CLKENA2/CLR0 | Row B | Row C | Row E | Row B |
| CLKENA3/OE7/GLOBAL2 | Row B | Row D | Row G | Row H |
| CLKENA4/CLR1 | Row C | Row E | Row I | Row J |
| CLKENA5/CLK1/GLOBAL3 | Row C | Row F | Row J | Row G |

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

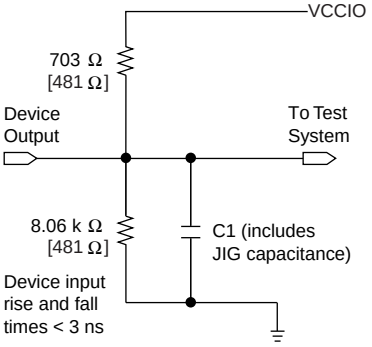
The chip-wide output enable pin is an active-high pin that can be used to tri-state all pins on the device. This option can be set in the Altera software. The built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

## Generic Testing

Each ACEX 1K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for ACEX 1K devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. ACEX 1K AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.*




## Operating Conditions

Tables 18 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V ACEX 1K devices.

***Table 18. ACEX 1K Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, and BGA packages, under bias | | 135 | ° C |

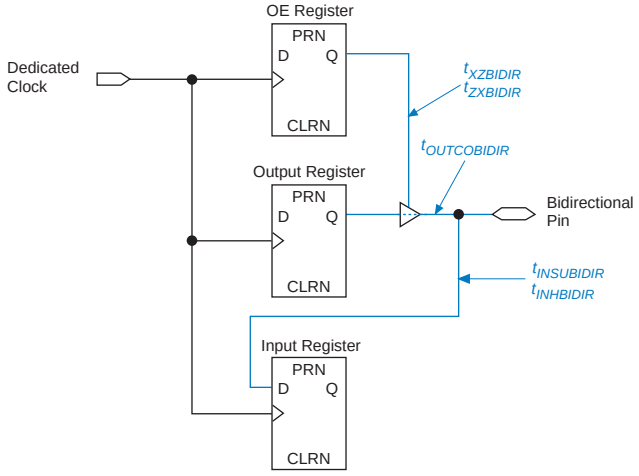
*Table 19. ACEX 1K Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(2)*, *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | Commercial range | 0 | 70 | ° C |
| | | Industrial range | –40 | 85 | ° C |
| $T_J$ | Junction temperature | Commercial range | 0 | 85 | ° C |
| | | Industrial range | –40 | 100 | ° C |
| | | Extended range | –40 | 125 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 20. ACEX 1K Device DC Operating Conditions (Part 1 of 2)* *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, $0.5 \times V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, $0.3 \times V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 ×†$V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.375 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.375 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.375 V *(9)* | 1.7 | | | V |

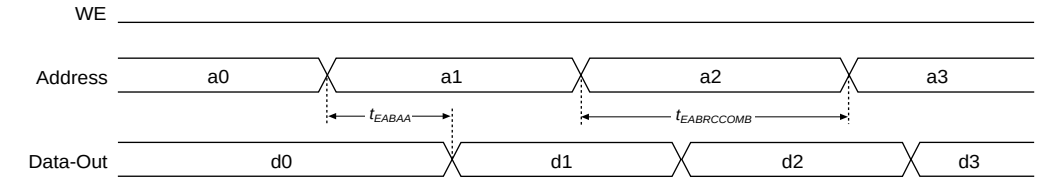
*Figure 28. Synchronous Bidirectional Pin External Timing Model*



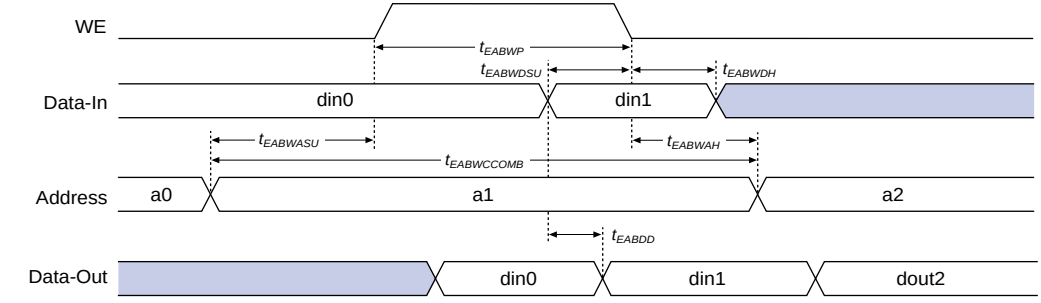

Tables 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 24.

*Figure 29. EAB Asynchronous Timing Waveforms*

**EAB Asynchronous Read**




**EAB Asynchronous Write**



Tables 27 through 29 describe the ACEX 1K external timing parameters and their symbols.

**Table 27. External Reference Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{DRR}$ | Register-to-register delay via four LEs, three row interconnects, and four local interconnects | *(2)* |

**Table 28. External Timing Parameters**

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time with global clock at IOE register | *(3)* |
| $t_{INH}$ | Hold time with global clock at IOE register | *(3)* |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register | *(3)* |
| $t_{PCISU}$ | Setup time with global clock for registers used in PCI designs | *(3)*, *(4)* |
| $t_{PCIH}$ | Hold time with global clock for registers used in PCI designs | *(3)*, *(4)* |
| $t_{PCICO}$ | Clock-to-output delay with global clock for registers used in PCI designs | *(3)*, *(4)* |

**Table 29. External Bidirectional Timing Parameters** *Note (3)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | CI = 35 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | CI = 35 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | CI = 35 pF |

***Notes to tables:***

(1) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(2) Contact Altera Applications for test circuit specifications and test conditions.
(3) These timing parameters are sample-tested only.
(4) This parameter is measured with the measurement and test conditions, including load, specified in the ***PCI Local Bus Specification, Revision 2.2.***

Tables 30 through 36 show EP1K10 device internal and external timing parameters.

**Table 30. EP1K10 Device LE Timing Microparameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.9 | | 1.0 | | 1.3 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.7 | | 0.9 | | 1.1 | ns |
| $t_{C}$ | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{H}$ | 0.9 | | 1.0 | | 1.1 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 2.5 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 2.5 | | ns |

| *Table 31. EP1K10 Device IOE Timing Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IOD}$ | | 2.6 | | 3.1 | | 4.0 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 1.3 | | 1.5 | | 2.0 | | ns |
| $t_{IOH}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{OD1}$ | | 3.1 | | 3.7 | | 4.1 | ns |
| $t_{OD2}$ | | 2.6 | | 3.3 | | 3.9 | ns |
| $t_{OD3}$ | | 5.8 | | 6.9 | | 8.3 | ns |
| $t_{XZ}$ | | 3.8 | | 4.5 | | 5.9 | ns |
| $t_{ZX1}$ | | 3.8 | | 4.5 | | 5.9 | ns |
| $t_{ZX2}$ | | 3.3 | | 4.1 | | 5.7 | ns |
| $t_{ZX3}$ | | 6.5 | | 7.7 | | 10.1 | ns |
| $t_{INREG}$ | | 3.7 | | 4.3 | | 5.7 | ns |
| $t_{IOFD}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INCOMB}$ | | 1.9 | | 2.3 | | 3.0 | ns |

| *Table 33. EP1K10 Device EAB Internal Timing Macroparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABAA}$ | | 6.7 | | 7.3 | | 7.3 | ns |
| $t_{EABRCCOMB}$ | 6.7 | | 7.3 | | 7.3 | | ns |
| $t_{EABRCREG}$ | 4.7 | | 4.9 | | 4.9 | | ns |
| $t_{EABWP}$ | 2.7 | | 2.8 | | 2.8 | | ns |
| $t_{EABWCCOMB}$ | 6.4 | | 6.7 | | 6.7 | | ns |
| $t_{EABWCREG}$ | 7.4 | | 7.6 | | 7.6 | | ns |
| $t_{EABDD}$ | | 6.0 | | 6.5 | | 6.5 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 0.9 | ns |
| $t_{EABDATASU}$ | 1.6 | | 1.7 | | 1.7 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.4 | | 1.4 | | 1.4 | | ns |
| $t_{EABWEH}$ | 0.1 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.6 | | 1.7 | | 1.7 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.1 | | 3.4 | | 3.4 | | ns |
| $t_{EABWAH}$ | 0.6 | | 0.5 | | 0.5 | | ns |
| $t_{EABWO}$ | | 5.4 | | 5.8 | | 5.8 | ns |

*Table 37. EP1K30 Device LE Timing Microparameters (Part 2 of 2)* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{COMB}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.6 | | ns |
| $t_{H}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{PRE}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CLR}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 2.5 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 2.5 | | ns |

*Table 38. EP1K30 Device IOE Timing Microparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 2.4 | | 2.8 | | 3.8 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 1.2 | | 1.4 | | 1.9 | | ns |
| $t_{IOH}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{OD1}$ | | 1.9 | | 2.3 | | 3.0 | ns |
| $t_{OD2}$ | | 1.4 | | 1.8 | | 2.5 | ns |
| $t_{OD3}$ | | 4.4 | | 5.2 | | 7.0 | ns |
| $t_{XZ}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX1}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX2}$ | | 2.2 | | 2.6 | | 3.8 | ns |
| $t_{ZX3}$ | | 5.2 | | 6.0 | | 8.3 | ns |
| $t_{INREG}$ | | 3.4 | | 4.1 | | 5.5 | ns |
| $t_{IOFD}$ | | 0.8 | | 1.3 | | 2.4 | ns |
| $t_{INCOMB}$ | | 0.8 | | 1.3 | | 2.4 | ns |

*Table 39. EP1K30 Device EAB Internal Microparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{EABDATA1}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.3 | | 1.4 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABSU}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{EABH}$ | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.3 | | ns |
| $t_{AA}$ | | 3.2 | | 3.8 | | 4.4 | ns |
| $t_{WP}$ | 2.5 | | 2.9 | | 3.3 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.2 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.0 | | 1.1 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.7 | | 2.0 | | 2.3 | | ns |
| $t_{WAH}$ | 1.8 | | 2.1 | | 2.4 | | ns |
| $t_{RASU}$ | 3.1 | | 3.7 | | 4.2 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.2 | | ns |
| $t_{WO}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{DD}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.3 | | ns |
| $t_{EABCL}$ | 2.5 | | 2.9 | | 3.3 | | ns |

*Table 46. EP1K50 Device EAB Internal Microparameters* *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA2}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.0 | | 1.4 | | 1.9 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0.0 | | 0.0 | | 0.0 | |
| $t_{EABRE2}$ | | 0.4 | | 0.6 | | 0.8 | |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABSU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABCLR}$ | 0.8 | | 1.1 | | 1.5 | | |
| $t_{AA}$ | | 2.0 | | 2.8 | | 3.8 | ns |
| $t_{WP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.4 | | 1.9 | | |
| $t_{WDSU}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.0 | | 1.4 | | 1.9 | | ns |
| $t_{WAH}$ | 1.5 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 1.5 | | 2.1 | | 2.8 | | |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | |
| $t_{WO}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{DD}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

**Table 48. EP1K50 Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.1 | | 3.7 | | 4.6 | ns |
| $t_{DIN2LE}$ | | 1.7 | | 2.1 | | 2.7 | ns |
| $t_{DIN2DATA}$ | | 2.7 | | 3.1 | | 5.1 | ns |
| $t_{DCLK2IOE}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{DCLK2LE}$ | | 1.7 | | 2.1 | | 2.7 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{SAMECOLUMN}$ | | 1.0 | | 1.3 | | 2.1 | ns |
| $t_{DIFFROW}$ | | 2.5 | | 3.0 | | 4.5 | ns |
| $t_{TWOROWS}$ | | 4.0 | | 4.7 | | 6.9 | ns |
| $t_{LEPERIPH}$ | | 2.6 | | 2.9 | | 3.4 | ns |
| $t_{LABCARRY}$ | | 0.1 | | 0.2 | | 0.2 | ns |
| $t_{LABCASC}$ | | 0.8 | | 1.0 | | 1.3 | ns |

**Table 49. EP1K50 External Timing Parameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | – | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | – | – | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

Tables 51 through 57 show EP1K100 device internal and external timing parameters.

**Table 51. EP1K100 Device LE Timing Microparameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 1.0 | | 1.5 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

**Table 55. EP1K100 Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.1 | | 3.6 | | 4.4 | ns |
| $t_{DIN2LE}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{DIN2DATA}$ | | 1.6 | | 1.8 | | 2.0 | ns |
| $t_{DCLK2IOE}$ | | 0.8 | | 1.1 | | 1.4 | ns |
| $t_{DCLK2LE}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.5 | | 2.5 | | 3.4 | ns |
| $t_{SAMECOLUMN}$ | | 0.4 | | 1.0 | | 1.6 | ns |
| $t_{DIFFROW}$ | | 1.9 | | 3.5 | | 5.0 | ns |
| $t_{TWOROWS}$ | | 3.4 | | 6.0 | | 8.4 | ns |
| $t_{LEPERIPH}$ | | 4.3 | | 5.4 | | 6.5 | ns |
| $t_{LABCARRY}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{LABCASC}$ | | 0.8 | | 1.0 | | 1.4 | ns |

**Table 56. EP1K100 External Timing Parameters** *Notes (1), (2)*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 9.0 | | 12.0 | | 16.0 | ns |
| $t_{INSU}$ *(3)* | 2.0 | | 2.5 | | 3.3 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 5.2 | 2.0 | 6.9 | 2.0 | 9.1 | ns |
| $t_{INSU}$ *(4)* | 2.0 | | 2.2 | | – | | ns |
| $t_{INH}$ *(4)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(4)* | 0.5 | 3.0 | 0.5 | 4.6 | – | – | ns |
| $t_{PCISU}$ | 3.0 | | 6.2 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 6.9 | – | – | ns |

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow ACEX 1K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, re-initializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 40 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an ACEX 1K device can be loaded with one of five configuration schemes (see Table 59), chosen on the basis of the target application. An EPC16, EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a ACEX 1K device, allowing automatic configuration on system power-up.

Multiple ACEX 1K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional APEX 20K, APEX 20KE, FLEX 10K, FLEX 10KA, FLEX 10KE, ACEX 1K, and FLEX 6000 devices can be configured in the same serial chain.

*Table 59. Data Sources for ACEX 1K Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC16, EPC2, EPC1, or EPC1441 configuration device |
| Passive serial (PS) | BitBlaster or ByteBlasterMV download cables, or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL File or JBC File |

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Documentation Library*** for pin-out information.

## Revision History

The information contained in the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4 supersedes information published in previous versions.

The following changes were made to the *ACEX 1K Programmable Logic Device Family Data Sheet* version 3.4: added extended temperature support.