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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051c6t6

2 Description

The access line ultra-low-power STM32L051x6/8 microcontrollers incorporate the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L051x6/8 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L051x6/8 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L051x6/8 devices embed standard and advanced communication interfaces: up to two I2C, two SPIs, one I2S, two USARTs, a low-power UART (LPUART), .

The STM32L051x6/8 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L051x6/8 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance

3.14 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.15 Timers and watchdogs

The ultra-low-power STM32L051x6/8 devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

[Table 9](#) compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L051x6/8 devices (see [Table 9](#) for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The two USART interfaces (USART1, USART2) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. They also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

[Table 12](#) for the supported modes and features of USART interfaces.

Table 12. USART implementation

USART modes/features ⁽¹⁾	USART1 and USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode ⁽²⁾	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Table 15. STM32L051x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	TFBGA64	LQFP48	WLCSP36 ⁽¹⁾	LQFP32	UFQFPN32						
5	C1	5	-	-	-	PH0-OSC_IN (PH0)	I/O	TC	-	-	OSC_IN
6	D1	6	-	-	-	PH1- OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
7	E1	7	C6	4	4	NRST	I/O	RST	-	-	-
8	E3	-	-	-	-	PC0	I/O	FT	-	LPTIM1_IN1, EVENTOUT	ADC_IN10
9	E2	-	-	-	-	PC1	I/O	FT	-	LPTIM1_OUT, EVENTOUT	ADC_IN11
10	F2	-	-	-	-	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO/I2S2_M CK	ADC_IN12
11	-	-	-	-	-	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD	ADC_IN13
12	F1	8	-	-	-	VSSA	S		-	-	-
-	G1	-	E6	-	-	VREF+	S		-	-	-
13	H1	9	D5	5	5	VDDA	S		-	-	-
14	G2	10	D4	6	6	PA0	I/O	TC	-	TIM2_CH1, USART2_CTS, TIM2_ETR, COMP1_OUT	COMP1_INM6, ADC_IN0, RTC_TAMP2/WKU P1
15	H2	11	F6	7	7	PA1	I/O	FT	-	EVENTOUT, TIM2_CH2, USART2_RTS_DE, TIM21_ETR	COMP1_INP, ADC_IN1
16	F3	12	E5	8	8	PA2	I/O	FT	-	TIM21_CH1, TIM2_CH3, USART2_TX, COMP2_OUT	COMP2_INM6, ADC_IN2
17	G3	13	F5	9	9	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX	COMP2_INP, ADC_IN3
18	C2	-	-	-	-	VSS	S		-	-	-



Table 16. Alternate function port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/TIM21/SYS_A F/EVENTOUT/	-	TIM2/ EVENTOUT/	EVENTOUT	USART1/2/3	TIM2/21/22	EVENTOUT	COMP1/2
Port A	PA0	-	-	TIM2_CH1	-	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	-	TIM2_CH2	-	USART2_RTS_ DE	TIM21_ETR	-	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	-	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	-	-
	PA4	SPI1_NSS	-	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR	-	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	-	-	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	-	-	-	-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	-	EVENTOUT	USART1_CK	-	-	-
	PA9	MCO	-	-	-	USART1_TX	-	-	-
	PA10	-	-	-	-	USART1_RX	-	-	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART1_RTS_ DE	-	-	COMP2_OUT
	PA13	SWDIO	-	-	-	-	-	-	-
	PA14	SWCLK	-	-	-	USART2_TX	-	-	-
	PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 20: Voltage characteristics](#), [Table 21: Current characteristics](#), and [Table 22: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 20. Voltage characteristics

Symbol	Definition	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DDIO2} , V_{DD}) ⁽¹⁾	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TC pins	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0	V_{SS}	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DD} $	Variations between different V_{DDx} power pins	-	50	mV
$ V_{DDA}-V_{DDx} $	Variations between any V_{DDx} and V_{DDA} power pins ⁽³⁾	-	300	
$ \Delta V_{SS} $	Variations between all different ground pins	-	50	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.11		

1. All main power (V_{DD} , V_{DDIO2} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 21](#) for maximum allowed injected current values.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation. V_{DDIO2} is independent from V_{DD} and V_{DDA} : its value does not need to respect this rule.

Table 31. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	43.5	90	µA
				2 MHz	72	120	
				4 MHz	130	180	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	160	210	
				8 MHz	305	370	
				16 MHz	590	710	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	370	430	
				16 MHz	715	860	
				32 MHz	1650	1900	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	18	65	
				524 kHz	31.5	75	
				4.2 MHz	140	210	
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	665	830	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1750	2100	
	Supply current in Sleep mode, Flash ON	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	57.5	130	
				2 MHz	84	170	
				4 MHz	150	280	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	170	310	
				8 MHz	315	420	
				16 MHz	605	770	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	380	460	
				16 MHz	730	950	
				32 MHz	1650	2400	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	29.5	110	
				524 kHz	44.5	130	
				4.2 MHz	150	270	
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	680	950	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1750	2100	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked OFF
 - with only one peripheral clocked on

Table 37. Peripheral current consumption in Run or Sleep mode⁽¹⁾

Peripheral		Typical consumption, $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ °C}$				Unit
		Range 1, $V_{CORE}=1.8\text{ V}$ $VOS[1:0] = 01$	Range 2, $V_{CORE}=1.5\text{ V}$ $VOS[1:0] = 10$	Range 3, $V_{CORE}=1.2\text{ V}$ $VOS[1:0] = 11$	Low-power sleep and run	
APB1	I2C1	11	9.5	7.5	9	$\mu\text{A/MHz}$ (f_{HCLK})
	I2C2	4	3.5	3	2.5	
	LPTIM1	10	8.5	6.5	8	
	LPUART1	8	6.5	5.5	6	
	SPI2	9	4.5	3.5	4	
	USART2	14.5	12	9.5	11	
	TIM2	10.5	8.5	7	9	
	TIM6	3.5	3	2.5	2	
	WWDG	3	2	2	2	
APB2	ADC1 ⁽²⁾	5.5	5	3.5	4	$\mu\text{A/MHz}$ (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	$\mu\text{A/MHz}$ (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
AHB	CRC	1.5	1	1	1	$\mu\text{A/MHz}$ (f_{HCLK})
	FLASH	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	DMA1	10	8	6.5	8.5	

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

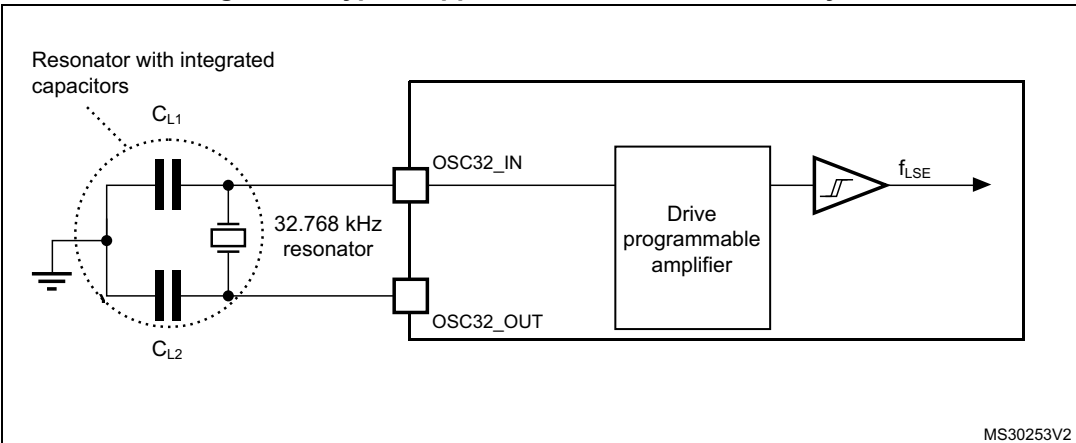
Table 43. LSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min ⁽²⁾	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$ ⁽³⁾	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in [Table 44](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 23](#).

High-speed internal 16 MHz (HSI16) RC oscillator

Table 44. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	$V_{DD} = 3.0 \text{ V}$	-	16	-	MHz
$\text{TRIM}^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$\text{ACC}_{\text{HSI16}}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	$V_{DDA} = 3.0 \text{ V}, T_A = 25^\circ\text{C}$	-1 ⁽³⁾	-	1 ⁽³⁾	%
		$V_{DDA} = 3.0 \text{ V}, T_A = 0 \text{ to } 55^\circ\text{C}$	-1.5	-	1.5	%
		$V_{DDA} = 3.0 \text{ V}, T_A = -10 \text{ to } 70^\circ\text{C}$	-2	-	2	%
		$V_{DDA} = 3.0 \text{ V}, T_A = -10 \text{ to } 85^\circ\text{C}$	-2.5	-	2	%
		$V_{DDA} = 3.0 \text{ V}, T_A = -10 \text{ to } 105^\circ\text{C}$	-4	-	2	%
		$V_{DDA} = 1.65 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ to } 125^\circ\text{C}$	-5.45	-	3.25	%
$t_{\text{SU(HSI16)}}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	μs
$I_{\text{DD(HSI16)}}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	μA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 23. HSI16 minimum and maximum value versus temperature

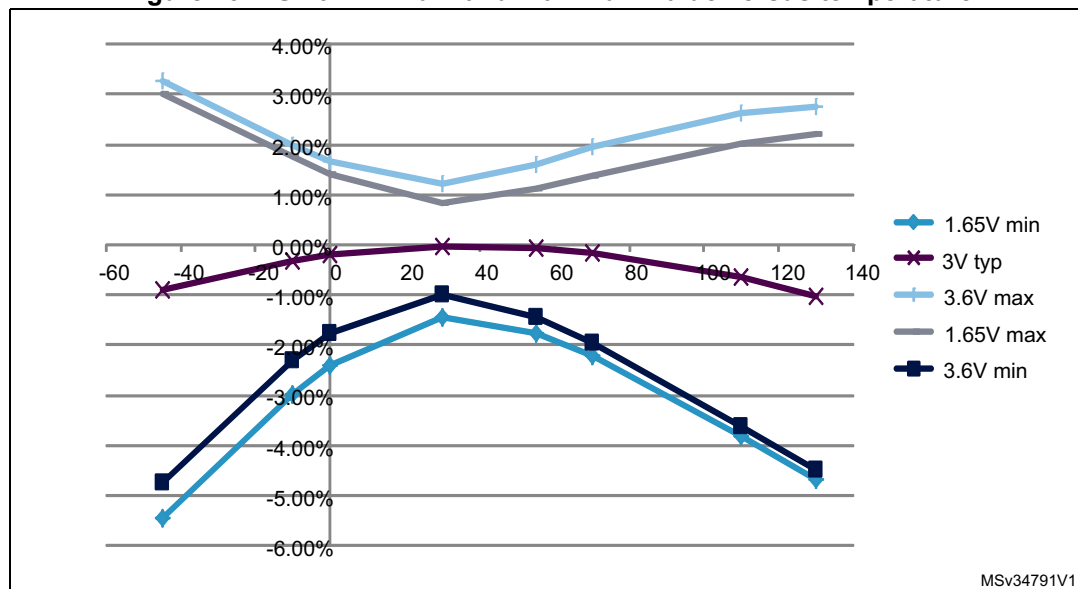
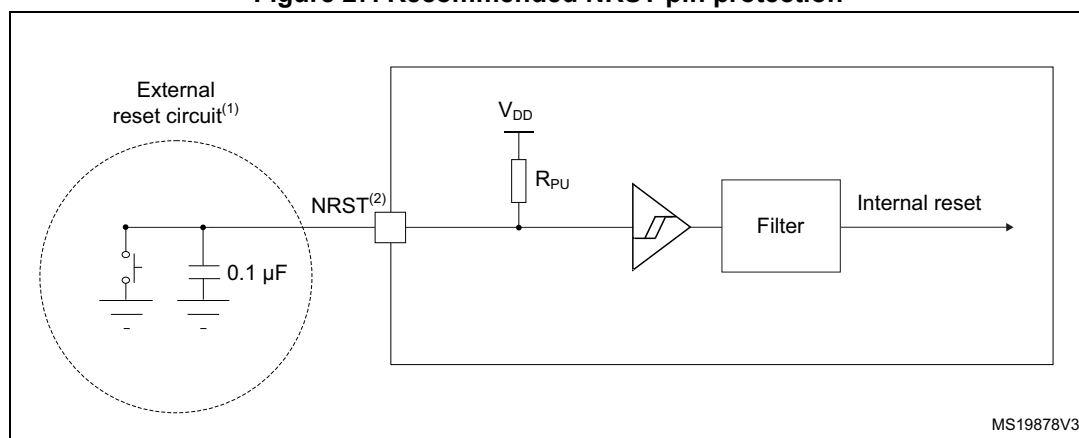


Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 59](#). Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 60](#) are derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 23: General operating conditions](#).

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	Fast channel	1.65	-	3.6	V
		Standard channel	1.75 ⁽¹⁾	-	3.6	
V_{REF+}	Positive reference voltage	-	1.65		V_{DDA}	V
I_{DDA} (ADC)	Current consumption of the ADC on V_{DDA} and V_{REF+}	1.14 Msps	-	200	-	μA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD} ⁽²⁾	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S ⁽³⁾	Sampling rate	12-bit resolution	0.01	-	1.14	MHz
f_{TRIG} ⁽³⁾	External trigger frequency	$f_{ADC} = 16$ MHz, 12-bit resolution	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V

Table 62. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$1.65\text{ V} < V_{\text{REF}+} < V_{\text{DDA}} < 3.6\text{ V}$, range 1/2/3	-	2	5	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	3	
ED	Differential linearity error		-	1	2	
ENOB	Effective number of bits		10.0	11.0	-	bits
SINAD	Signal-to-noise distortion		62	69	-	dB
SNR	Signal-to-noise ratio		61	69	-	
THD	Total harmonic distortion		-	-85	-65	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{\text{INJ(PIN)}}$ and $\Sigma I_{\text{INJ(PIN)}}$ in [Section 6.3.12](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 28. ADC accuracy characteristics

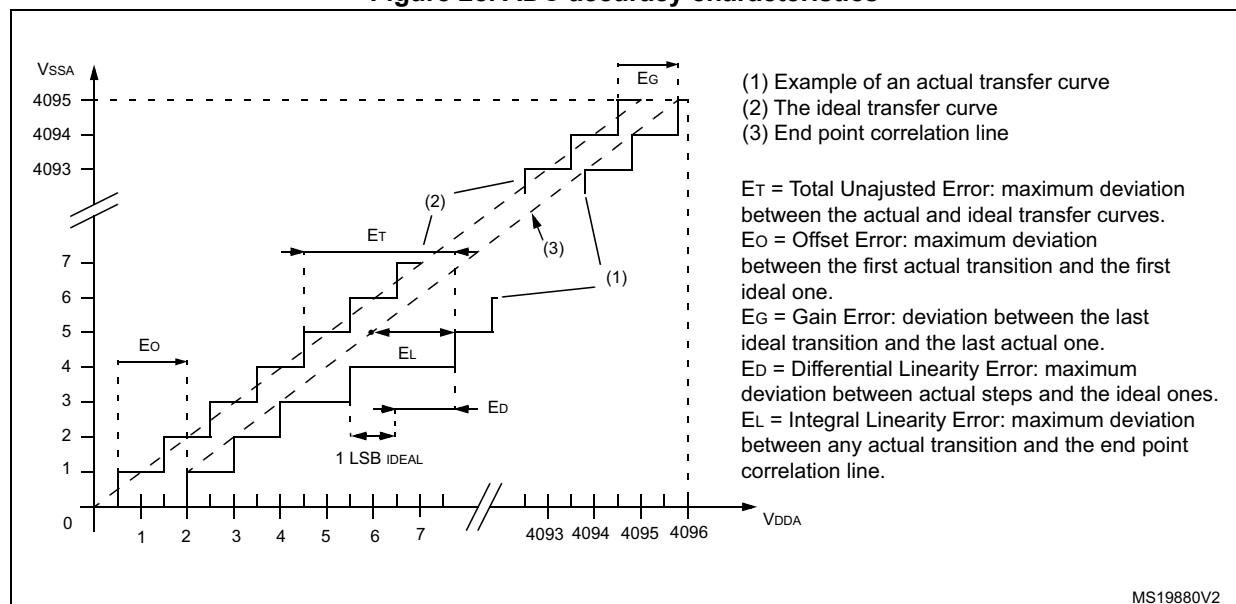
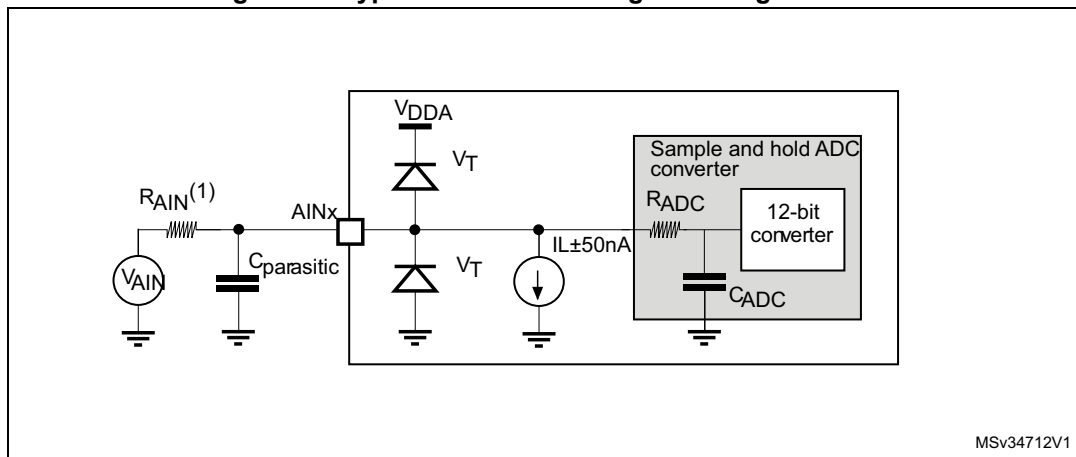


Figure 29. Typical connection diagram using the ADC



1. Refer to [Table 60: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 30](#) or [Figure 31](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

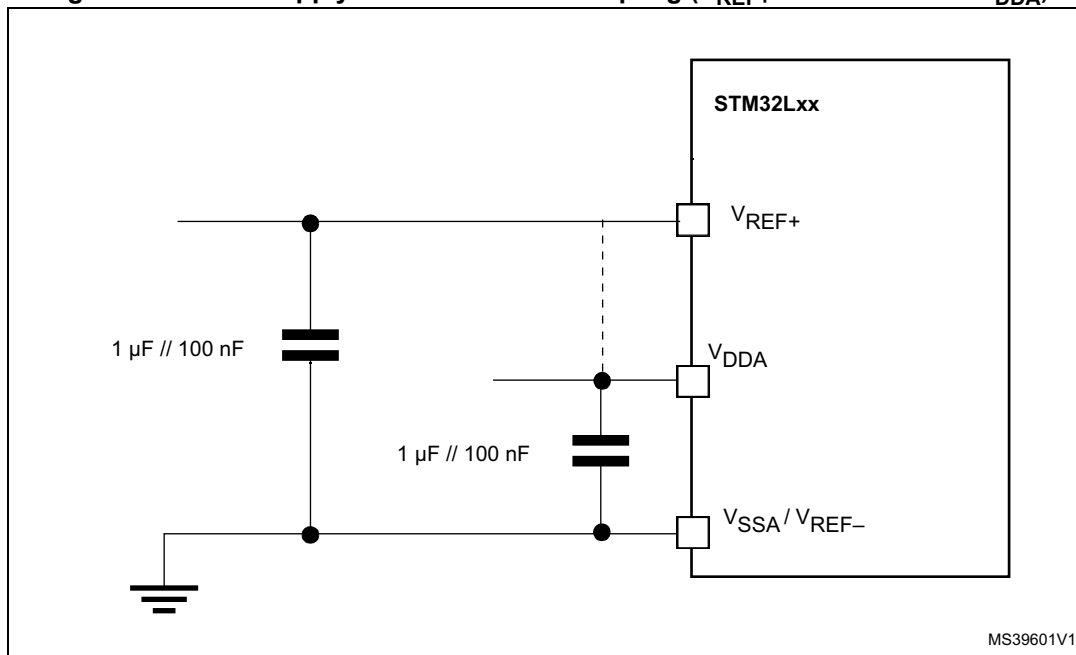
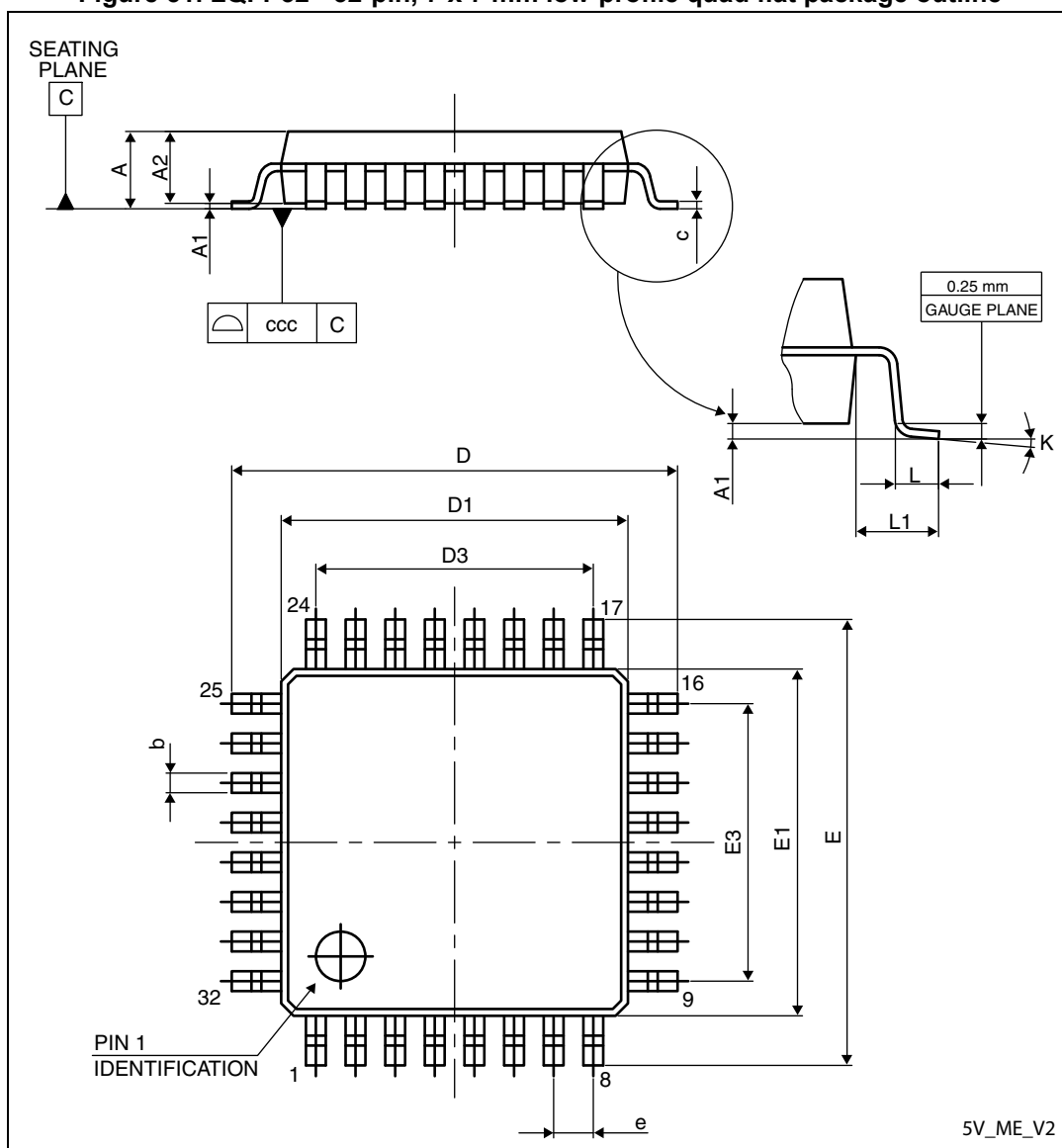
Figure 30. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

Table 81. WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

7.6 LQFP32 package information

Figure 51. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



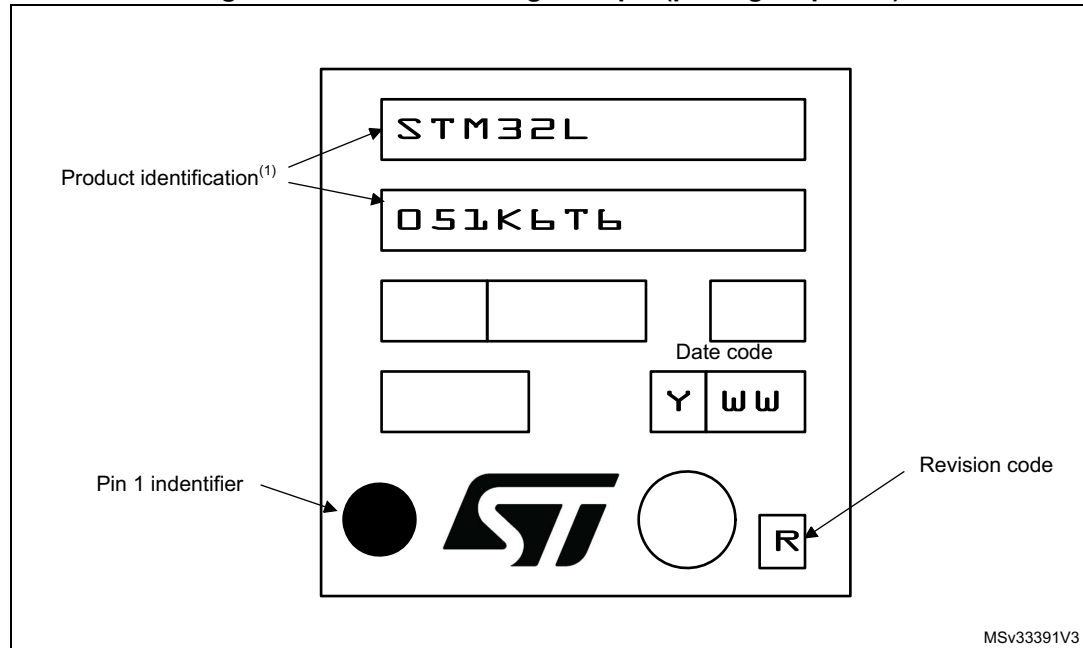
1. Drawing is not to scale.

Device marking for LQFP32

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 53. LQFP32 marking example (package top view)



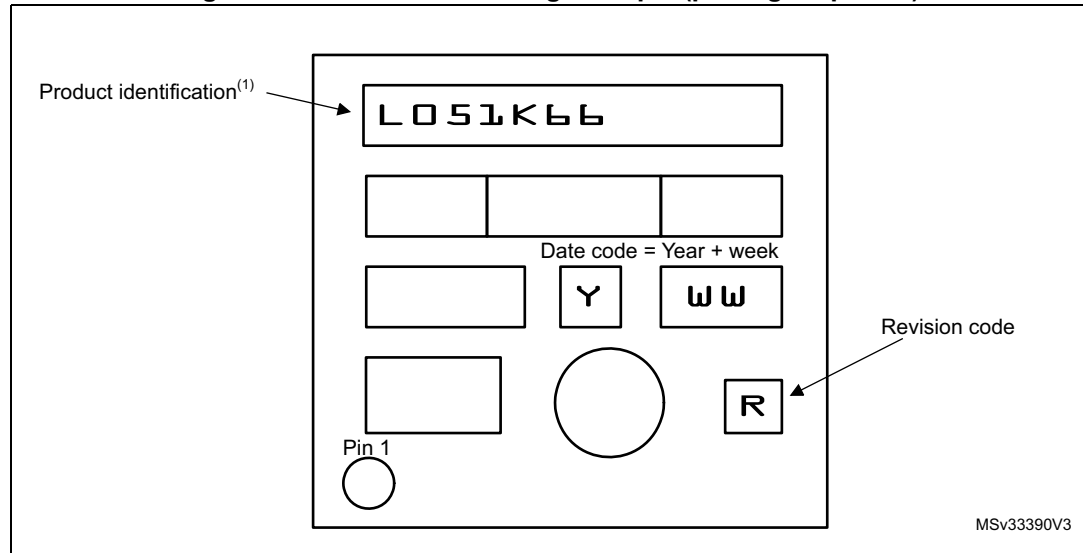
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for UFQFPN32

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 56. UFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 86. Document revision history (continued)

Date	Revision	Changes
08-Sep-2015	5	<p>Updated LQFP64, TFBGA64 and LQFP48 pinout/ballout schematics to highlight pin/ball supplied through VDDIO2.</p> <p>Updated current consumption in Run mode in Section : Features.</p> <p>Updated Figure 6: STM32L051x6/8 WLCSP36 ballout and Figure 4: STM32L051x6/8 TFBGA64 ballout - 5x 5 mm to change bump to top view. Renamed BOOT1 into nBOOT1. Changed USARTx_RTS into USARTx_RTS_DE and LPUARTx_RTS into LPUARTx_RTS_DE.</p> <p>Changed I/O structure to FT for PC15 in Table 15: STM32L051x6/8 pin definitions</p> <p>ADC no more available in Low-power run and Low-power Sleep modes in Table 5: Functionalities depending on the working mode (from Run/active down to standby).</p> <p>Updated Figure 7: STM32L051x6/8 LQFP32 pinout (PC14).</p> <p>Suppressed I2C2_SMBA alternate function for PB12 in Table 15: STM32L051x6/8 pin definitions and Table 17: Alternate function port B.</p> <p>In whole Section 6: Electrical characteristics, modified notes related to characteristics guaranteed by design and by tests during characterization.</p> <p>Added ΣI_{VDDIO2} and updated $\Sigma I_{IO(PIN)}$ in Table 21: Current characteristics. Updated Table 20: Voltage characteristics.</p> <p>Changed temperature condition in Table 8: Internal voltage reference measured values and Table 25: Embedded internal reference voltage calibration values.</p> <p>Updated TCoeff in Table 26: Embedded internal reference voltage.</p> <p>Updated Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS, Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive and Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF.</p> <p>Added note related to Standby mode in Table 38: Peripheral current consumption in Stop and Standby mode.</p> <p>Updated Table 39: Low-power mode wakeup timings</p> <p>Updated MSI oscillator temperature frequency drift in Table 46: MSI oscillator characteristics.</p> <p>Updated Table 55: I/O current injection susceptibility, Table 56: I/O static characteristics and Table 58: I/O AC characteristics.</p> <p>Section : I2C interface characteristics: updated introduction, Table 68: I2C analog filter characteristics.</p> <p>updated Figure 32: SPI timing diagram - slave mode and CPHA = 0.</p> <p>Updated Table 51: EMS characteristics and Table 52: EMI characteristics.</p> <p>Added t_{UP_LDO} in Table 60: ADC characteristics.</p> <p>Added Section : Device marking for LQFP64 and Section : Device marking for standard WLCSP36. Updated Section : Device marking for TFBGA64, Section : Device marking for LQFP48, Section : Device marking for LQFP32 and Section : Device marking for UFQFPN32.</p> <p>Updated note below marking schematics in Section 7: Package information. Added Figure 46: WLCSP36 - 2.596 x 2.868 mm, 0.4 mm pitch wafer level chip scale package outline.</p>

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