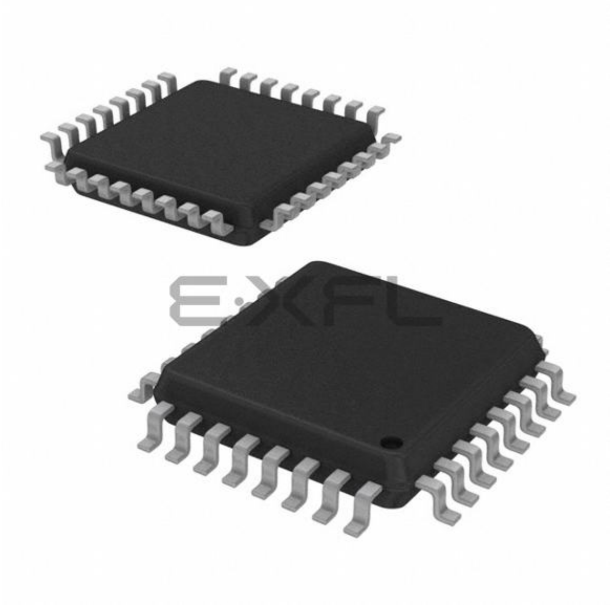
STMicroelectronics - STM32L051K6T6 Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051k6t6

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
“Y” = Yes (enable).
“O” = Optional can be enabled/disabled by software)
“-” = Not available
2. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
3. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
4. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-

Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L051x6/8 are compatible with all ARM tools and software.

Figure 2. Clock tree

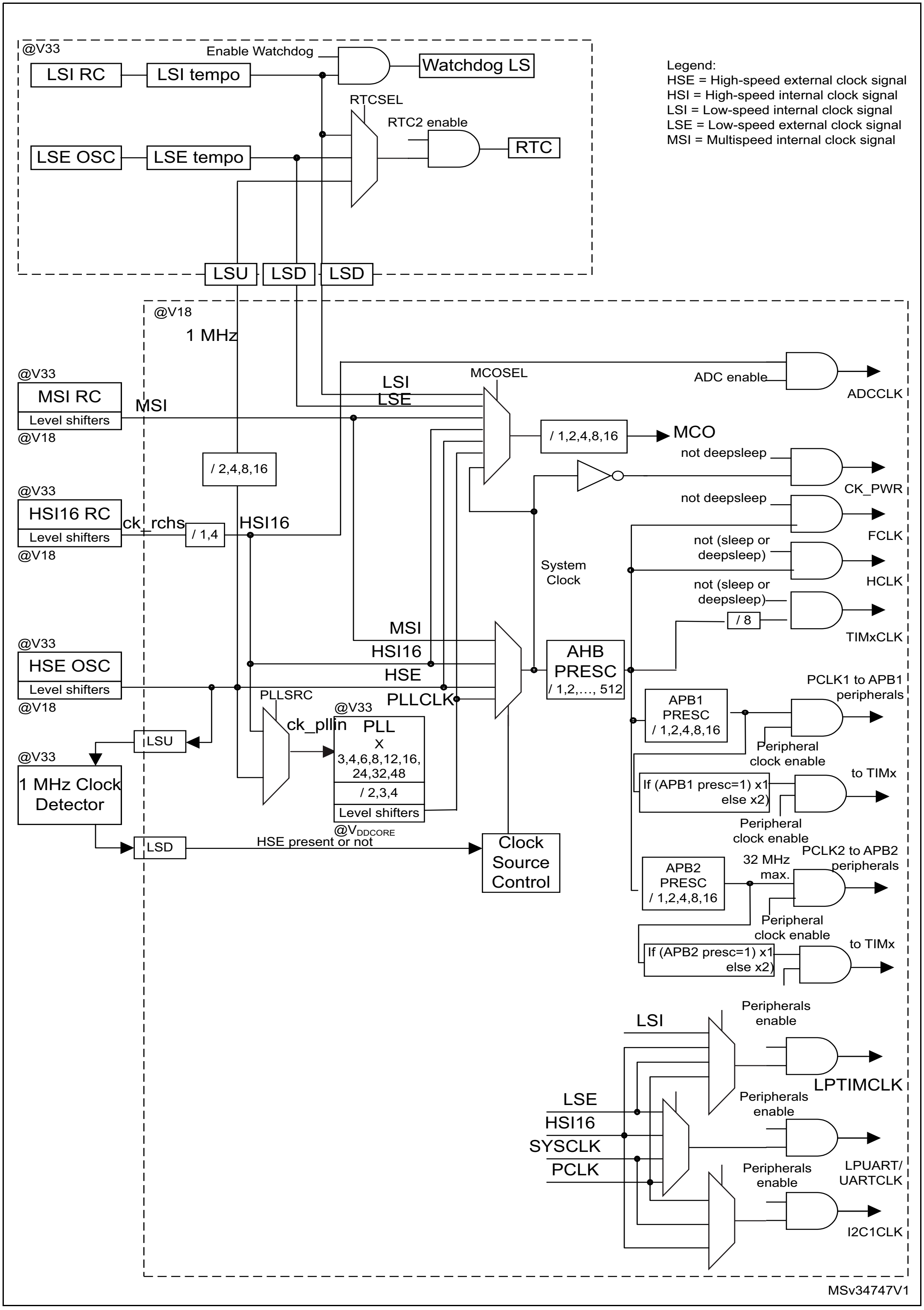


Table 18. Alternate function port C

Port		AF0	AF1	AF2
		LPUART1/LPTIM/TIM21/12/EVENTOUT	**-**	**SPI2/I2S2/LPUART1/EVENTOUT**
Port C	PC0	LPTIM1_IN1	-	EVENTOUT
	PC1	LPTIM1_OUT	-	EVENTOUT
	PC2	LPTIM1_IN2	-	SPI2_MISO/I2S2_MCK
	PC3	LPTIM1_ETR	-	SPI2_MOSI/I2S2_SD
	PC4	EVENTOUT	-	LPUART1_TX
	PC5		-	LPUART1_RX
	PC6	TIM22_CH1	-	-
	PC7	TIM22_CH2	-	-
	PC8	TIM22_ETR	-	-
	PC9	TIM21_ETR	-	-
	PC10	LPUART1_TX	-	-
	PC11	LPUART1_RX	-	-
	PC12	-	-	-
	PC13	-	-	-
	PC14	-	-	-
	PC15	-	-	-

Table 19. Alternate function port D

Port		AF0	AF1
		LPUART1	**-**
Port D	PD2	LPUART1_RTS_DE	-

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 23*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power-on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 46. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤ T_A ≤ 85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤ T_A ≤ 110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤ V_{DD} ≤ 3.6 V, T_A = 25 °C	-	-	2.5	%/V

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 52. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}			Unit
				8 MHz/ 4 MHz	8 MHz/ 16 MHz	8 MHz/ 32 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, compliant with IEC 61967-2	0.1 to 30 MHz	-21	-15	-12	dBµV
			30 to 130 MHz	-14	-12	-1	
			130 MHz to 1GHz	-10	-11	-7	
			EMI Level	1	1	1	-

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 55*.

Table 55. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA4, PA5, PA11, PA12, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT, FTf pins	-5 (1)	NA	
	Injected current on any other pins	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Output voltage levels

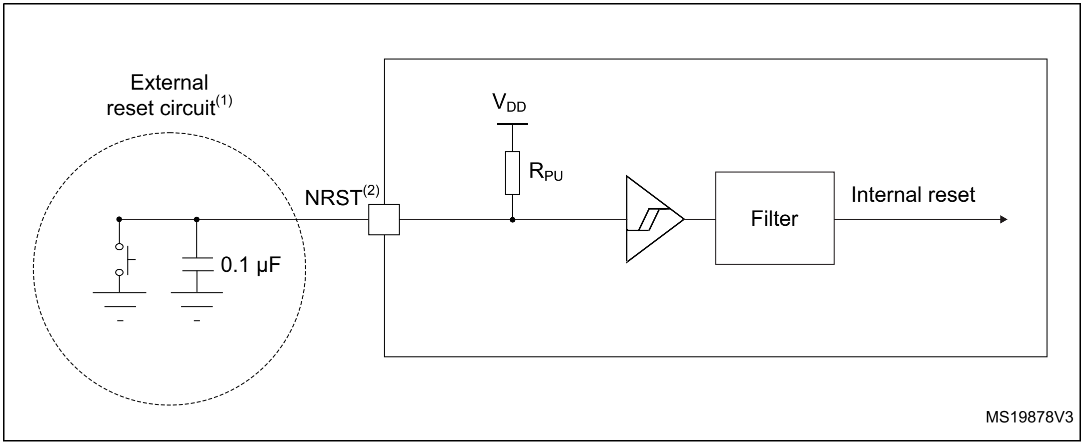
Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*. All I/Os are CMOS and TTL compliant.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2), $I_{IO} = +8$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2), $I_{IO} =+ 8$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	0.4	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	TTL port(2), $I_{IO} = -6$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	$I_{IO} = +15$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin	$I_{IO} = -15$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	V_{DD}-1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	$I_{IO} = +4$ mA $1.65\ V \leq V_{DD} < 3.6\ V$	-	0.45	
V_{OH}(3)(4)	Output high level voltage for an I/O pin	$I_{IO} = -4$ mA $1.65\ V \leq V_{DD} \leq 3.6\ V$	V_{DD}-0.45	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in Fm+ mode	$I_{IO} = 20$ mA $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	0.4	
		$I_{IO} = 10$ mA $1.65\ V \leq V_{DD} \leq 3.6\ V$	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 21*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 21*. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 23: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	Fast channel	1.65	-	3.6	V
		Standard channel	1.75[1]	-	3.6	
V_{REF+}	Positive reference voltage	-	1.65		V_{DDA}	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC on V_{DDA} and V_{REF+}	1.14 Msps	-	200	-	µA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD}[2]	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S[3]	Sampling rate	12-bit resolution	0.01	-	1.14	MHz
f_{TRIG}[3]	External trigger frequency	f_{ADC} = 16 MHz, 12-bit resolution	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{AIN} max for f_{ADC} = 16 MHz[1]

T_s (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > -10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 62. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} = V_{REF+} < 3.6 V, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(4)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(4)		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

6.3.17 Comparators

Table 65. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V, V_{IN+} = 0 V, V_{IN-} = V_{REFINT}, T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

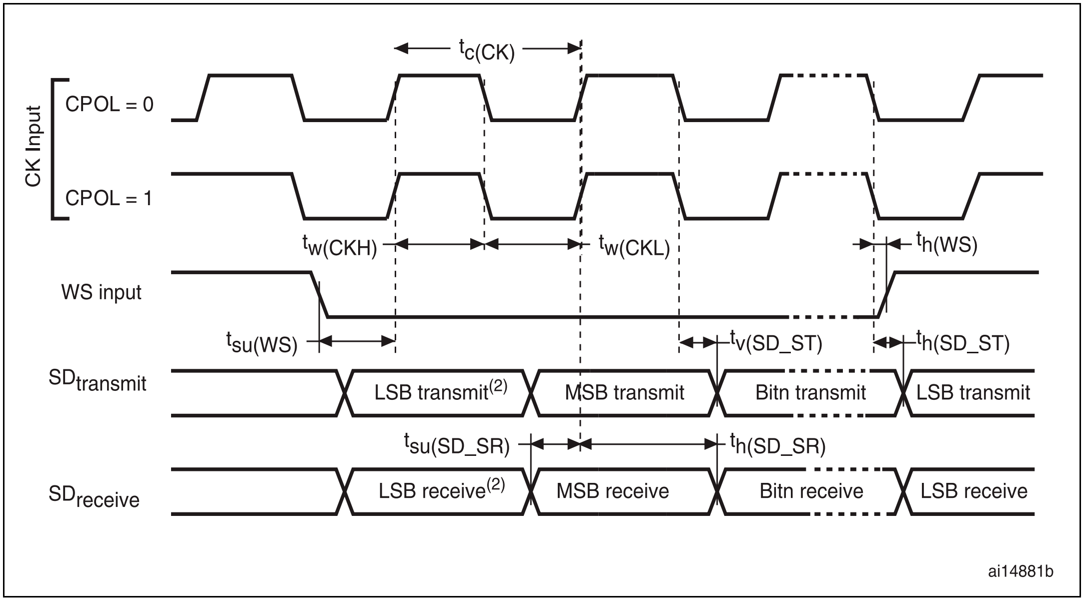
1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 66. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C, V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

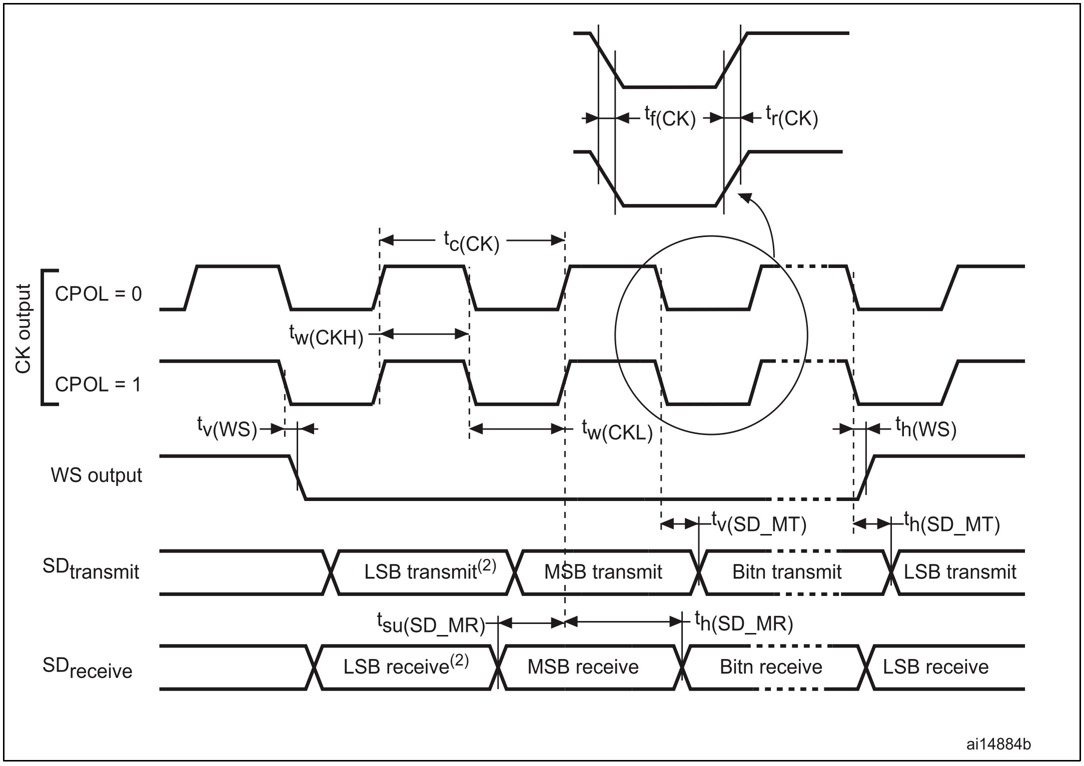
1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

Figure 35. I^2S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: 0.3 × V_{DD} and 0.7 × V_{DD}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 36. I^2S master timing diagram (Philips protocol)(1)



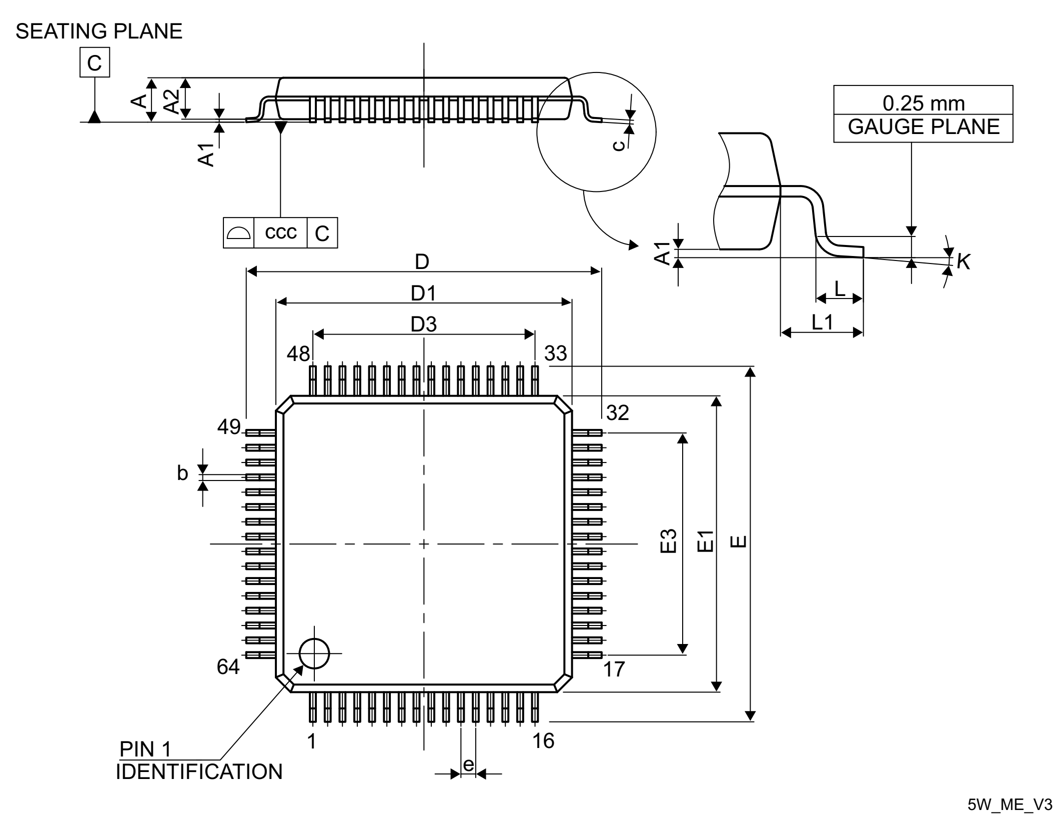
1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP64 package information

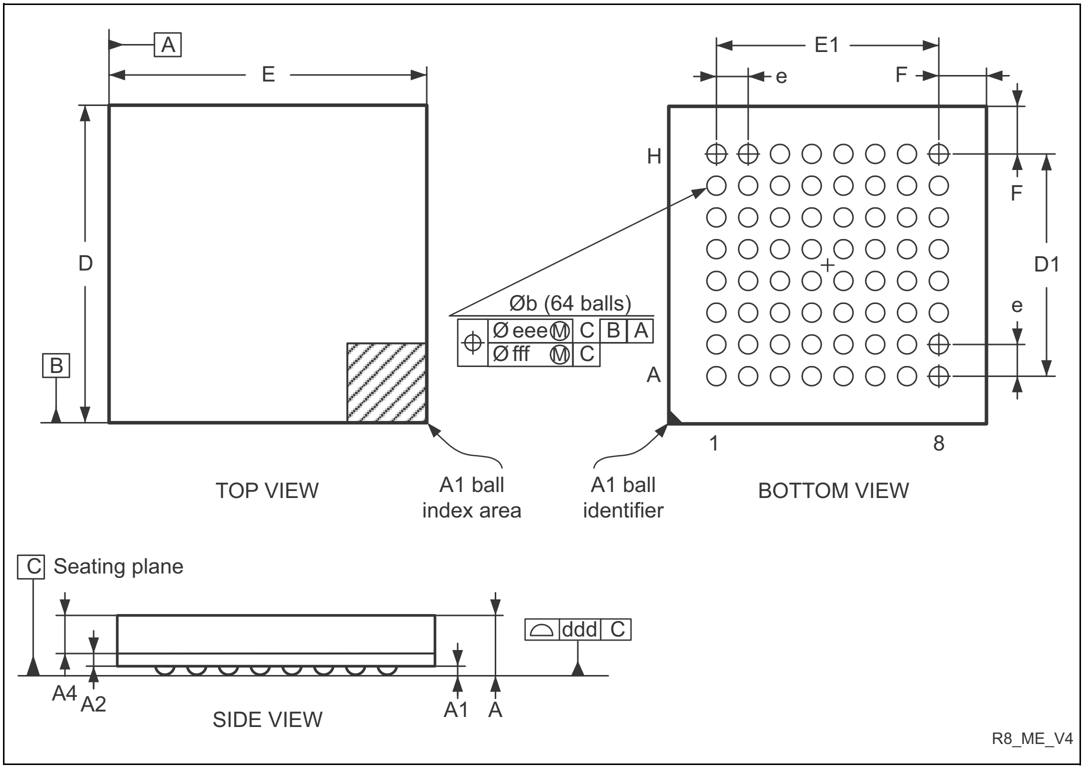
Figure 37. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.2 TFBGA64 package information

Figure 40. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 75. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

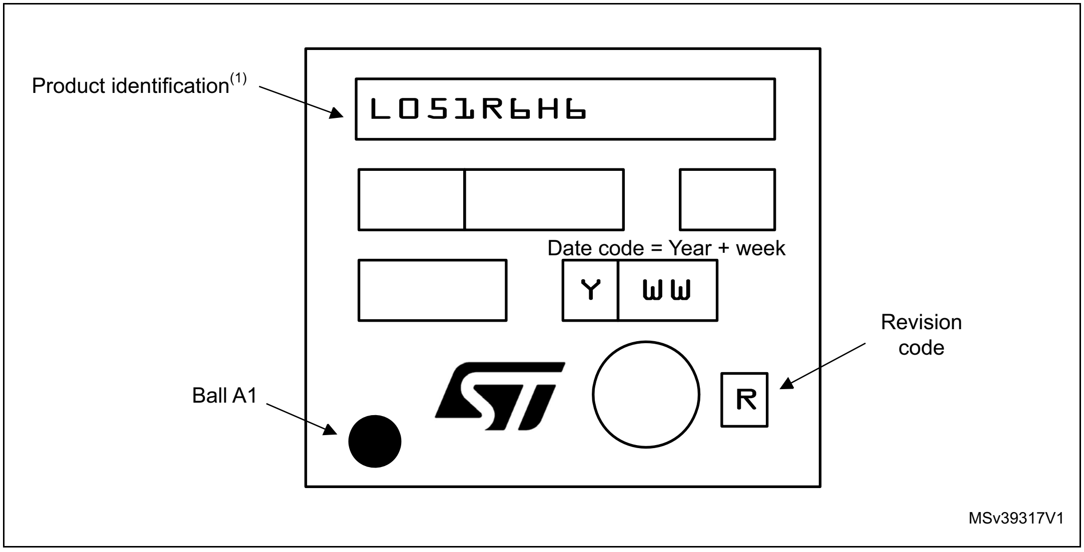
Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 42. TFBGA64 marking example (package top view)



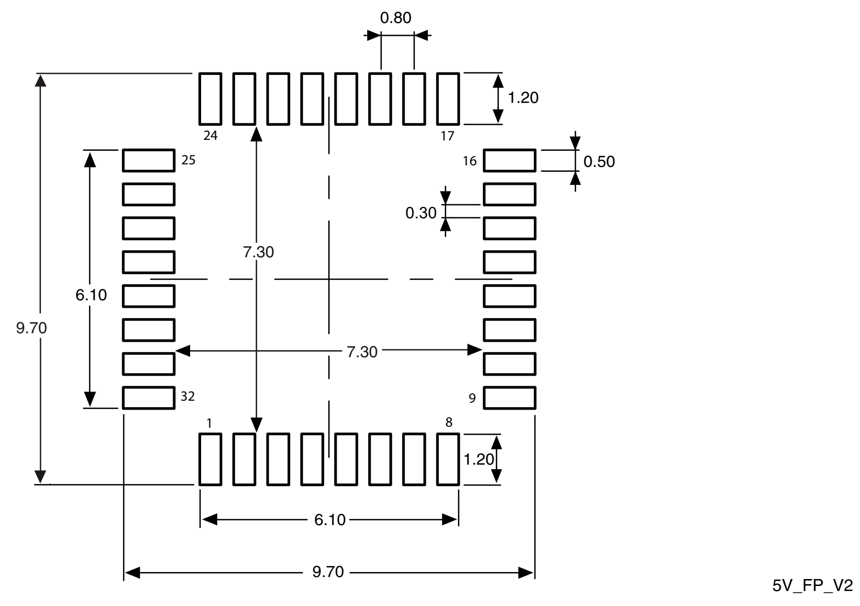
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 82. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



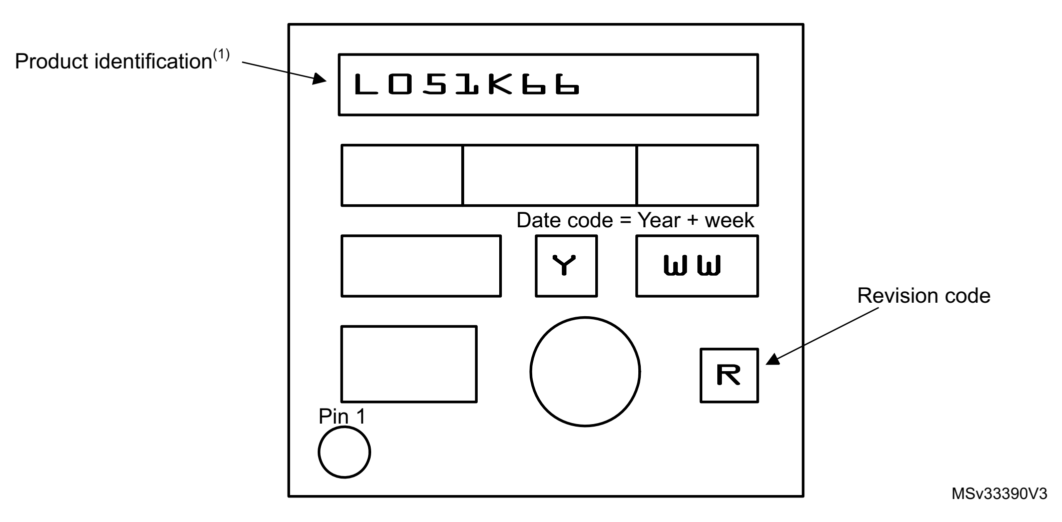
1. Dimensions are expressed in millimeters.

Device marking for UFQFPN32

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 56. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 86. Document revision history (continued)

Date	Revision	Changes
25-Jun-2014	3	Cover page: changed LQFP32 size, updated core speed. updated core speed, added minimum supply voltage for ADC and comparators. ADC now guaranteed down to 1.65 V. Updated list of applications in *Section 1: Introduction*. Changed number of I2S interfaces to one in *Section 2: Description*. Updated *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*. Updated *Table 3: Functionalities depending on the operating power supply range*. Updated RTC/TIM21 in *Table 6: STM32L0xx peripherals interconnect matrix*. Added note related to UFQFPN32 and note related to WLCSP36 in *Table 15: STM32L051x6/8 pin definitions*. Split LQFP32/UFQFPN32 pinout schematics into two distinct figures: *Figure 7* and *Figure 8*. Updated V_{DDA} in *Table 23: General operating conditions*. Split Table *Current consumption in Run mode, code with data processing running from Flash* into *Table 27* and *Table 28* and content updated. Split Table *Current consumption in Run mode, code with data processing running from RAM* into *Table 29* and *Table 30* and content updated. Updated *Table 31: Current consumption in Sleep mode*, *Table 32: Current consumption in Low-power run mode*, *Table 33: Current consumption in Low-power sleep mode*, *Table 34: Typical and maximum current consumptions in Stop mode*, *Table 35: Typical and maximum current consumptions in Standby mode*, and added *Table 36: Average current consumption during Wakeup*. Updated *Table 37: Peripheral current consumption in Run or Sleep mode* and added *Table 38: Peripheral current consumption in Stop and Standby mode*. Updated t_{LOCK} in *Table 47: PLL characteristics*. Removed note 1 below *Figure 21: HSE oscillator circuit diagram*. Updated *Table 49: Flash memory and data EEPROM characteristics* and *Table 50: Flash memory and data EEPROM endurance and retention*. Updated *Table 58: I/O AC characteristics*. Updated *Table 60: ADC characteristics*. Updated *Figure 57: Thermal resistance* and added note 1.

Table 86. Document revision history (continued)

Date	Revision	Changes
07-Mar-2017	7	Added thin WLCSP36 package Updated number of I2S interfaces in *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*. Removed note 2 related to PA4 in *Table 15: STM32L051x6/8 pin definitions* Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*. Removed CRS from *Table 37: Peripheral current consumption in Run or Sleep mode*. Added note 2. related to the position of the external capacitor below *Figure 27: Recommended NRST pin protection*. Updated R_L in *Table 60: ADC characteristics*. Updated t_{AF} maximum value for range 1 in *Table 68: I2C analog filter characteristics*. Updated $t_{WUUSART}$ description in *Table 69: USART/LPUART characteristics*. NSS timing waveforms updated in *Figure 32: SPI timing diagram - slave mode and CPHA = 0* and *Figure 33: SPI timing diagram - slave mode and CPHA = 1(1)*. Added reference to optional marking or inset/upset marks in all package device marking sections. Previous WLCSP36 package renamed “Standard” WLCSP36; added Note *2.* below *Figure 46: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline* and updated *Table 78: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data*.