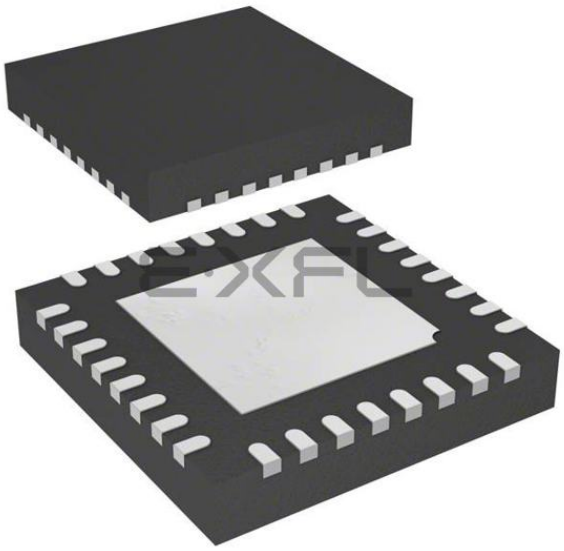


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051k6u6

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance

3.8 Memories

The STM32L051x6/8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32 or 64 Kbytes of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1(PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

3.13 Ultra-low-power comparators and reference voltage

The STM32L051x6/8 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

Table 15. STM32L051x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	TFBGA64	LQFP48	WLCSP36[1]	LQFP32	UFQFPN32						
33	H8	25	-	-	-	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, EVENTOUT	-
34	G8	26	-	-	-	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
35	F8	27	-	-	-	PB14	I/O	FTf	-	SPI2_MISO/I 2S2_MCK, RTC_OUT, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
36	F7	28	-	-	-	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD , RTC_REFIN	-
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM22_CH1	-
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM22_CH2	-
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM22_ETR	-
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM21_ETR	-
41	D7	29	E1	18	18	PA8	I/O	FT	-	MCO, EVENTOUT, USART1_CK	-
42	C7	30	D1	19	19	PA9	I/O	FT	-	MCO, USART1_TX	-
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX	-
44	C8	32	C2	21	21	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART1_CTS, COMP1_OUT	-
45	B8	33	B1	22	22	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART1_RTS_DE, COMP2_OUT	-
46	A8	34	A1	23	23	PA13	I/O	FT	-	SWDIO	-
47	D5	35	-	-	-	VSS	S		-	-	-

Table 15. STM32L051x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	TFBGA64	LQFP48	WLCSP36[1]	LQFP32	UFQFPN32						
63	D4	47	D6	32	-	VSS	S	-	-	-	-
64	E4	48	A5	1	1	VDD	S	-	-	-	-

1. PB9/12/13/14/15, PH0/1 and PC13 GPIOs should be configured as output and driven Low, even if they are not available on this package.

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 23*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power-on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 26* are based on characterization results, unless otherwise specified.

Table 25. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 26. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 26. Embedded internal reference voltage(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 38: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 40: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 47*, *Table 23* and *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

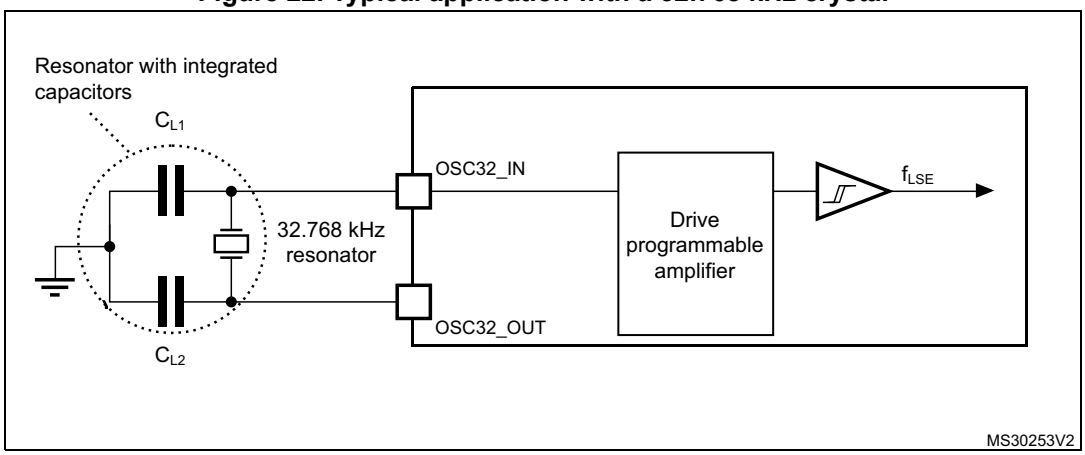
Table 43. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Table 58. I/O AC characteristics(1)

OSPEEDRx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	320	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	0.6	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	65	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	13	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	28	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	35	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	10	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	6	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	17	
Fm+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.5 V to 3.6 V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	10	ns
	$t_{r(IO)out}$	Output rise time		-	30	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 1.65 V to 3.6 V	-	350	KHz
	$t_{f(IO)out}$	Output fall time		-	15	ns
	$t_{r(IO)out}$	Output rise time		-	60	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 26*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.

The analog spike filter is compliant with I^2C timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1 or Range 2.
  - V_{DD} < 2 V, voltage scaling Range 1 or Range 2, C_{load} < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 68. I2C analog filter characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50(2)	260(3)	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 69. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when the USART/LPUART is clocked by HSI	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	µs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 70. SPI characteristics in voltage Range 1 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71<V_{DD}<3.6V$	-	-	12(2)	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$	-	-	16(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+ 2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	3.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.65\ V<V_{DD}<3.6\ V$	-	18	41	
		Slave mode $2.7\ V<V_{DD}<3.6\ V$	-	18	25	
$t_{v(MO)}$		Master mode	-	4	7	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

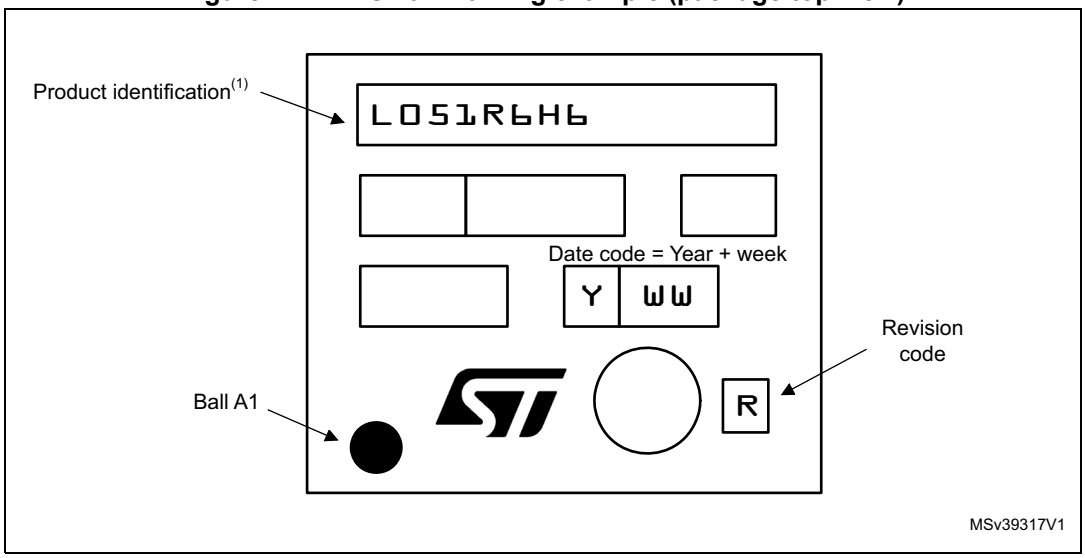
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 42. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 78. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.305[3]	-	-	0.012	-
G	-	0.440[3]	-	-	0.017	-
aaa	-	-	0.100	-	-	0.004
bbb	-	-	0.100	-	-	0.004
ccc	-	-	0.100	-	-	0.004
ddd	-	-	0.050	-	-	0.002
eee	-	-	0.050	-	-	0.002

1. Values in inches are converted from mm and rounded to the 3rd decimal place.
2. Nominal dimension rounded to the 3rd decimal place results from process capability.
3. Calculated dimensions are rounded to the 3rd decimal place.

Figure 47. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale recommended footprint

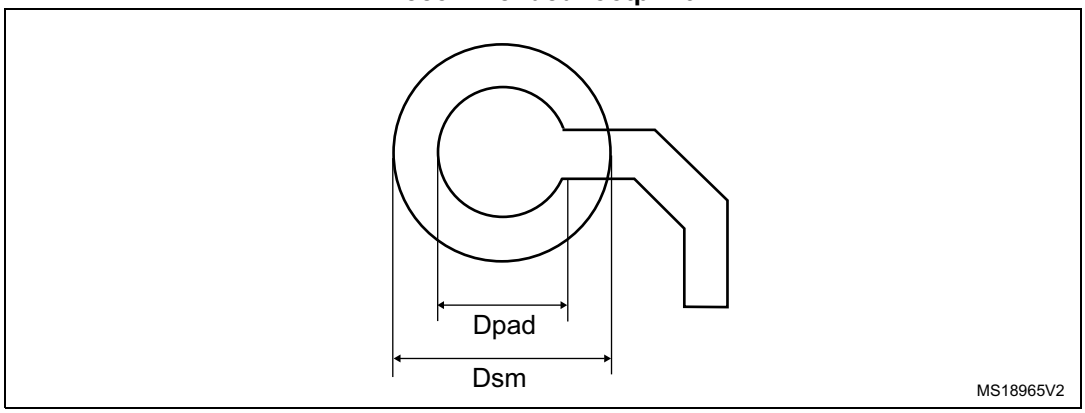


Table 79. Standard WLCSP36 recommended PCB design rules

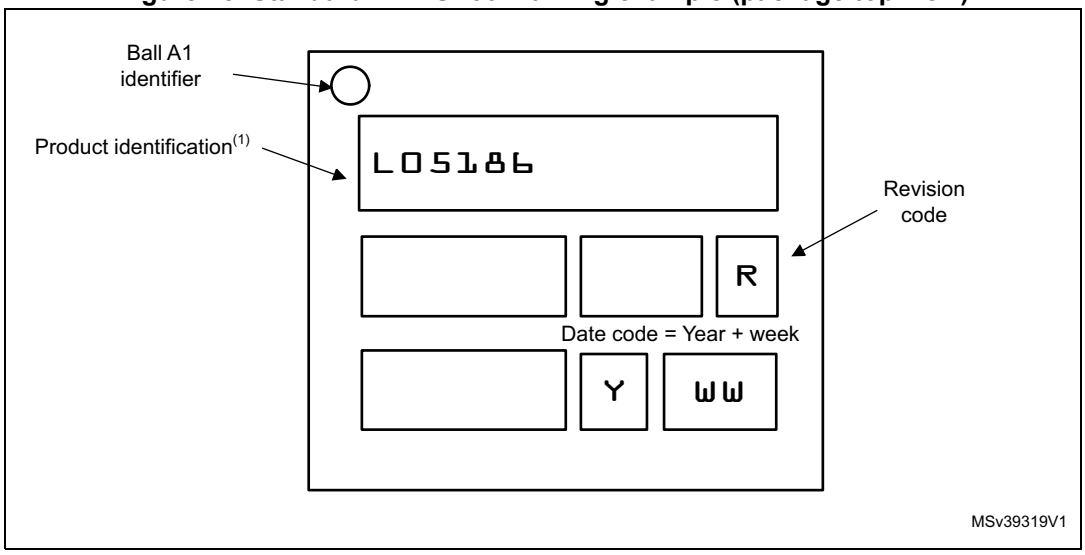
Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Device marking for standard WLCSP36

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. Standard WLCSP36 marking example (package top view)



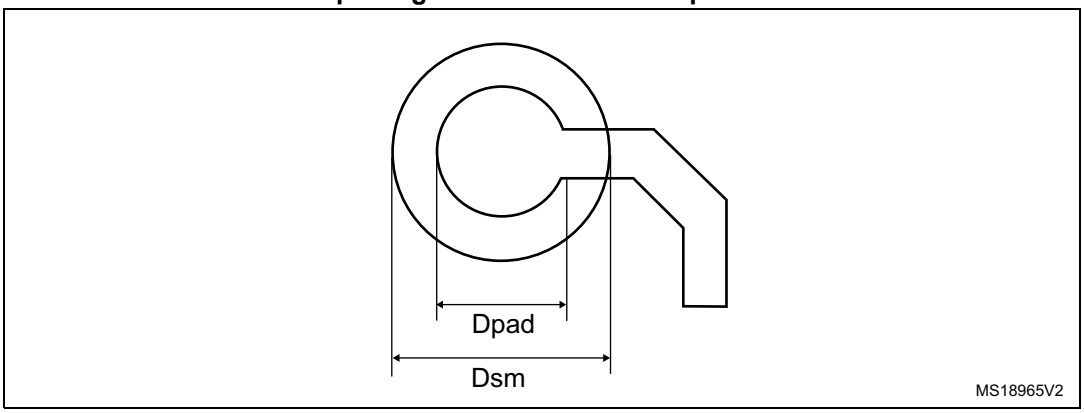
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 80. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.33	-	-	0.013
A1	-	0.10	-	-	0.004	-
A2	-	0.20	-	-	0.008	-
A3	-	0.025[2]	-	-	0.001	-
b	0.16	0.19	0.22	0.006	0.007	0.009
D	2.59	2.61	2.63	0.102	0.103	0.104
E	2.86	2.88	2.90	0.112	0.113	0.114
e	-	0.40	-	-	0.016	-
e1	-	2.00	-	-	0.079	-
e2	-	2.00	-	-	0.079	-
F	-	0.305[3]	-	-	0.012	-
G	-	0.440[3]	-	-	0.017	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

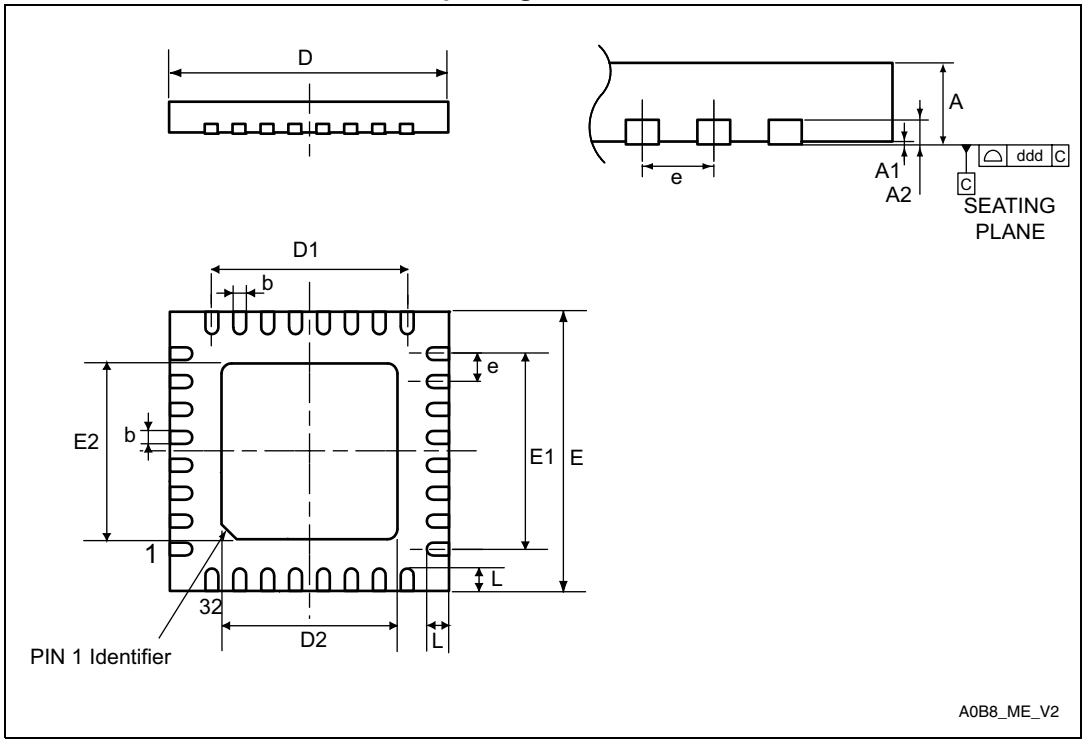
1. Values in inches are converted from mm and rounded to the 3rd decimal place.
2. Back side coating. Nominal dimension rounded to the 3rd decimal place results from process capability.
3. Calculated dimensions are rounded to 3rd decimal place.

Figure 50. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



7.7 UFQFPN32 package information

Figure 54. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

8 Part numbering

Table 85. STM32L051x6/8 ordering information scheme

Example: STM32 L 051 R 8 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

051 = Access line

Pin count

K = 32 pins

T = 36 pins

C = 48/49 pins

R = 64 pins

Flash memory size

6 = 32 Kbytes

8 = 64 Kbytes

Package

T = LQFP

H = TFBGA

U = UFQFPN

Y = Standard WLCSP pins

F = Thin WLCSP pins

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 86. Document revision history (continued)

Date	Revision	Changes
05-Sep-2014	4	Extended operating temperature range to 125 °C. Updated minimum ADC operating voltage to 1.65 V. Updated *Section 3.4.1: Power supply schemes*. Replaced USART3 by LPUART1 and updated I/O structure for PC5 and PC15 pins in *Table 15: STM32L051x6/8 pin definitions*. Replaced LPUART by LPUART1 in *Table 16: Alternate function port A*, *Table 17: Alternate function port B*, *Table 18: Alternate function port C* and *Table 19: Alternate function port D*. Updated temperature range in *Section 2: Description*, *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*. Updated P_D, $T_{A\ and}$ T_J to add range 3 in *Table 23: General operating conditions*. Added range 3 in *Table 50: Flash memory and data EEPROM endurance and retention*, *Table 85: STM32L051x6/8 ordering information scheme*. Update note 1 in *Table 27: Current consumption in Run mode, code with data processing running from Flash*, *Table 29: Current consumption in Run mode, code with data processing running from RAM*, *Table 31: Current consumption in Sleep mode*, *Table 32: Current consumption in Low-power run mode*, *Table 33: Current consumption in Low-power sleep mode*, *Table 34: Typical and maximum current consumptions in Stop mode*, *Table 35: Typical and maximum current consumptions in Standby mode* and *Table 39: Low-power mode wakeup timings*. Updated *Figure 57: Thermal resistance* and removed note 1. Updated *Table 60: ADC characteristics* and *Table 62: ADC accuracy*. Updated *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive*, *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 35: Typical and maximum current consumptions in Standby mode*. Updated SYSCFG in *Table 37: Peripheral current consumption in Run or Sleep mode*. Updated *Table 38: Peripheral current consumption in Stop and Standby mode* and *Table 39: Low-power mode wakeup timings*. Updated ACC_{HSI16} temperature conditions in *Table 44: 16 MHz HSI16 oscillator characteristics*. Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in *Table 59: NRST pin characteristics*. Updated *Table 60: ADC characteristics* and *Table 62: ADC accuracy*. Added range 3 in *Table 85: STM32L051x6/8 ordering information scheme*.

Table 86. Document revision history (continued)

Date	Revision	Changes
17-Mar-2016	6	Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*. Changed minimum comparator supply voltage to 1.65 V on cover page. Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*. Updated *Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.16.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.16.3: Low-power universal asynchronous receiver transmitter (LPUART)*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Changed V_{DDA} minimum value to 1.65 V in *Table 23: General operating conditions*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 60: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note *1.* Added note 4 related to R_{ADC}. Updated f_{TRIG} and V_{AIN} maximum value. Updated t_S and t_{CONV}. Added V_{REF+}. – Updated equation 1 description. – Updated *Table 61: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. Added *Table 69: USART/LPUART characteristics*. Updated *Figure 45: LQFP48 marking example (package top view)*.