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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051k8t6

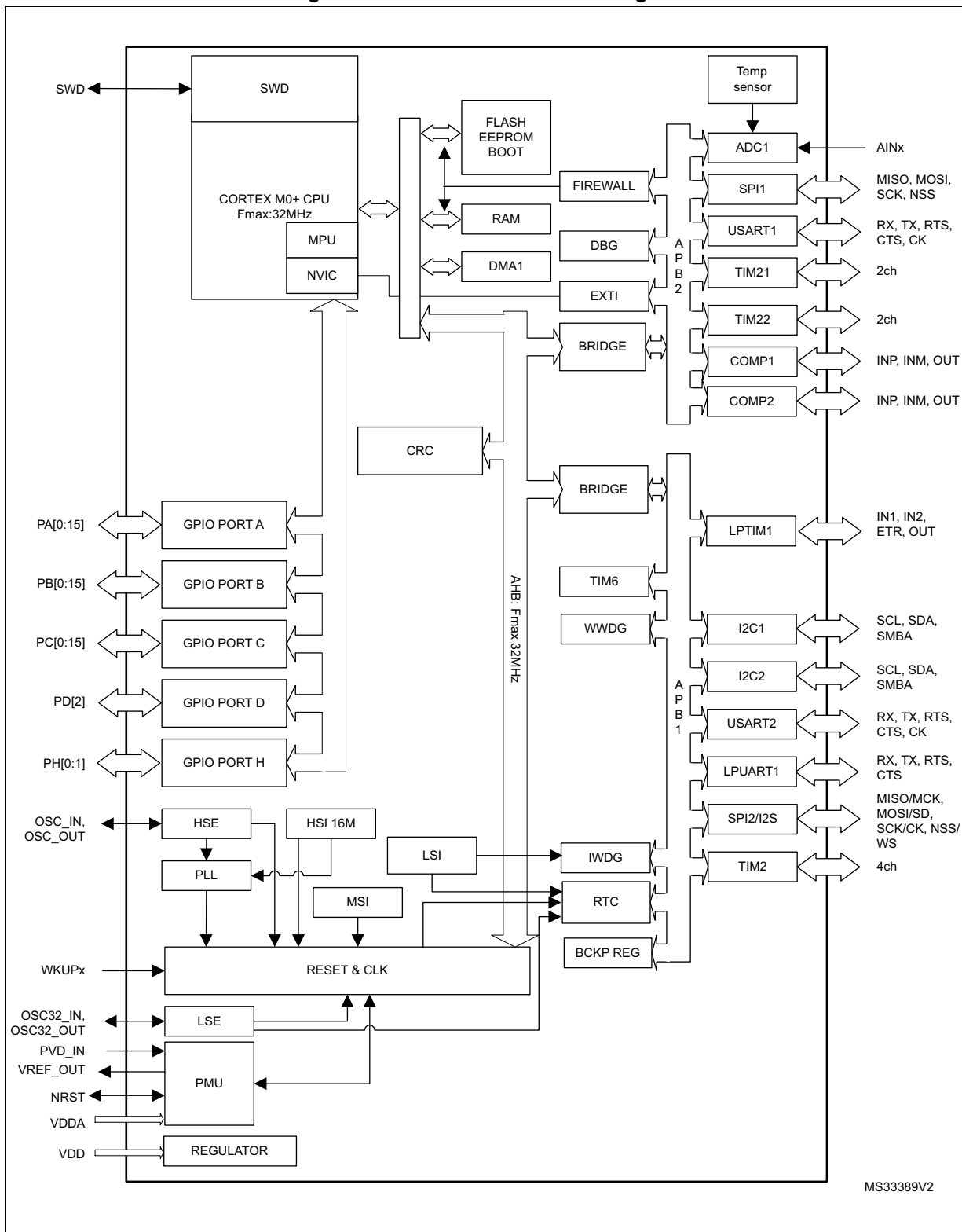
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Figure 1. STM32L051x6/8 block diagram



**Table 5. Functionalities depending on the working mode
(from Run/active down to standby) (continued)⁽¹⁾**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Consumption $V_{DD}=1.8$ to 3.6 V (Typ)	Down to $140\text{ }\mu\text{A/MHz}$ (from Flash memory)	Down to $37\text{ }\mu\text{A/MHz}$ (from Flash memory)	Down to $8\text{ }\mu\text{A}$	Down to $4.5\text{ }\mu\text{A}$	$0.4\text{ }\mu\text{A}$ (No RTC) $V_{DD}=1.8\text{ V}$	$0.28\text{ }\mu\text{A}$ (No RTC) $V_{DD}=1.8\text{ V}$
					$0.8\text{ }\mu\text{A}$ (with RTC) $V_{DD}=1.8\text{ V}$	$0.65\text{ }\mu\text{A}$ (with RTC) $V_{DD}=1.8\text{ V}$
					$0.4\text{ }\mu\text{A}$ (No RTC) $V_{DD}=3.0\text{ V}$	$0.29\text{ }\mu\text{A}$ (No RTC) $V_{DD}=3.0\text{ V}$
					$1\text{ }\mu\text{A}$ (with RTC) $V_{DD}=3.0\text{ V}$	$0.85\text{ }\mu\text{A}$ (with RTC) $V_{DD}=3.0\text{ V}$

- Legend:
 "Y" = Yes (enable).
 "O" = Optional can be enabled/disabled by software
 "-" = Not available
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2, TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-

internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**
To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**
Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**
To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**
Three different clock sources can be used to drive the master clock SYSCLK:
 - 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source**
Two ultra-low-power clock sources that can be used to drive the real-time clock:

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3\text{ V}$	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C $V_{DDA} = 3\text{ V}$	0x1FF8 007E - 0x1FF8 007F

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+} , is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C $V_{DDA} = 3\text{ V}$	0x1FF8 0078 - 0x1FF8 0079

3.13 Ultra-low-power comparators and reference voltage

The STM32L051x6/8 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
 - External I/O pins
 - Internal reference voltage (V_{REFINT})
 - submultiple of Internal reference voltage (1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μA typical).

3.14 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.15 Timers and watchdogs

The ultra-low-power STM32L051x6/8 devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

[Table 9](#) compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L051x6/8 devices (see [Table 9](#) for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or

Table 18. Alternate function port C

Port		AF0	AF1	AF2
		LPUART1/LPTIM/TIM21/12/EVENTOUT	-	SPI2/I2S2/LPUART1/EVENTOUT
Port C	PC0	LPTIM1_IN1	-	EVENTOUT
	PC1	LPTIM1_OUT	-	EVENTOUT
	PC2	LPTIM1_IN2	-	SPI2_MISO/I2S2_MCK
	PC3	LPTIM1_ETR	-	SPI2_MOSI/I2S2_SD
	PC4	EVENTOUT	-	LPUART1_TX
	PC5		-	LPUART1_RX
	PC6	TIM22_CH1	-	-
	PC7	TIM22_CH2	-	-
	PC8	TIM22_ETR	-	-
	PC9	TIM21_ETR	-	-
	PC10	LPUART1_TX	-	-
	PC11	LPUART1_RX	-	-
	PC12	-	-	-
	PC13	-	-	-
	PC14	-	-	-
	PC15	-	-	-

Table 19. Alternate function port D

Port		AF0	AF1
		LPUART1	-
Port D	PD2	LPUART1_RTS_DE	-

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. LSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min ⁽²⁾	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$ ⁽³⁾	Startup time	V_{DD} is stabilized	-	2	-	s

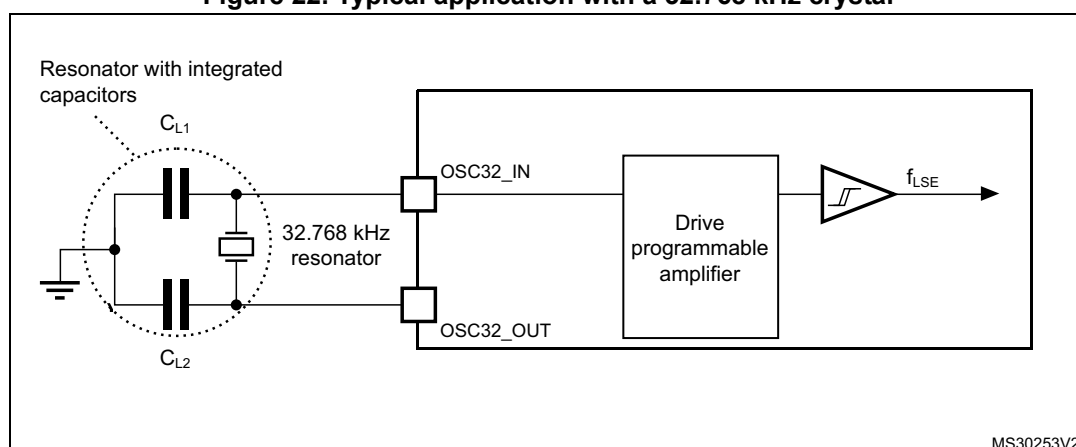
1. Guaranteed by design.

2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{\text{LSI}}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{\text{LSI}}^{(2)}$	LSI oscillator frequency drift $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	-10	-	4	%
$t_{\text{su(LSI)}}^{(3)}$	LSI oscillator startup time	-	-	200	μs
$I_{\text{DD(LSI)}}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.

2. This is a deviation for an individual part, once the initial frequency has been measured.

3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 46. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at $V_{\text{DD}} = 3.3\text{ V}$ and $T_A = 25^{\circ}\text{C}$	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	± 0.5	-	%
$D_{\text{TEMP(MSI)}}^{(1)}$	MSI oscillator frequency drift $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	-	± 3	-	%
	MSI oscillator frequency drift $V_{\text{DD}} = 3.3\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 110^{\circ}\text{C}$	MSI range 0	- 8.9	+7.0	
		MSI range 1	- 7.1	+5.0	
		MSI range 2	- 6.4	+4.0	
		MSI range 3	- 6.2	+3.0	
		MSI range 4	- 5.2	+3.0	
		MSI range 5	- 4.8	+2.0	
$D_{\text{VOLT(MSI)}}^{(1)}$	MSI oscillator frequency drift $1.65\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$, $T_A = 25^{\circ}\text{C}$	-	-	2.5	%V

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

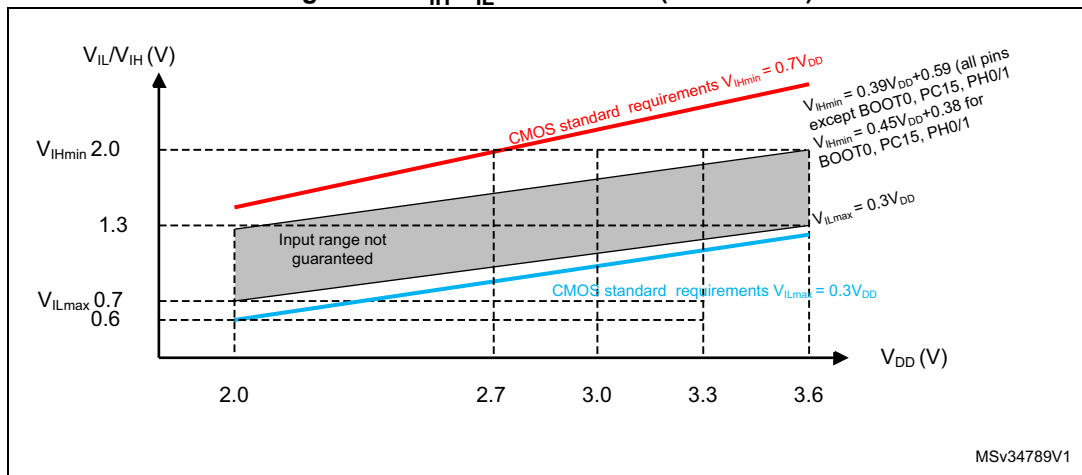
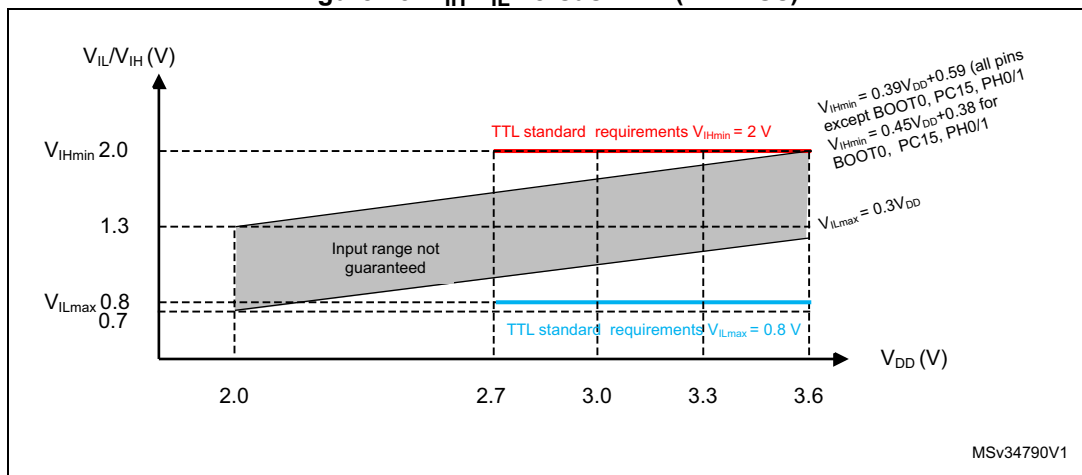
The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\ \mu\text{A}/+0\ \mu\text{A}$ range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the [Table 55](#).

Table 55. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA4, PA5, PA11, PA12, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT, FTf pins	-5 ⁽¹⁾	NA	
	Injected current on any other pins	-5 ⁽¹⁾	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Figure 24. V_{IH}/V_{IL} versus V_{DD} (CMOS I/Os)Figure 25. V_{IH}/V_{IL} versus V_{DD} (TTL I/Os)

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 15 mA with the non-standard V_{OL}/V_{OH} specifications given in [Table 57](#).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see [Table 21](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see [Table 21](#)).

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{AIN} max for $f_{ADC} = 16 \text{ MHz}^{(1)}$

T_S (cycles)	t_S (μs)	R_{AIN} max for fast channels ($k\Omega$)	R_{AIN} max for standard channels ($k\Omega$)						
			$V_{DD} > 2.7 \text{ V}$	$V_{DD} > 2.4 \text{ V}$	$V_{DD} > 2.0 \text{ V}$	$V_{DD} > 1.8 \text{ V}$	$V_{DD} > 1.75 \text{ V}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > -10 \text{ }^\circ\text{C}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > 25 \text{ }^\circ\text{C}$
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 62. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

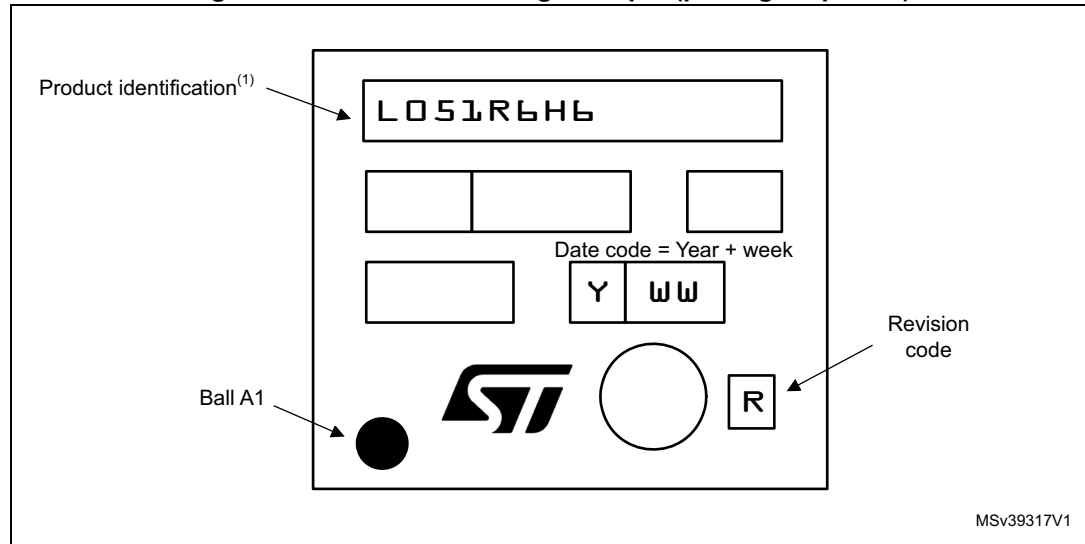
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$1.65 \text{ V} < V_{DDA} = V_{REF+} < 3.6 \text{ V}$, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11	-	bits
	Effective number of bits (16-bit mode oversampling with ratio =256) ⁽⁴⁾		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) ⁽⁴⁾		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 42. TFBGA64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

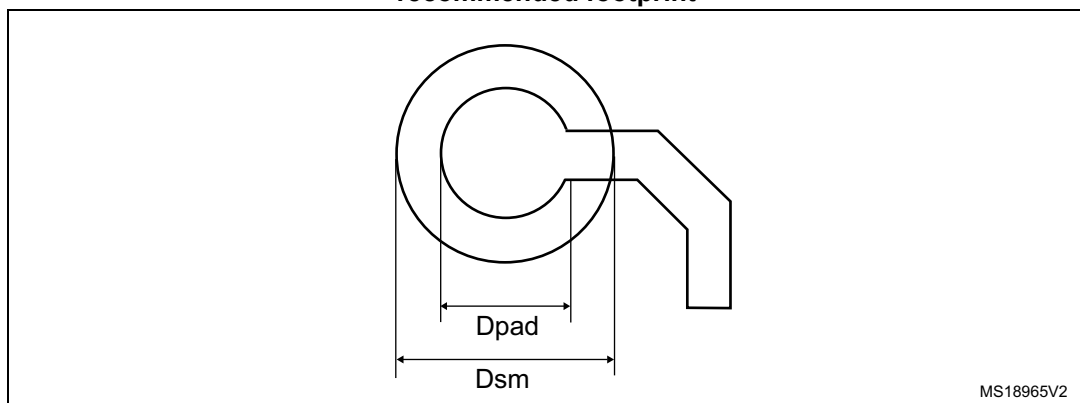
Table 78. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
F	-	0.305 ⁽³⁾	-	-	0.012	-
G	-	0.440 ⁽³⁾	-	-	0.017	-
aaa	-	-	0.100	-	-	0.004
bbb	-	-	0.100	-	-	0.004
ccc	-	-	0.100	-	-	0.004
ddd	-	-	0.050	-	-	0.002
eee	-	-	0.050	-	-	0.002

1. Values in inches are converted from mm and rounded to the 3rd decimal place.

2. Nominal dimension rounded to the 3rd decimal place results from process capability.

3. Calculated dimensions are rounded to the 3rd decimal place.

Figure 47. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale recommended footprint**Table 79. Standard WLCSP36 recommended PCB design rules**

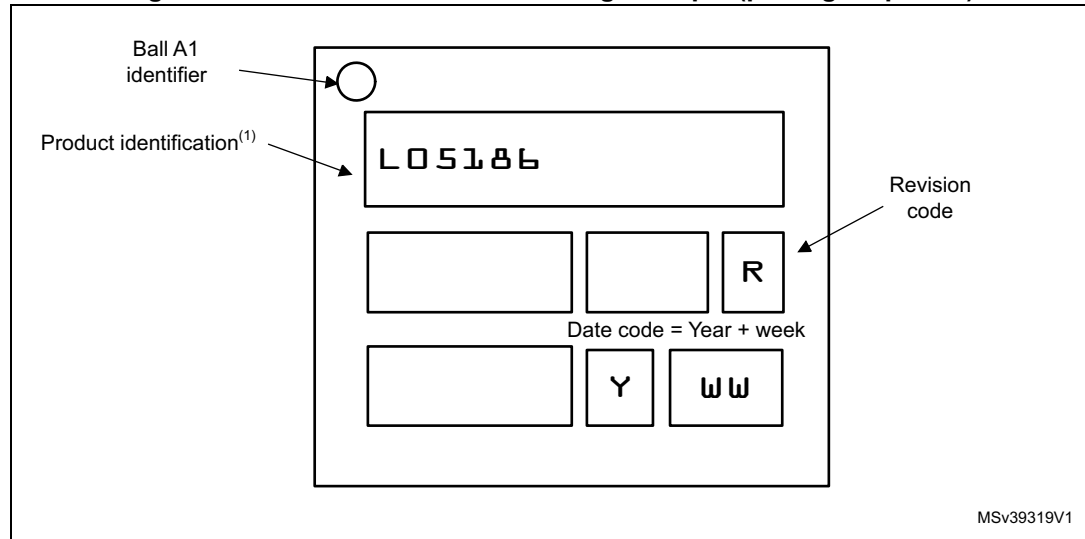
Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Device marking for standard WLCSP36

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. Standard WLCSP36 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 84. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	61	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient Standard WLCSP36 - 0.4 mm pitch	63	
	Thermal resistance junction-ambient Thin WLCSP36 - 0.4 mm pitch	59	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	38	

8 Part numbering

Table 85. STM32L051x6/8 ordering information scheme

Example:	STM32	L	051	R	8	T	6	D	TR									
Device family																		
STM32 = ARM-based 32-bit microcontroller																		
Product type																		
L = Low power																		
Device subfamily																		
051 = Access line																		
Pin count																		
K = 32 pins																		
T = 36 pins																		
C = 48/49 pins																		
R = 64 pins																		
Flash memory size																		
6 = 32 Kbytes																		
8 = 64 Kbytes																		
Package																		
T = LQFP																		
H = TFBGA																		
U = UFQFPN																		
Y = Standard WLCSP pins																		
F = Thin WLCSP pins																		
Temperature range																		
6 = Industrial temperature range, −40 to 85 °C																		
7 = Industrial temperature range, −40 to 105 °C																		
3 = Industrial temperature range, −40 to 125 °C																		
Options																		
No character = V _{DD} range: 1.8 to 3.6 V and BOR enabled																		
D = V _{DD} range: 1.65 to 3.6 V and BOR disabled																		
Packing																		
TR = tape and reel																		
No character = tray or tube																		

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

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