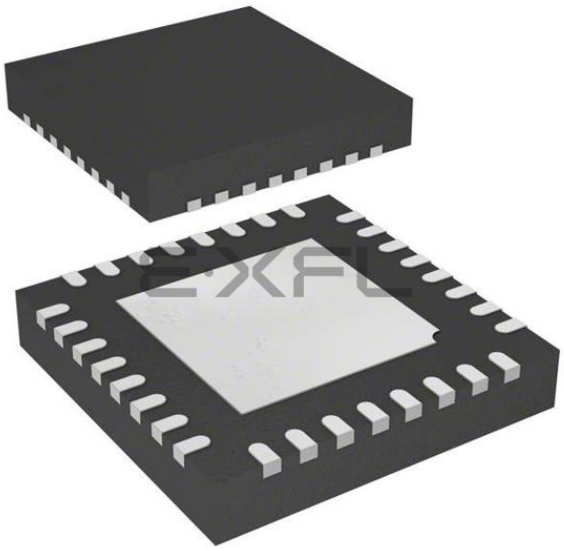

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051k8u3

List of tables

2 Description

The access line ultra-low-power STM32L051x6/8 microcontrollers incorporate the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L051x6/8 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L051x6/8 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L051x6/8 devices embed standard and advanced communication interfaces: up to two I2C, two SPIs, one I2S, two USARTs, a low-power UART (LPUART), .

The STM32L051x6/8 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L051x6/8 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USARTs, LPUART, LPTIMER or comparator events.

3.8 Memories

The STM32L051x6/8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32 or 64 Kbytes of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1(PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

3.13 Ultra-low-power comparators and reference voltage

The STM32L051x6/8 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

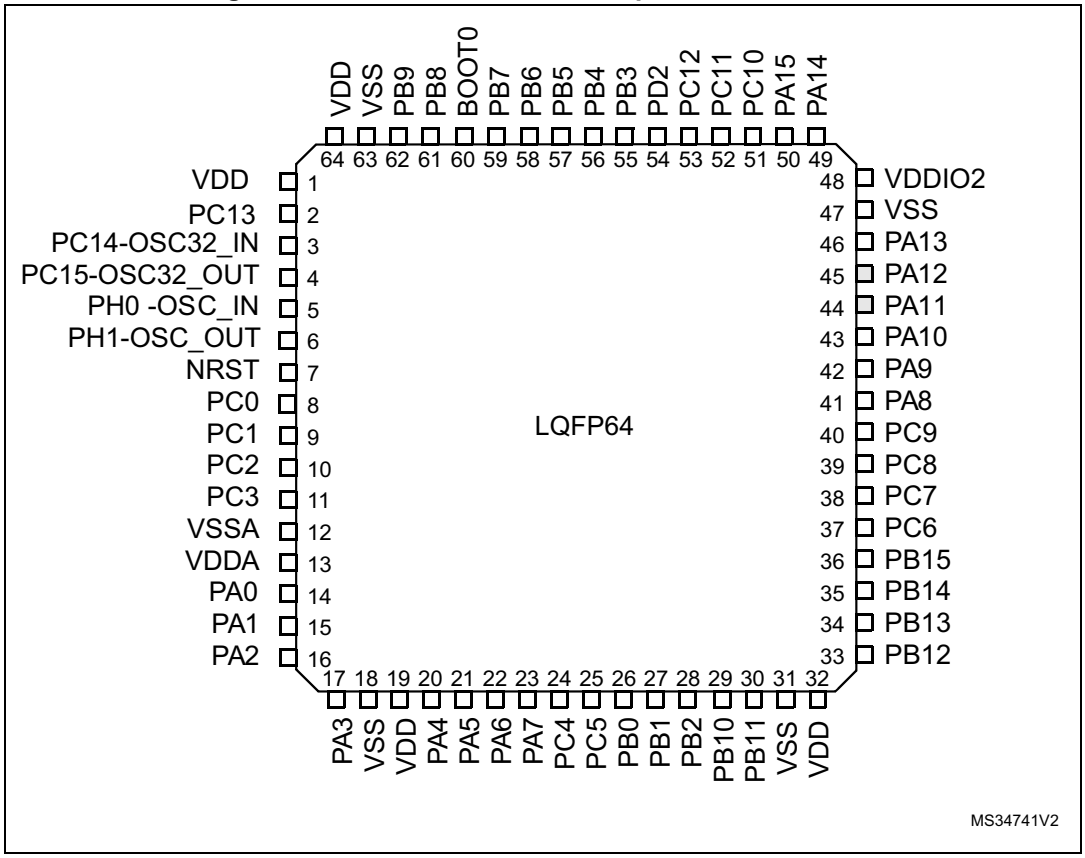
- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

4 Pin descriptions

Figure 3. STM32L051x6/8 LQFP64 pinout - 10 x 10 mm



1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 15. STM32L051x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	TFBGA64	LQFP48	WLCSP36[1]	LQFP32	UFQFPN32						
33	H8	25	-	-	-	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, EVENTOUT	-
34	G8	26	-	-	-	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
35	F8	27	-	-	-	PB14	I/O	FTf	-	SPI2_MISO/I 2S2_MCK, RTC_OUT, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
36	F7	28	-	-	-	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD , RTC_REFIN	-
37	F6	-	-	-	-	PC6	I/O	FT	-	TIM22_CH1	-
38	E7	-	-	-	-	PC7	I/O	FT	-	TIM22_CH2	-
39	E8	-	-	-	-	PC8	I/O	FT	-	TIM22_ETR	-
40	D8	-	-	-	-	PC9	I/O	FT	-	TIM21_ETR	-
41	D7	29	E1	18	18	PA8	I/O	FT	-	MCO, EVENTOUT, USART1_CK	-
42	C7	30	D1	19	19	PA9	I/O	FT	-	MCO, USART1_TX	-
43	C6	31	C1	20	20	PA10	I/O	FT	-	USART1_RX	-
44	C8	32	C2	21	21	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART1_CTS, COMP1_OUT	-
45	B8	33	B1	22	22	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART1_RTS_DE, COMP2_OUT	-
46	A8	34	A1	23	23	PA13	I/O	FT	-	SWDIO	-
47	D5	35	-	-	-	VSS	S		-	-	-

Table 15. STM32L051x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	TFBGA64	LQFP48	WLCSP36[1]	LQFP32	UFQFPN32						
48	E5	36	-	-	-	VDDIO2	S		-	-	-
49	A7	37	B2	24	24	PA14	I/O	FT	-	SWCLK, USART2_TX	
50	A6	38	A2	25	25	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	-
51	B7	-	-	-	-	PC10	I/O	FT	-	LPUART1_TX	-
52	B6	-	-	-	-	PC11	I/O	FT	-	LPUART1_RX	-
53	C5	-	-	-	-	PC12	I/O	FT	-	-	-
54	B5	-	-	-	-	PD2	I/O	FT	-	LPUART1_RTS_DE	-
55	A5	39	B3	26	26	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INN
56	A4	40	A3	27	27	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TIM22_CH1	COMP2_INP
57	C4	41	C4	28	28	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
58	D3	42	B4	29	29	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR	COMP2_INP
59	C3	43	A4	30	30	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2	COMP2_INP, PVD_IN
60	B4	44	C5	31	31	BOOT0	B		-	-	-
61	B3	45	B5	-	32	PB8	I/O	FTf	-	I2C1_SCL	-
62	A3	46	-	-	-	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 23*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power-on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 37. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral	Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
	Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
All enabled	283	225	222.5	212.5	µA/MHz (f_{HCLK})
PWR	2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 38. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	-	1.4	
-	LSE Low drive(2)	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	

1. LPTIM peripheral cannot operate in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

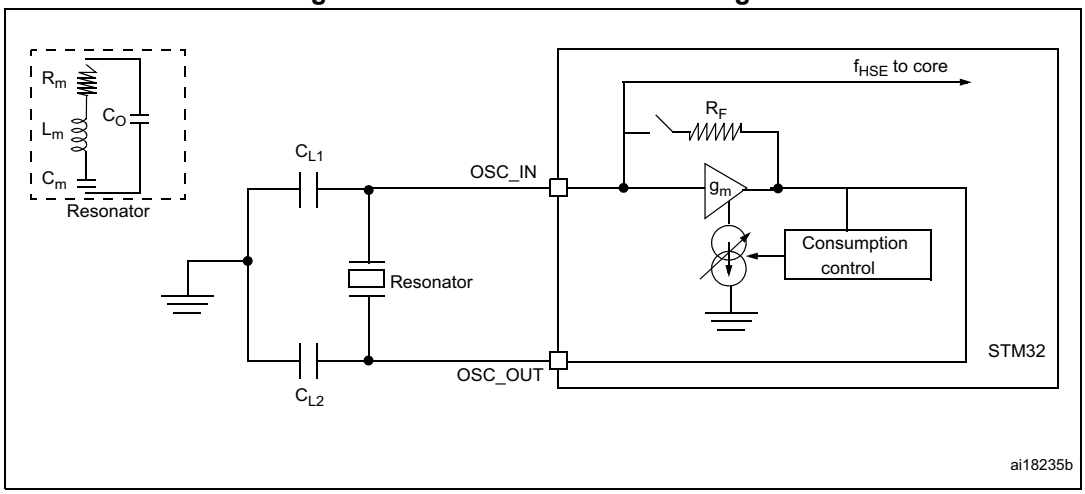
Table 42. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
G_m	Maximum critical crystal transconductance	Startup	-	-	700	µA /V
$t_{SU(HSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 21. HSE oscillator circuit diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

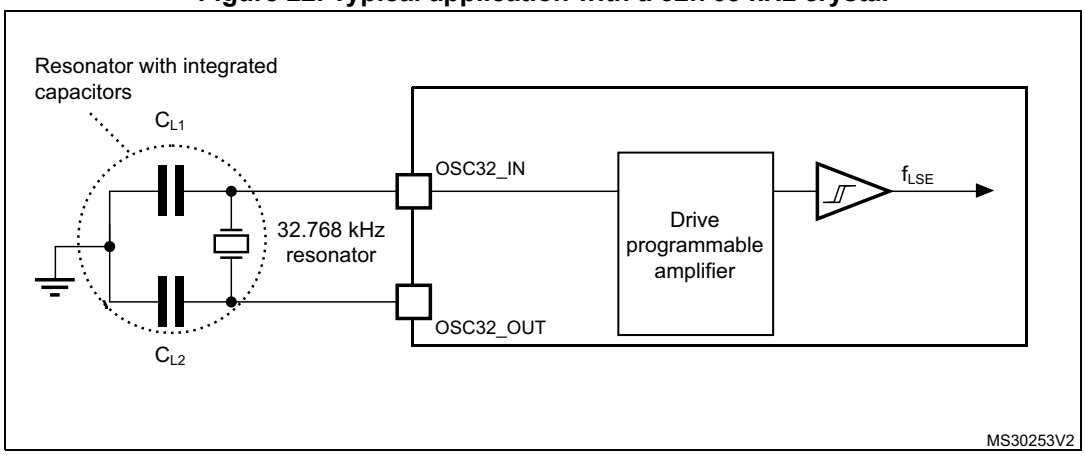
Table 43. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤T_A ≤85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 46. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤T_A ≤110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 55*.

Table 55. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA4, PA5, PA11, PA12, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT, FTf pins	-5 (1)	NA	
	Injected current on any other pins	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

The analog spike filter is compliant with I^2C timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1 or Range 2.
  - V_{DD} < 2 V, voltage scaling Range 1 or Range 2, C_{load} < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 68. I2C analog filter characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50(2)	260(3)	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 69. USART/LPUART characteristics

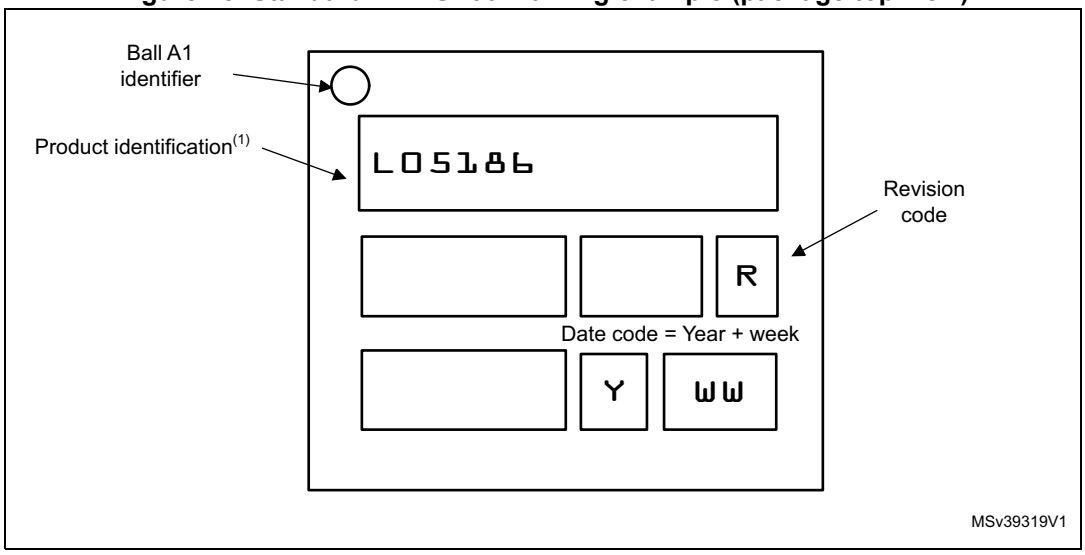
Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when the USART/LPUART is clocked by HSI	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	µs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

Device marking for standard WLCSP36

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. Standard WLCSP36 marking example (package top view)



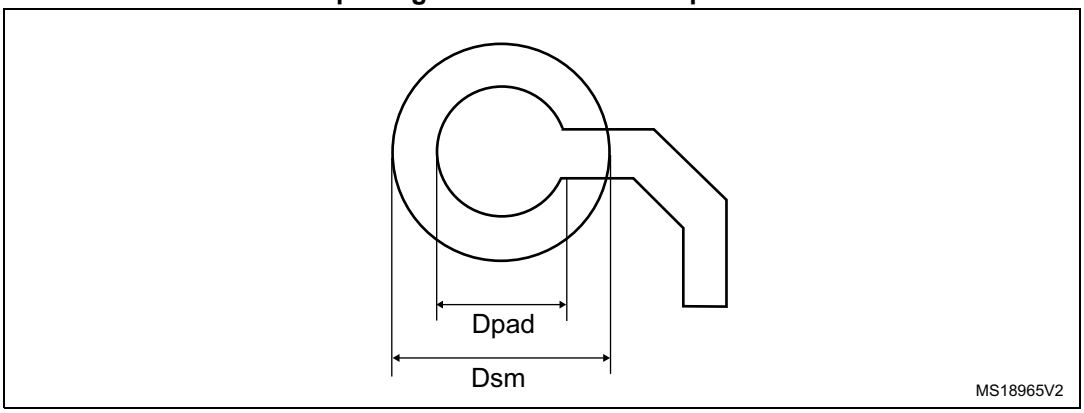
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 80. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.33	-	-	0.013
A1	-	0.10	-	-	0.004	-
A2	-	0.20	-	-	0.008	-
A3	-	0.025[2]	-	-	0.001	-
b	0.16	0.19	0.22	0.006	0.007	0.009
D	2.59	2.61	2.63	0.102	0.103	0.104
E	2.86	2.88	2.90	0.112	0.113	0.114
e	-	0.40	-	-	0.016	-
e1	-	2.00	-	-	0.079	-
e2	-	2.00	-	-	0.079	-
F	-	0.305[3]	-	-	0.012	-
G	-	0.440[3]	-	-	0.017	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

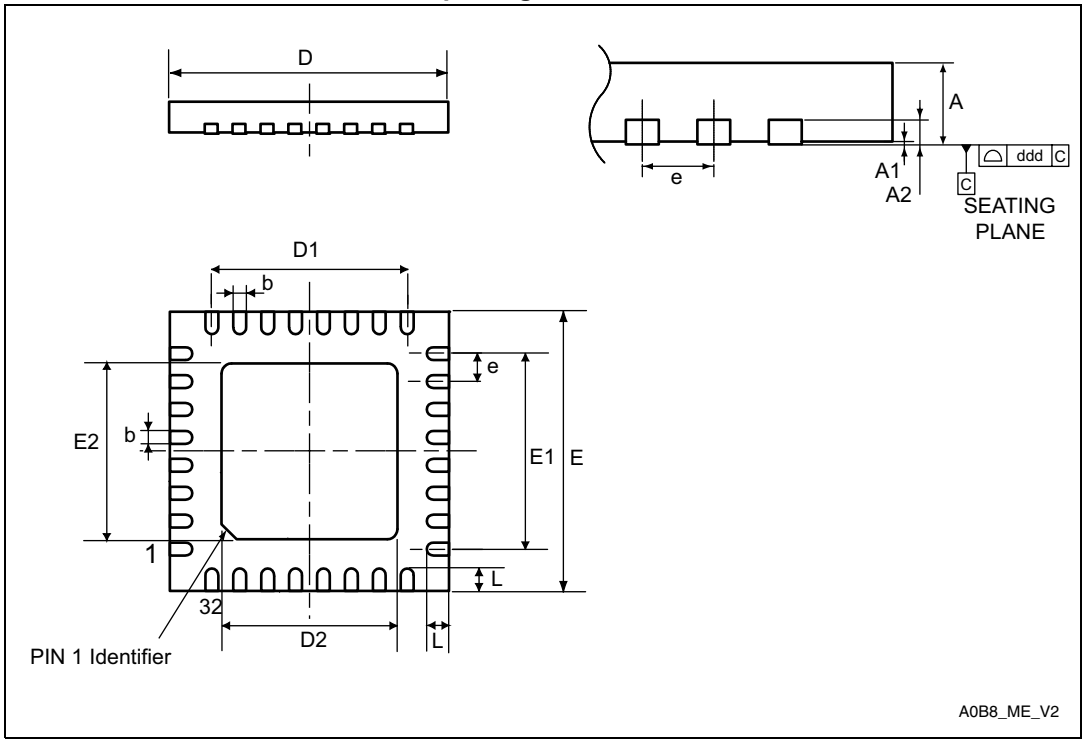
1. Values in inches are converted from mm and rounded to the 3rd decimal place.
2. Back side coating. Nominal dimension rounded to the 3rd decimal place results from process capability.
3. Calculated dimensions are rounded to 3rd decimal place.

Figure 50. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



7.7 UFQFPN32 package information

Figure 54. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 86. Document revision history (continued)

Date	Revision	Changes
25-Jun-2014	3	Cover page: changed LQFP32 size, updated core speed. updated core speed, added minimum supply voltage for ADC and comparators. ADC now guaranteed down to 1.65 V. Updated list of applications in *Section 1: Introduction*. Changed number of I2S interfaces to one in *Section 2: Description*. Updated *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*. Updated *Table 3: Functionalities depending on the operating power supply range*. Updated RTC/TIM21 in *Table 6: STM32L0xx peripherals interconnect matrix*. Added note related to UFQFPN32 and note related to WLCSP36 in *Table 15: STM32L051x6/8 pin definitions*. Split LQFP32/UFQFPN32 pinout schematics into two distinct figures: *Figure 7* and *Figure 8*. Updated V_{DDA} in *Table 23: General operating conditions*. Split Table *Current consumption in Run mode, code with data processing running from Flash* into *Table 27* and *Table 28* and content updated. Split Table *Current consumption in Run mode, code with data processing running from RAM* into *Table 29* and *Table 30* and content updated. Updated *Table 31: Current consumption in Sleep mode*, *Table 32: Current consumption in Low-power run mode*, *Table 33: Current consumption in Low-power sleep mode*, *Table 34: Typical and maximum current consumptions in Stop mode*, *Table 35: Typical and maximum current consumptions in Standby mode*, and added *Table 36: Average current consumption during Wakeup*. Updated *Table 37: Peripheral current consumption in Run or Sleep mode* and added *Table 38: Peripheral current consumption in Stop and Standby mode*. Updated t_{LOCK} in *Table 47: PLL characteristics*. Removed note 1 below *Figure 21: HSE oscillator circuit diagram*. Updated *Table 49: Flash memory and data EEPROM characteristics* and *Table 50: Flash memory and data EEPROM endurance and retention*. Updated *Table 58: I/O AC characteristics*. Updated *Table 60: ADC characteristics*. Updated *Figure 57: Thermal resistance* and added note 1.