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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051r8t6 |

**Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1]**

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | | Standby | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Wakeup capability | | Wakeup capability |
| High Speed External (HSE) | O | O | O | O | -- | | -- | |
| Low Speed Internal (LSI) | O | O | O | O | O | | O | |
| Low Speed External (LSE) | O | O | O | O | O | | O | |
| Multi-Speed Internal (MSI) | O | O | Y | Y | -- | | -- | |
| Inter-Connect Controller | Y | Y | Y | Y | Y | | -- | |
| RTC | O | O | O | O | O | O | O | |
| RTC Tamper | O | O | O | O | O | O | O | O |
| Auto WakeUp (AWU) | O | O | O | O | O | O | O | O |
| USART | O | O | O | O | O[3] | O | -- | |
| LPUART | O | O | O | O | O[3] | O | -- | |
| SPI | O | O | O | O | -- | | -- | |
| I2C | O | O | O | O | O[4] | O | -- | |
| ADC | O | O | -- | -- | -- | | -- | |
| Temperature sensor | O | O | O | O | O | | -- | |
| Comparators | O | O | O | O | O | O | -- | |
| 16-bit timers | O | O | O | O | -- | | -- | |
| LPTIMER | O | O | O | O | O | O | | |
| IWDG | O | O | O | O | O | O | O | O |
| WWDG | O | O | O | O | -- | | -- | |
| SysTick Timer | O | O | O | O | | | -- | |
| GPIOs | O | O | O | O | O | O | | 2 pins |
| Wakeup time to Run mode | 0 µs | 0.36 µs | 3 µs | 32 µs | 3.5 µs | | 50 µs | |

## 3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, LPUART, general-purpose timers, and ADC.

## 3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L051x6/8 device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

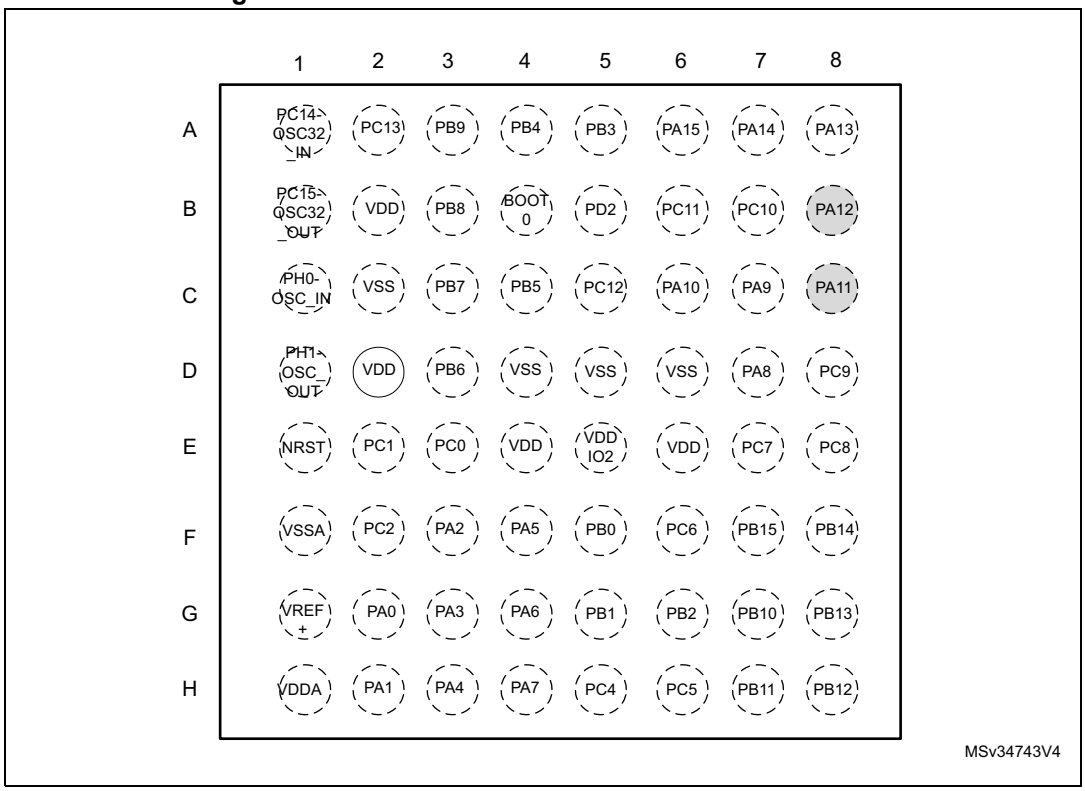
## 3.12 Temperature sensor

The temperature sensor ($T_{SENSE}$) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

**Figure 4. STM32L051x6/8 TFBGA64 ballout - 5x 5 mm**




1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 15. STM32L051x6/8 pin definitions (continued)

| Pin Number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | TFBGA64 | LQFP48 | WLCSP36[1] | LQFP32 | UFQFPN32 | | | | | | |
| 48 | E5 | 36 | - | - | - | VDDIO2 | S | | - | - | - |
| 49 | A7 | 37 | B2 | 24 | 24 | PA14 | I/O | FT | - | SWCLK, USART2_TX | |
| 50 | A6 | 38 | A2 | 25 | 25 | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1 | - |
| 51 | B7 | - | - | - | - | PC10 | I/O | FT | - | LPUART1_TX | - |
| 52 | B6 | - | - | - | - | PC11 | I/O | FT | - | LPUART1_RX | - |
| 53 | C5 | - | - | - | - | PC12 | I/O | FT | - | - | - |
| 54 | B5 | - | - | - | - | PD2 | I/O | FT | - | LPUART1_RTS_DE | - |
| 55 | A5 | 39 | B3 | 26 | 26 | PB3 | I/O | FT | - | SPI1_SCK, TIM2_CH2, EVENTOUT | COMP2_INN |
| 56 | A4 | 40 | A3 | 27 | 27 | PB4 | I/O | FT | - | SPI1_MISO, EVENTOUT, TIM22_CH1 | COMP2_INP |
| 57 | C4 | 41 | C4 | 28 | 28 | PB5 | I/O | FT | - | SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2 | COMP2_INP |
| 58 | D3 | 42 | B4 | 29 | 29 | PB6 | I/O | FTf | - | USART1_TX, I2C1_SCL, LPTIM1_ETR | COMP2_INP |
| 59 | C3 | 43 | A4 | 30 | 30 | PB7 | I/O | FTf | - | USART1_RX, I2C1_SDA, LPTIM1_IN2 | COMP2_INP, PVD_IN |
| 60 | B4 | 44 | C5 | 31 | 31 | BOOT0 | B | | - | - | - |
| 61 | B3 | 45 | B5 | - | 32 | PB8 | I/O | FTf | - | I2C1_SCL | - |
| 62 | A3 | 46 | - | - | - | PB9 | I/O | FTf | - | EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS | - |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.6 V (for the 1.65 V ≤$V_{DD}$ ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

**Figure 10. Pin loading conditions**

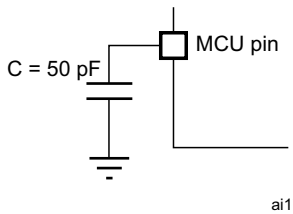



**Figure 11. Pin input voltage**

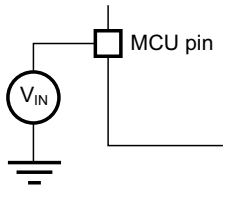


**Table 21. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ (2) | Total current into sum of all $V_{DD}$ power lines (source)(1) | 105 | mA |
| $\Sigma I_{VSS}$ (2) | Total current out of sum of all $V_{SS}$ ground lines (sink)(1) | 105 | |
| $\Sigma I_{VDDIO2}$ | Total current into $V_{DDIO2}$ power line (source) | 25 | |
| $I_{VDD(PIN)}$ | Maximum current into each $V_{DD}$ power pin (source)(1) | 100 | |
| $I_{VSS(PIN)}$ | Maximum current out of each $V_{SS}$ ground pin (sink)(1) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin except FTf pins | 16 | |
| | Output current sunk by FTf pins | 22 | |
| | Output current sourced by any I/O and control pin | -16 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2) | 90 | |
| | Total output current sunk by PA11 and PA12 | 25 | |
| | Total output current sourced by sum of all IOs and control pins(2) | -90 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FTf, RST and B pins | -5/+0(3) | |
| | Injected current on TC pin | ± 5(4) | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 20* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 22. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

### 6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 23*.

**Table 24. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$(1) | $V_{DD}$ rise time rate | BOR detector enabled | 0 | - | ∞ | µs/V |
| | | BOR detector disabled | 0 | - | 1000 | |
| | $V_{DD}$ fall time rate | BOR detector enabled | 20 | - | ∞ | |
| | | BOR detector disabled | 0 | - | 1000 | |
| $T_{RSTTEMPO}$(1) | Reset temporization | $V_{DD}$ rising, BOR enabled | - | 2 | 3.3 | ms |
| | | $V_{DD}$ rising, BOR disabled(2) | 0.4 | 0.7 | 1.6 | |
| $V_{POR/PDR}$ | Power-on/power down reset threshold | Falling edge | 1 | 1.5 | 1.65 | V |
| | | Rising edge | 1.3 | 1.5 | 1.65 | |
| $V_{BOR0}$ | Brown-out reset threshold 0 | Falling edge | 1.67 | 1.7 | 1.74 | |
| | | Rising edge | 1.69 | 1.76 | 1.8 | |
| $V_{BOR1}$ | Brown-out reset threshold 1 | Falling edge | 1.87 | 1.93 | 1.97 | |
| | | Rising edge | 1.96 | 2.03 | 2.07 | |
| $V_{BOR2}$ | Brown-out reset threshold 2 | Falling edge | 2.22 | 2.30 | 2.35 | |
| | | Rising edge | 2.31 | 2.41 | 2.44 | |
| $V_{BOR3}$ | Brown-out reset threshold 3 | Falling edge | 2.45 | 2.55 | 2.6 | |
| | | Rising edge | 2.54 | 2.66 | 2.7 | |
| $V_{BOR4}$ | Brown-out reset threshold 4 | Falling edge | 2.68 | 2.8 | 2.85 | |
| | | Rising edge | 2.78 | 2.9 | 2.95 | |
| $V_{PVD0}$ | Programmable voltage detector threshold 0 | Falling edge | 1.8 | 1.85 | 1.88 | |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| $V_{PVD1}$ | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| $V_{PVD2}$ | PVD threshold 2 | Falling edge | 2.20 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| $V_{PVD3}$ | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| $V_{PVD4}$ | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| $V_{PVD5}$ | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |

**Table 24. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | V |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| $V_{hyst}$ | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 26* are based on characterization results, unless otherwise specified.

**Table 25. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C $V_{DDA}$= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 26. Embedded internal reference voltage(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$(2) | Internal reference voltage | – 40 °C < $T_J$ < +125 °C | 1.202 | 1.224 | 1.242 | V |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ and $V_{REF+}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REFINT}$ value(3) | Including uncertainties due to ADC and $V_{DDA}$/$V_{REF+}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(4) | Temperature coefficient | –40 °C < $T_J$ < +125 °C | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$(4) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(4) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(4)(5) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$(4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(4) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(4) | VREF_OUT output current(6) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(4) | VREF_OUT output load | - | - | - | 50 | pF |

**Table 26. Embedded internal reference voltage(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LPBUF}$(4) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(4) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(4) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(4) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Refer to *Table 38: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption ($I_{REFINT}$).
2. Guaranteed by test in production.
3. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 40: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 47*, *Table 23* and *Table 24* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

**Table 29. Current consumption in Run mode, code with data processing running from RAM**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from RAM) | Supply current in Run mode, code executed from RAM, Flash switched off | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 1 MHz | 135 | 170 | µA |
| | | | | 2 MHz | 240 | 270 | |
| | | | | 4 MHz | 450 | 480 | |
| | | | Range 2, $V_{CORE}$=1.5 ,V, VOS[1:0]=10 | 4 MHz | 0.52 | 0.6 | mA |
| | | | | 8 MHz | 1 | 1.2 | |
| | | | | 16 MHz | 2 | 2.3 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 8 MHz | 1.25 | 1.4 | |
| | | | | 16 MHz | 2.45 | 2.8 | |
| | | | | 32 MHz | 5.1 | 5.4 | |
| | | MSI clock | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 65 kHz | 34.5 | 75 | µA |
| | | | | 524 kHz | 83 | 120 | |
| | | | | 4.2 MHz | 485 | 540 | |
| | | HSI16 clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10 | 16 MHz | 2.1 | 2.3 | mA |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 32 MHz | 5.1 | 5.6 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 30. Current consumption in Run mode vs code type, code with data processing running from RAM(1)**

| Symbol | Parameter | Conditions | | | $f_{HCLK}$ | Typ | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from RAM) | Supply current in Run mode, code executed from RAM, Flash switched off | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | Dhrystone | 4 MHz | 450 | µA |
| | | | | CoreMark | | 575 | |
| | | | | Fibonacci | | 370 | |
| | | | | while(1) | | 340 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | Dhrystone | 32 MHz | 5.1 | mA |
| | | | | CoreMark | | 6.25 | |
| | | | | Fibonacci | | 4.4 | |
| | | | | while(1) | | 4.7 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 37. Peripheral current consumption in Run or Sleep mode(1) (continued)**

| Peripheral | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|
| | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| All enabled | 283 | 225 | 222.5 | 212.5 | µA/MHz ($f_{HCLK}$) |
| PWR | 2.5 | 2 | 2 | 1 | µA/MHz ($f_{HCLK}$) |

1. Data based on differential $I_{DD}$ measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: $f_{HCLK}$ = 32 MHz (range 1), $f_{HCLK}$ = 16 MHz (range 2), $f_{HCLK}$ = 4 MHz (range 3), $f_{HCLK}$ = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

**Table 38. Peripheral current consumption in Stop and Standby mode(1)**

| Symbol | Peripheral | Typical consumption, $T_A$ = 25 °C | | Unit |
|---|---|---|---|---|
| | | $V_{DD}$=1.8 V | $V_{DD}$=3.0 V | |
| $I_{DD(PVD / BOR)}$ | - | 0.7 | 1.2 | µA |
| $I_{REFINT}$ | - | - | 1.4 | |
| - | LSE Low drive(2) | 0,1 | 0,1 | |
| - | LPTIM1, Input 100 Hz | 0,01 | 0,01 | |
| - | LPTIM1, Input 1 MHz | 6 | 6 | |
| - | LPUART1 | 0,2 | 0,2 | |
| - | RTC | 0,3 | 0,48 | |

1. LPTIM peripheral cannot operate in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

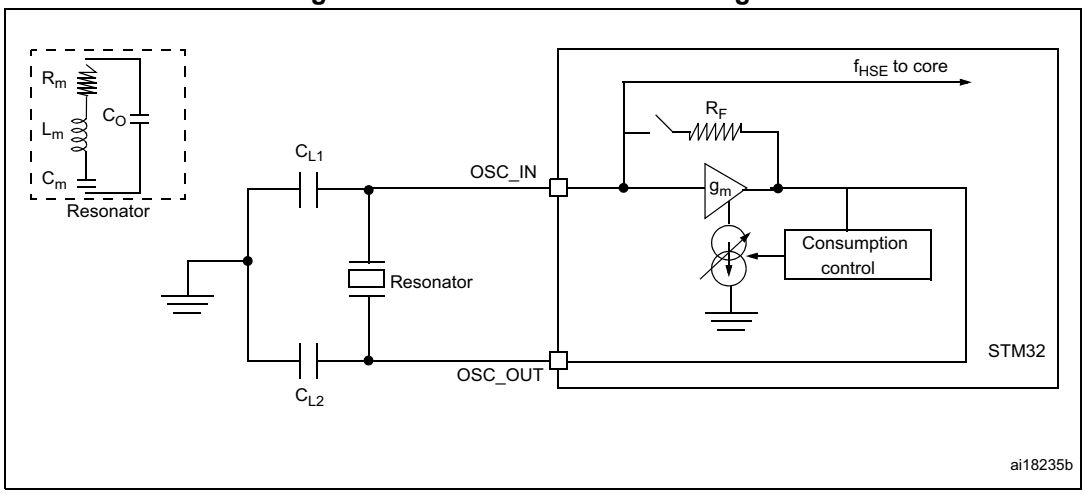
**Table 42. HSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 1 | | 25 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $G_m$ | Maximum critical crystal transconductance | Startup | - | - | 700 | µA /V |
| $t_{SU(HSE)}$ (2) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

**Figure 21. HSE oscillator circuit diagram**



## 6.3.7 Internal clock source characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

### High-speed internal 16 MHz (HSI16) RC oscillator

**Table 44. 16 MHz HSI16 oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI16}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |
| $TRIM^{(1)(2)}$ | HSI16 user-trimmed resolution | Trimming code is not a multiple of 16 | - | ±0.4 | 0.7 | % |
| | | Trimming code is a multiple of 16 | - | - | ±1.5 | % |
| $ACC_{HSI16}$ (2) | Accuracy of the factory-calibrated HSI16 oscillator | $V_{DDA}$ = 3.0 V, $T_A$ = 25 °C | -1(3) | - | 1(3) | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = 0 to 55 °C | -1.5 | - | 1.5 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 70 °C | -2 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 85 °C | -2.5 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 105 °C | -4 | - | 2 | % |
| | | $V_{DDA}$ = 1.65 V to 3.6 V<br>$T_A$ = − 40 to 125 °C | -5.45 | - | 3.25 | % |
| $t_{SU(HSI16)}^{(2)}$ | HSI16 oscillator startup time | - | - | 3.7 | 6 | µs |
| $I_{DD(HSI16)}^{(2)}$ | HSI16 oscillator power consumption | - | - | 100 | 140 | µA |

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

**Figure 23. HSI16 minimum and maximum value versus temperature**

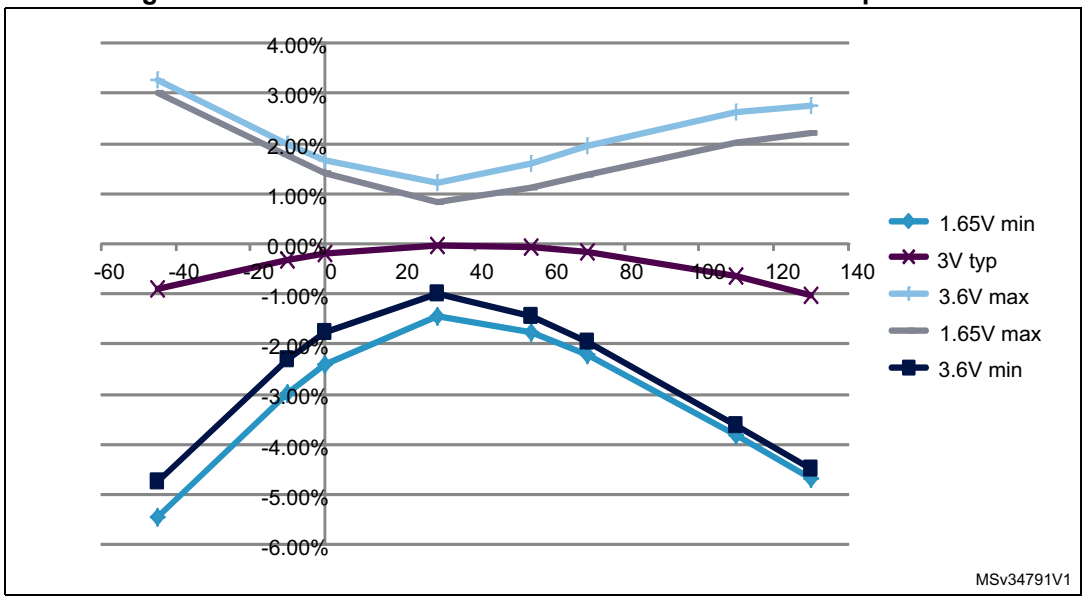


**Table 49. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 500 | 700 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 50. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 100 | |
| | Cycling (erase / write) Program memory | $T_A$ = -40°C to 125 °C | 0.2 | |
| | Cycling (erase / write) EEPROM data memory | | 2 | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | years |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 85 °C | | 30 | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 105 °C | | | |
| | Data retention (program memory) after 200 cycles at $T_A$ = 125 °C | $T_{RET}$ = +125 °C | | |
| | Data retention (EEPROM data memory) after 2 kcycles at $T_A$ = 125 °C | | | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

## 6.3.18 Timer characteristics

### TIM timer characteristics

The parameters given in the *Table 67* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 67. TIMx characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 31.25 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 32 MHz | 0 | 16 | MHz |
| $Res_{TIM}$ | Timer resolution | - | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 0.0312 | 2048 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | - | 134.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

## 6.3.19 Communications interfaces

### $I^2C$ interface characteristics

The $I^2C$ interface meets the timings requirements of the $I^2C$-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The $I^2C$ timing requirements are guaranteed by design when the $I^2C$ peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All $I^2C$ SDA and SCL I/Os embed an analog filter (see *Table 68* for the analog filter characteristics).

The analog spike filter is compliant with $I^2C$ timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤$V_{DD}$ ≤3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V ≤$V_{DD}$ ≤3.6 V and voltage scaling Range 1 or Range 2.
  - $V_{DD}$ < 2 V, voltage scaling Range 1 or Range 2, $C_{load}$ < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

*Note: In Standard mode, no spike filter is required.*

**Table 68. I2C analog filter characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | Range 1 | 50(2) | 260(3) | ns |
| | | Range 2 | | - | |
| | | Range 3 | | - | |

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

## USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

**Table 69. USART/LPUART characteristics**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUUSART}$ | Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when the USART/LPUART is clocked by HSI | Stop mode with main regulator in Run mode, Range 2 or 3 | - | 8.7 | µs |
| | | Stop mode with main regulator in Run mode, Range 1 | - | 8.1 | |
| | | Stop mode with main regulator in low-power mode, Range 2 or 3 | - | 12 | |
| | | Stop mode with main regulator in low-power mode, Range 1 | - | 11.4 | |

**Table 71. SPI characteristics in voltage Range 2 (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | - | 8 | MHz |
| | | Slave mode Transmitter $1.65<V_{DD}<3.6V$ | | | 8 | |
| | | Slave mode Transmitter $2.7<V_{DD}<3.6V$ | | | 8(2) | |
| $Duty_{(SCK)}$ | Duty cycle of SPI clock frequency | Slave mode | 30 | 50 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode | Tpclk-2 | Tpclk | Tpclk+2 | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 0 | - | - | |
| $t_{su(SI)}$ | | Slave mode | 3 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 11 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 4.5 | - | - | |
| $t_{a(SO}$ | Data output access time | Slave mode | 18 | - | 52 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 12 | - | 42 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode | - | 20 | 56.5 | |
| $t_{v(MO)}$ | | Master mode | - | 5 | 9 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode | 13 | - | - | |
| $t_{h(MO)}$ | | Master mode | 3 | - | - | |

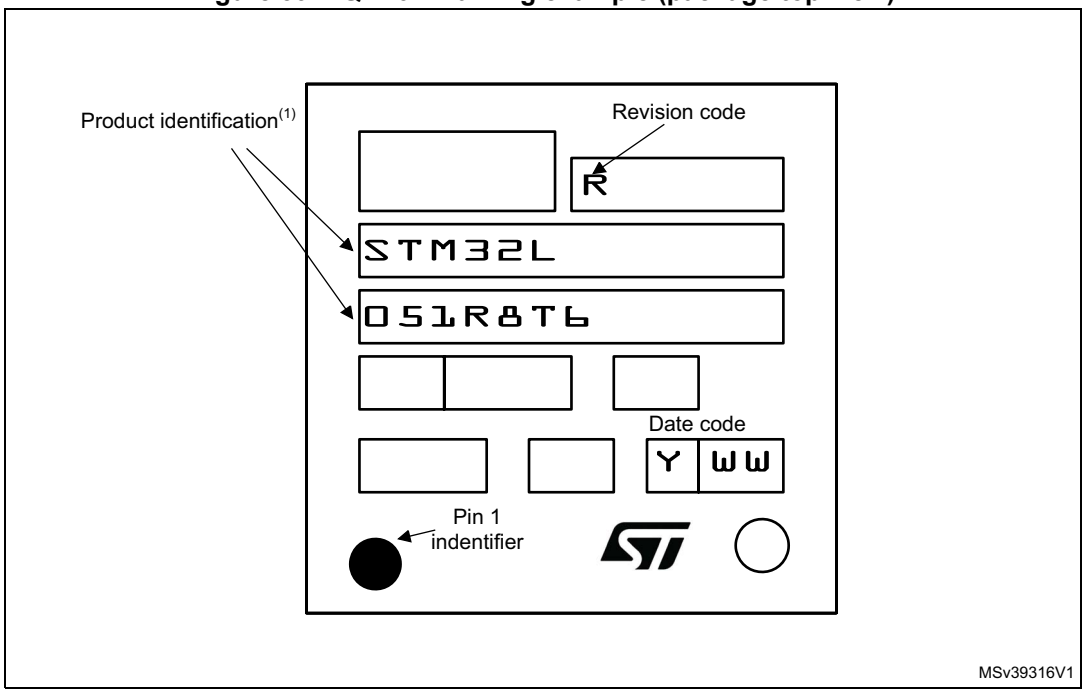
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

### Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 39. LQFP64 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 86. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 05-Sep-2014 | 4 | Extended operating temperature range to 125 °C.<br>Updated minimum ADC operating voltage to 1.65 V.<br>Updated *Section 3.4.1: Power supply schemes*.<br>Replaced USART3 by LPUART1 and updated I/O structure for PC5 and PC15 pins in *Table 15: STM32L051x6/8 pin definitions*.<br>Replaced LPUART by LPUART1 in *Table 16: Alternate function port A*, *Table 17: Alternate function port B*, *Table 18: Alternate function port C* and *Table 19: Alternate function port D*.<br>Updated temperature range in *Section 2: Description*, *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*.<br>Updated $P_D$, $T_{A\ and}$ $T_J$ to add range 3 in *Table 23: General operating conditions*. Added range 3 in *Table 50: Flash memory and data EEPROM endurance and retention*, *Table 85: STM32L051x6/8 ordering information scheme*. Update note 1 in *Table 27: Current consumption in Run mode, code with data processing running from Flash*, *Table 29: Current consumption in Run mode, code with data processing running from RAM*, *Table 31: Current consumption in Sleep mode*, *Table 32: Current consumption in Low-power run mode*, *Table 33: Current consumption in Low-power sleep mode*, *Table 34: Typical and maximum current consumptions in Stop mode*, *Table 35: Typical and maximum current consumptions in Standby mode* and *Table 39: Low-power mode wakeup timings*. Updated *Figure 57: Thermal resistance* and removed note 1. Updated *Table 60: ADC characteristics* and *Table 62: ADC accuracy*.<br>Updated *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive*, *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*.<br>Updated *Table 35: Typical and maximum current consumptions in Standby mode*.<br>Updated SYSCFG in *Table 37: Peripheral current consumption in Run or Sleep mode*.<br>Updated *Table 38: Peripheral current consumption in Stop and Standby mode* and *Table 39: Low-power mode wakeup timings*.<br>Updated $ACC_{HSI16}$ temperature conditions in *Table 44: 16 MHz HSI16 oscillator characteristics*.<br>Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in *Table 59: NRST pin characteristics*.<br>Updated *Table 60: ADC characteristics* and *Table 62: ADC accuracy*.<br>Added range 3 in *Table 85: STM32L051x6/8 ordering information scheme*. |

**Table 86. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 17-Mar-2016 | 6 | Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*.<br>Changed minimum comparator supply voltage to 1.65 V on cover page.<br>Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*.<br>Updated *Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.16.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.<br>Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.16.3: Low-power universal asynchronous receiver transmitter (LPUART)*.<br>In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization.<br>Changed $V_{DDA}$ minimum value to 1.65 V in *Table 23: General operating conditions*.<br>*Section 6.3.15: 12-bit ADC characteristics*:<br>– *Table 60: ADC characteristics*:<br>Distinction made between $V_{DDA}$ for fast and standard channels; added note *1.*<br>Added note 4 related to $R_{ADC}$.<br>Updated $f_{TRIG}$ and $V_{AIN}$ maximum value.<br>Updated $t_S$ and $t_{CONV}$.<br>Added $V_{REF+}$.<br>– Updated equation 1 description.<br>– Updated *Table 61: RAIN max for fADC = 16 MHz* for $f_{ADC}$ = 16 MHz and distinction made between fast and standard channels.<br>Added *Table 69: USART/LPUART characteristics*.<br>Updated *Figure 45: LQFP48 marking example (package top view)*. |