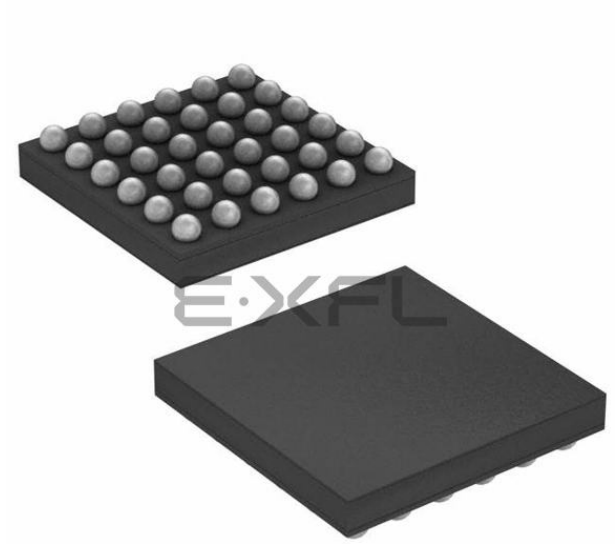

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 29 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-UFBGA, WLCSP |
| Supplier Device Package | 36-WLCSP (2.61x2.88) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l051t8y7dtr |

## 2.1 Device overview

**Table 2. Ultra-low-power STM32L051x6/x8 device features and peripheral counts**

| Peripheral | | STM32 L051K6 | STM32L 051T6 | STM32 L051C6 | STM32 L051R6 | STM32 L051K8 | STM32L 051T8 | STM32 L051C8 | STM32 L051R8 |
|---|---|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 32 | | | | 64 | | | |
| Data EEPROM (Kbytes) | | 2 | | | | 2 | | | |
| RAM (Kbytes) | | 8 | | | | 8 | | | |
| Timers | General-purpose | 3 | | | | 3 | | | |
| | Basic | 1 | | | | 1 | | | |
| | LPTIMER | 1 | | | | 1 | | | |
| RTC/SYSTICK/IWDG/ WWDG | | 1/1/1/1 | | | | 1/1/1/1 | | | |
| Communi-cation interfaces | SPI/I2S | 3(2)[1]/0 | 3(2)[1]/0 | 4(2)[1]/1 | 4(2)[1]/1 | 3(2)[1]/0 | 3(2)[1]/0 | 4(2)[1]/1 | 4(2)[1]/1 |
| | $I^2C$ | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | USART | 2 | | | | 2 | | | |
| | LPUART | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| GPIOs | | 27[2] | 29 | 37 | 51[3] | 27[2] | 29 | 37 | 51[3] |
| Clocks: HSE/LSE/HSI/MSI/LSI | | 0/1/1/1/1 | 0/1/1/1/1 | 1/1/1/1/1 | 1/1/1/1/1 | 0/1/1/1/1 | 0/1/1/1/1 | 1/1/1/1/1 | 1/1/1/1/1 |
| 12-bit synchronized ADC Number of channels | | 1<br>10 | 1<br>10 | 1<br>10 | 1<br>16[3] | 1<br>10 | 1<br>10 | 1<br>10 | 1<br>16[3] |
| Comparators | | 2 | | | | 2 | | | |
| Max. CPU frequency | | 32 MHz | | | | | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option<br>1.65 V to 3.6 V without BOR option | | | | | | | |
| Operating temperatures | | Ambient temperature: –40 to +125 °C<br>Junction temperature: –40 to +130 °C | | | | | | | |
| Packages | | LQFP32, UFQFPN 32 | WLCSP 36 | LQFP48 | LQFP64 TFBGA 64 | LQFP32, UFQFPN 32 | WLCSP 36 | LQFP48 | LQFP64 TFBGA 64 |

1. 2 SPI interfaces are USARTs operating in SPI master mode.
2. LQFP32 has two GPIOs, less than UFQFPN32 (27).
3. TFBGA64 has one GPIO, one ADC input and one capacitive sensing channel less than LQFP64.

## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

**Table 6. STM32L0xx peripherals interconnect matrix (continued)**

| Interconnect source | Interconnect destination | Interconnect action | Run | Sleep | Low-power run | Low-power sleep | Stop |
|---|---|---|---|---|---|---|---|
| RTC | TIM21 | Timer triggered by Auto wake-up | Y | Y | Y | Y | - |
| | LPTIM | Timer triggered by RTC event | Y | Y | Y | Y | Y |
| All clock source | TIMx | Clock source used as input channel for RC measurement and trimming | Y | Y | Y | Y | - |
| GPIO | TIMx | Timer input channel and trigger | Y | Y | Y | Y | - |
| | LPTIM | Timer input channel and trigger | Y | Y | Y | Y | Y |
| | ADC | Conversion trigger | Y | Y | Y | Y | - |

## 3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L051x6/8 are compatible with all ARM tools and software.

#### Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L051x6/8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.4 Reset and supply management

### 3.4.1 Power supply schemes

- $V_{DD}$ = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 1.65 to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.

### 3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

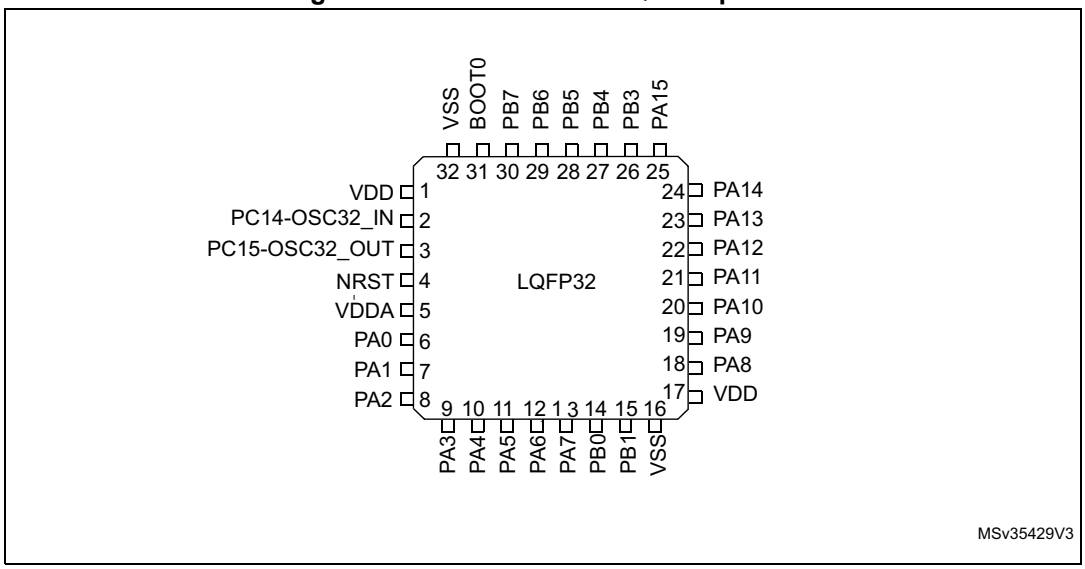
- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the $V_{DD}$ threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on $V_{DD}$ at least 1 ms after it exits the POR area.

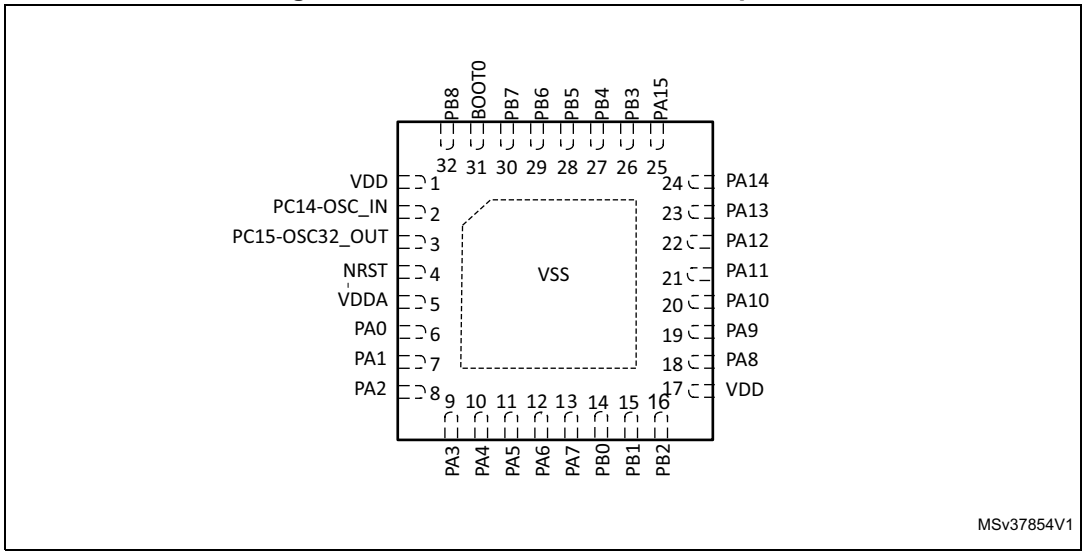
Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

**Figure 7. STM32L051x6/8 LQFP32 pinout**




1. The above figure shows the package top view.

**Figure 8. STM32L051x6/8 UFQFPN32 pinout**




1. The above figure shows the package top view.

**Table 18. Alternate function port C**

| Port | | AF0 | AF1 | AF2 |
|---|---|---|---|---|
| | | LPUART1/LPTIM/TIM21/12/EVENTOUT | - | SPI2/I2S2/LPUART1/EVENTOUT |
| Port C | PC0 | LPTIM1_IN1 | - | EVENTOUT |
| | PC1 | LPTIM1_OUT | - | EVENTOUT |
| | PC2 | LPTIM1_IN2 | - | SPI2_MISO/I2S2_MCK |
| | PC3 | LPTIM1_ETR | - | SPI2_MOSI/I2S2_SD |
| | PC4 | EVENTOUT | - | LPUART1_TX |
| | PC5 | | - | LPUART1_RX |
| | PC6 | TIM22_CH1 | - | - |
| | PC7 | TIM22_CH2 | - | - |
| | PC8 | TIM22_ETR | - | - |
| | PC9 | TIM21_ETR | - | - |
| | PC10 | LPUART1_TX | - | - |
| | PC11 | LPUART1_RX | - | - |
| | PC12 | - | - | - |
| | PC13 | - | - | - |
| | PC14 | - | - | - |
| | PC15 | - | - | - |

**Table 19. Alternate function port D**

| Port | | AF0 | AF1 |
|---|---|---|---|
| | | LPUART1 | - |
| Port D | PD2 | LPUART1_RTS_DE | - |

# 5 Memory mapping

**Figure 9. Memory map**

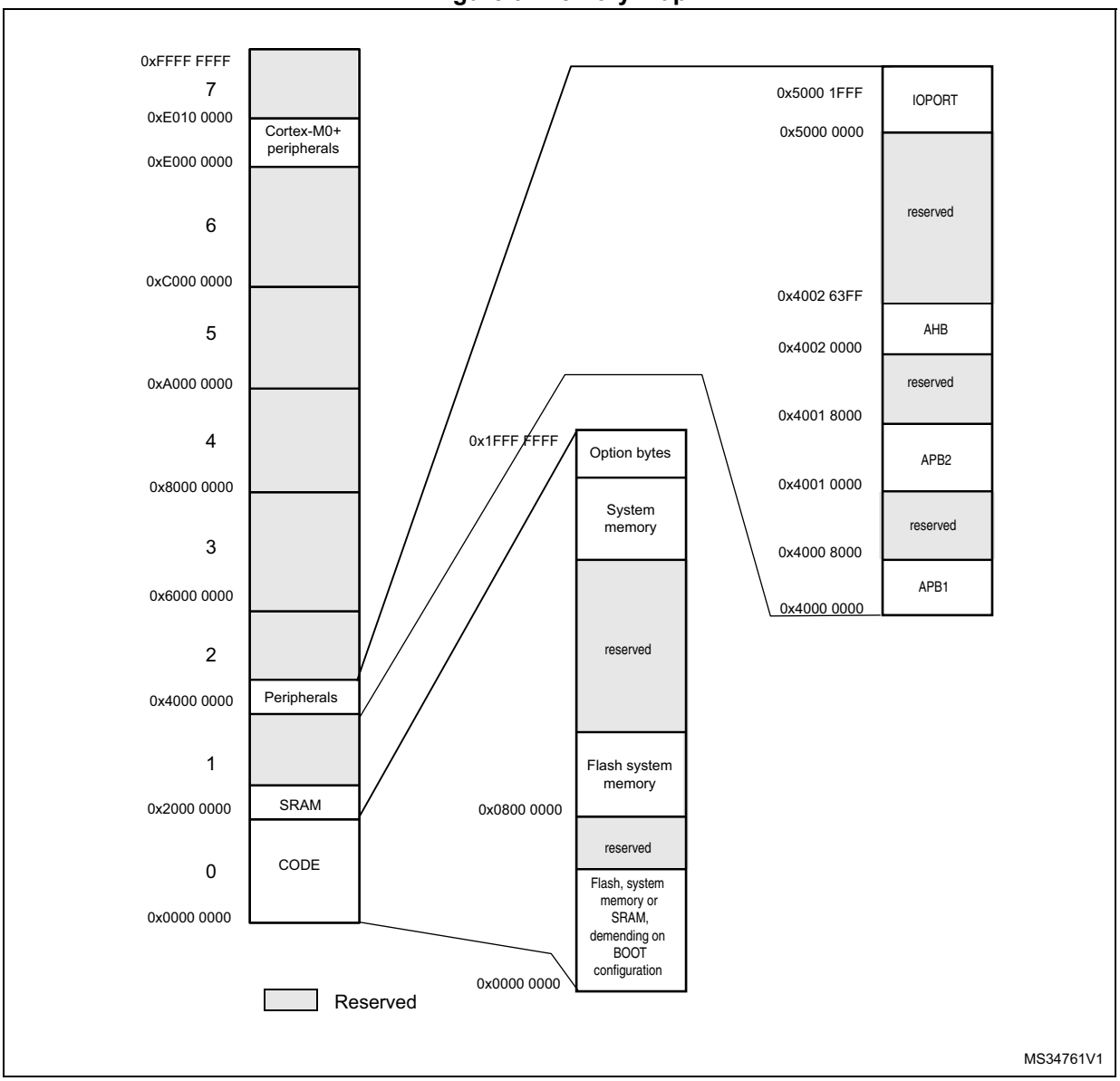


**Table 26. Embedded internal reference voltage(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LPBUF}$(4) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(4) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(4) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(4) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Refer to *Table 38: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption ($I_{REFINT}$).
2. Guaranteed by test in production.
3. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 40: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 47*, *Table 23* and *Table 24* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

**Table 35. Typical and maximum current consumptions in Standby mode**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby) | Supply current in Standby mode | Independent watchdog and LSI enabled | $T_A$ = − 40 to 25°C | 1.3 | 1.7 | µA |
| | | | $T_A$ = 55 °C | - | 2.9 | |
| | | | $T_A$= 85 °C | - | 3.3 | |
| | | | $T_A$ = 105 °C | - | 4.1 | |
| | | | $T_A$ = 125 °C | - | 8.5 | |
| | | Independent watchdog and LSI OFF | $T_A$ = − 40 to 25°C | 0.29 | 0.6 | |
| | | | $T_A$ = 55 °C | 0.32 | 0.9 | |
| | | | $T_A$ = 85 °C | 0.5 | 2.3 | |
| | | | $T_A$ = 105 °C | 0.94 | 3 | |
| | | | $T_A$ = 125 °C | 2.6 | 7 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

**Table 36. Average current consumption during Wakeup**

| Symbol | parameter | System frequency | Current consumption during wakeup | Unit |
|---|---|---|---|---|
| $I_{DD}$ (Wakeup from Stop) | Supply current during Wakeup from Stop mode | HSI | 1 | mA |
| | | HSI/4 | 0,7 | |
| | | MSI clock = 4,2 MHz | 0,7 | |
| | | MSI clock = 1,05 MHz | 0,4 | |
| | | MSI clock = 65 KHz | 0,1 | |
| $I_{DD}$ (Reset) | Reset pin pulled down | - | 0,21 | |
| $I_{DD}$ (Power-up) | BOR ON | - | 0,23 | |
| $I_{DD}$ (Wakeup from StandBy) | With Fast wakeup set | MSI clock = 2,1 MHz | 0,5 | |
| | With Fast wakeup disabled | MSI clock = 2,1 MHz | 0,12 | |

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked OFF
  - with only one peripheral clocked on

**Table 37. Peripheral current consumption in Run or Sleep mode(1)**

| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| APB1 | I2C1 | 11 | 9.5 | 7.5 | 9 | µA/MHz ($f_{HCLK}$) |
| | I2C2 | 4 | 3.5 | 3 | 2.5 | |
| | LPTIM1 | 10 | 8.5 | 6.5 | 8 | |
| | LPUART1 | 8 | 6.5 | 5.5 | 6 | |
| | SPI2 | 9 | 4.5 | 3.5 | 4 | |
| | USART2 | 14.5 | 12 | 9.5 | 11 | |
| | TIM2 | 10.5 | 8.5 | 7 | 9 | |
| | TIM6 | 3.5 | 3 | 2.5 | 2 | |
| | WWDG | 3 | 2 | 2 | 2 | |
| APB2 | ADC1(2) | 5.5 | 5 | 3.5 | 4 | µA/MHz ($f_{HCLK}$) |
| | SPI1 | 4 | 3 | 3 | 2.5 | |
| | USART1 | 14.5 | 11.5 | 9.5 | 12 | |
| | TIM21 | 7.5 | 6 | 5 | 5.5 | |
| | TIM22 | 7 | 6 | 5 | 6 | |
| | FIREWALL | 1.5 | 1 | 1 | 0.5 | |
| | DBGMCU | 1.5 | 1 | 1 | 0.5 | |
| | SYSCFG | 2.5 | 2 | 2 | 1.5 | |
| Cortex-M0+ core I/O port | GPIOA | 3.5 | 3 | 2.5 | 2.5 | µA/MHz ($f_{HCLK}$) |
| | GPIOB | 3.5 | 2.5 | 2 | 2.5 | |
| | GPIOC | 8.5 | 6.5 | 5.5 | 7 | |
| | GPIOD | 1 | 0.5 | 0.5 | 0.5 | |
| AHB | CRC | 1.5 | 1 | 1 | 1 | µA/MHz ($f_{HCLK}$) |
| | FLASH | 0(3) | 0(3) | 0(3) | 0(3) | |
| | DMA1 | 10 | 8 | 6.5 | 8.5 | |

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

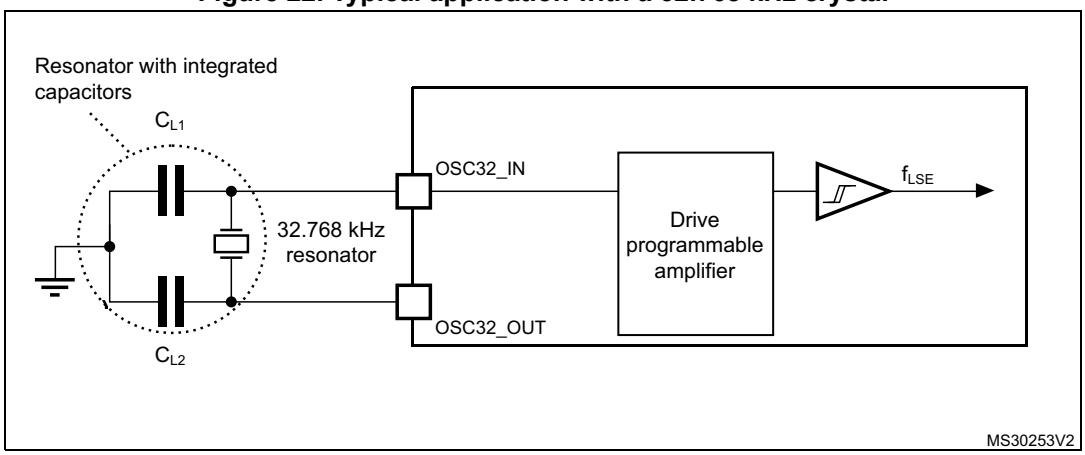
**Table 43. LSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions(2) | Min(2) | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | LSE oscillator frequency | | - | 32.768 | - | kHz |
| $G_m$ | Maximum critical crystal transconductance | LSEDRV[1:0]=00 lower driving capability | - | - | 0.5 | µA/V |
| | | LSEDRV[1:0]= 01 medium low driving capability | - | - | 0.75 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | - | - | 1.7 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 2.7 | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 22. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## 6.3.7 Internal clock source characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

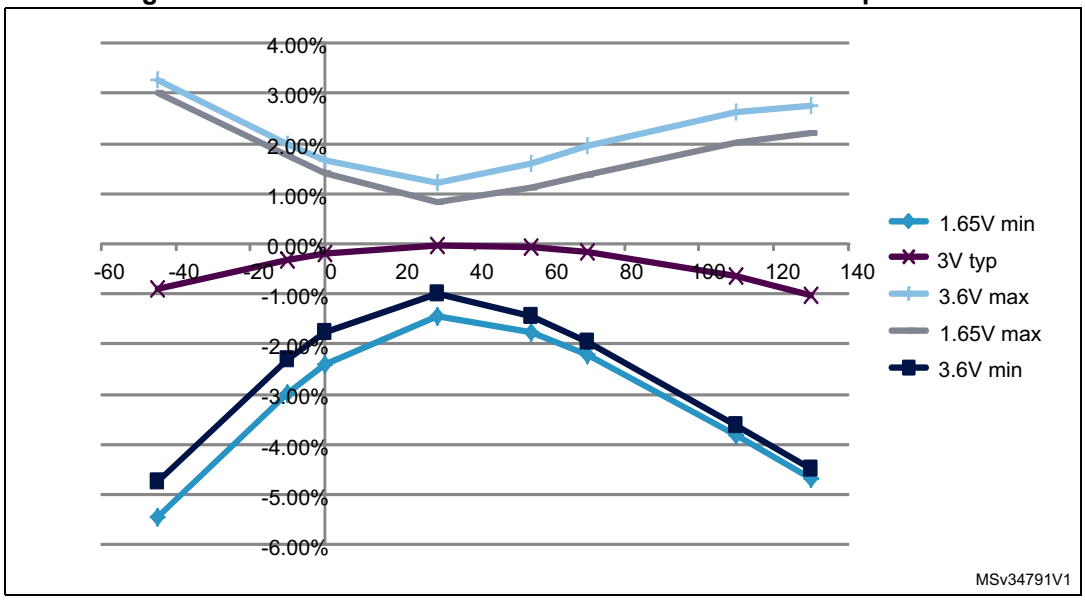
### High-speed internal 16 MHz (HSI16) RC oscillator

**Table 44. 16 MHz HSI16 oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI16}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |
| $TRIM^{(1)(2)}$ | HSI16 user-trimmed resolution | Trimming code is not a multiple of 16 | - | ±0.4 | 0.7 | % |
| | | Trimming code is a multiple of 16 | - | - | ±1.5 | % |
| $ACC_{HSI16}$ (2) | Accuracy of the factory-calibrated HSI16 oscillator | $V_{DDA}$ = 3.0 V, $T_A$ = 25 °C | -1(3) | - | 1(3) | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = 0 to 55 °C | -1.5 | - | 1.5 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 70 °C | -2 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 85 °C | -2.5 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 105 °C | -4 | - | 2 | % |
| | | $V_{DDA}$ = 1.65 V to 3.6 V<br>$T_A$ = − 40 to 125 °C | -5.45 | - | 3.25 | % |
| $t_{SU(HSI16)}^{(2)}$ | HSI16 oscillator startup time | - | - | 3.7 | 6 | µs |
| $I_{DD(HSI16)}^{(2)}$ | HSI16 oscillator power consumption | - | - | 100 | 140 | µA |

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

**Figure 23. HSI16 minimum and maximum value versus temperature**



### SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 70. SPI characteristics in voltage Range 1 (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | - | 16 | MHz |
| | | Slave mode receiver | | | 16 | |
| | | Slave mode Transmitter $1.71<V_{DD}<3.6V$ | - | - | 12(2) | |
| | | Slave mode Transmitter $2.7<V_{DD}<3.6V$ | - | - | 16(2) | |
| $Duty_{(SCK)}$ | Duty cycle of SPI clock frequency | Slave mode | 30 | 50 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode | Tpclk-2 | Tpclk | Tpclk+ 2 | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 0 | - | - | |
| $t_{su(SI)}$ | | Slave mode | 3 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 7 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 3.5 | - | - | |
| $t_{a(SO}$ | Data output access time | Slave mode | 15 | - | 36 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 10 | - | 30 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode $1.65\ V<V_{DD}<3.6\ V$ | - | 18 | 41 | |
| | | Slave mode $2.7\ V<V_{DD}<3.6\ V$ | - | 18 | 25 | |
| $t_{v(MO)}$ | | Master mode | - | 4 | 7 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode | 10 | - | - | |
| $t_{h(MO)}$ | | Master mode | 0 | - | - | |

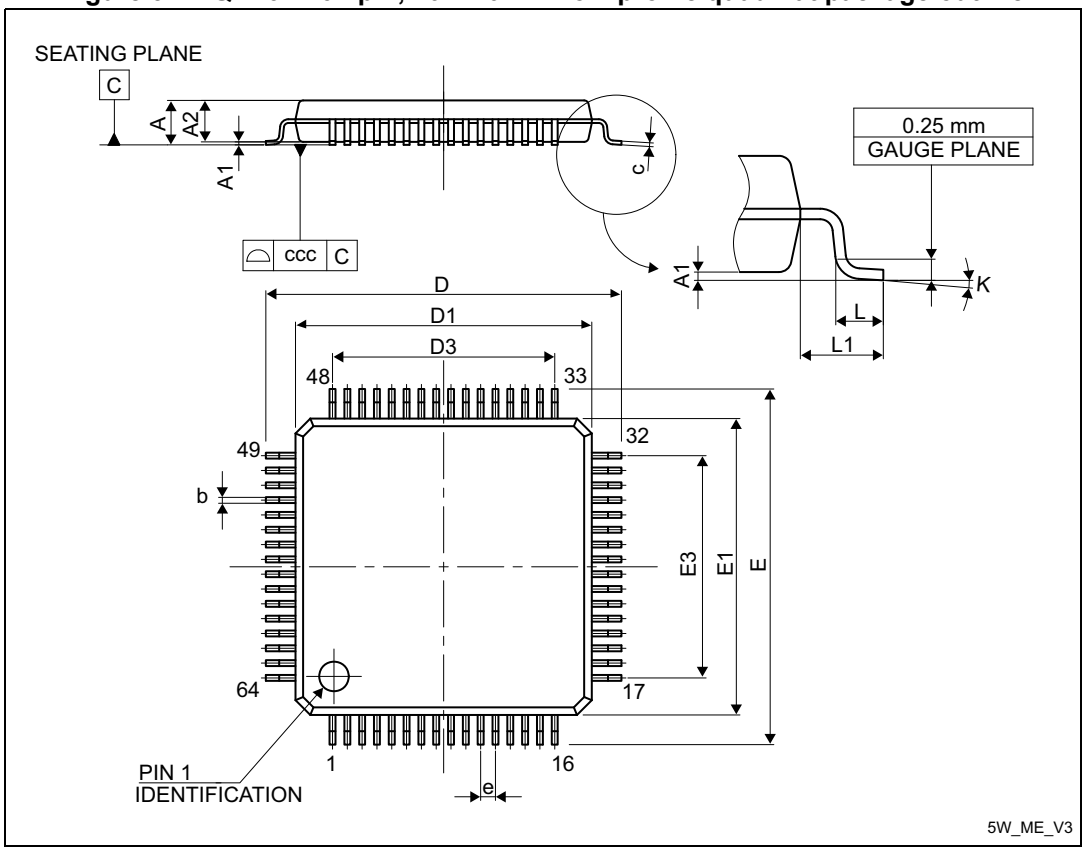
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

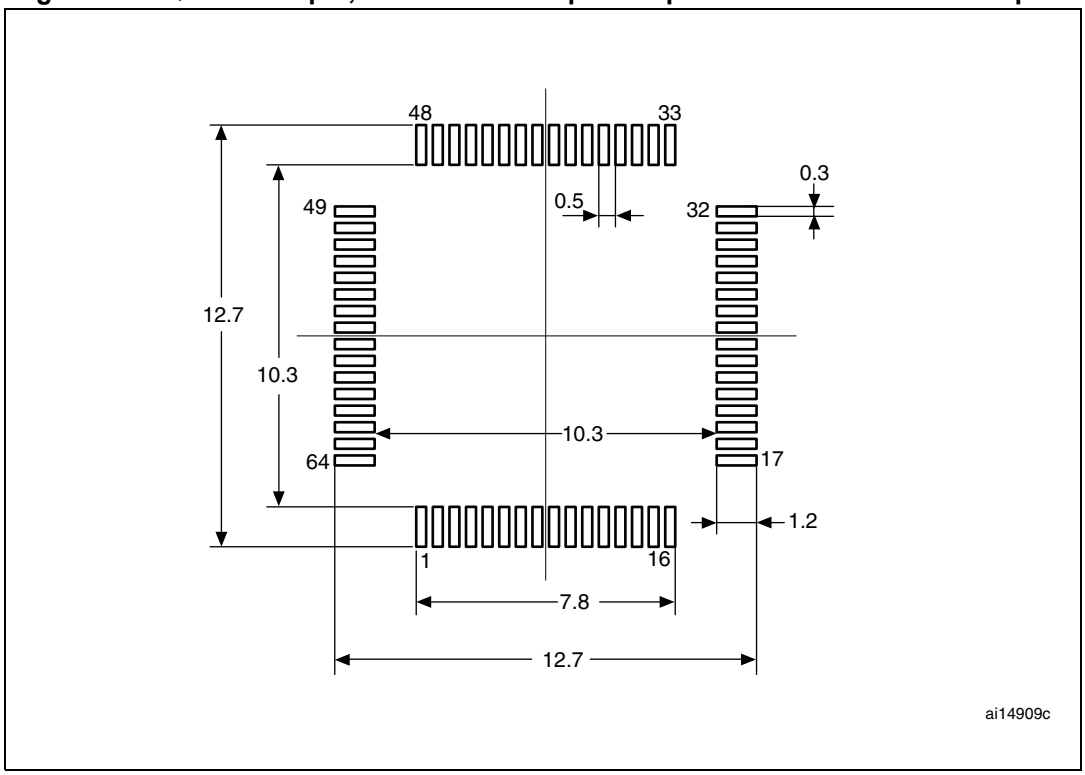
## 7.1 LQFP64 package information

**Figure 37. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint**



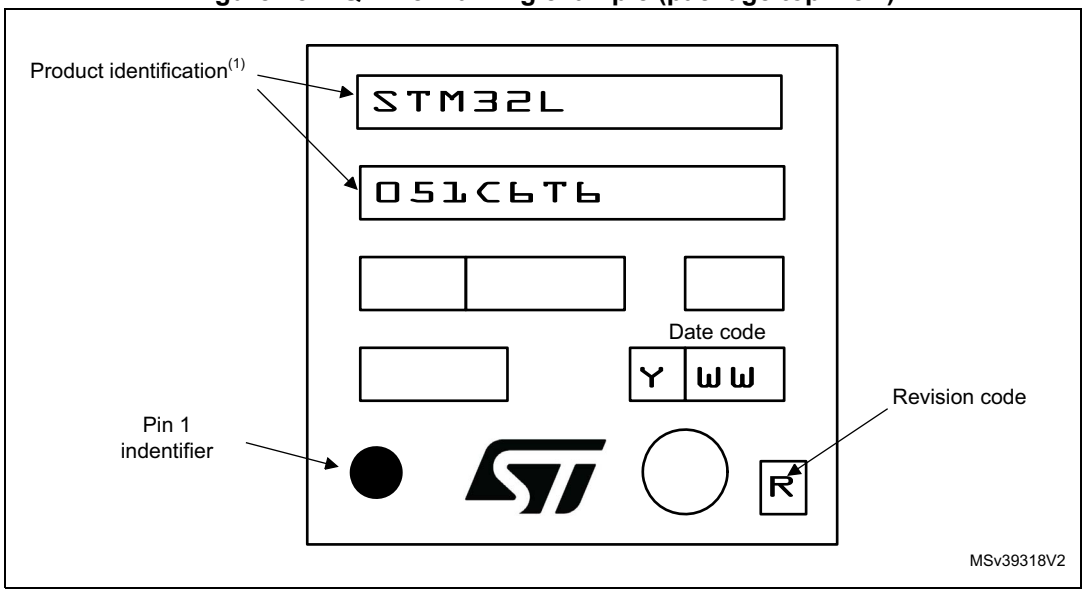

1. Dimensions are expressed in millimeters.

### Device marking for LQFP48

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

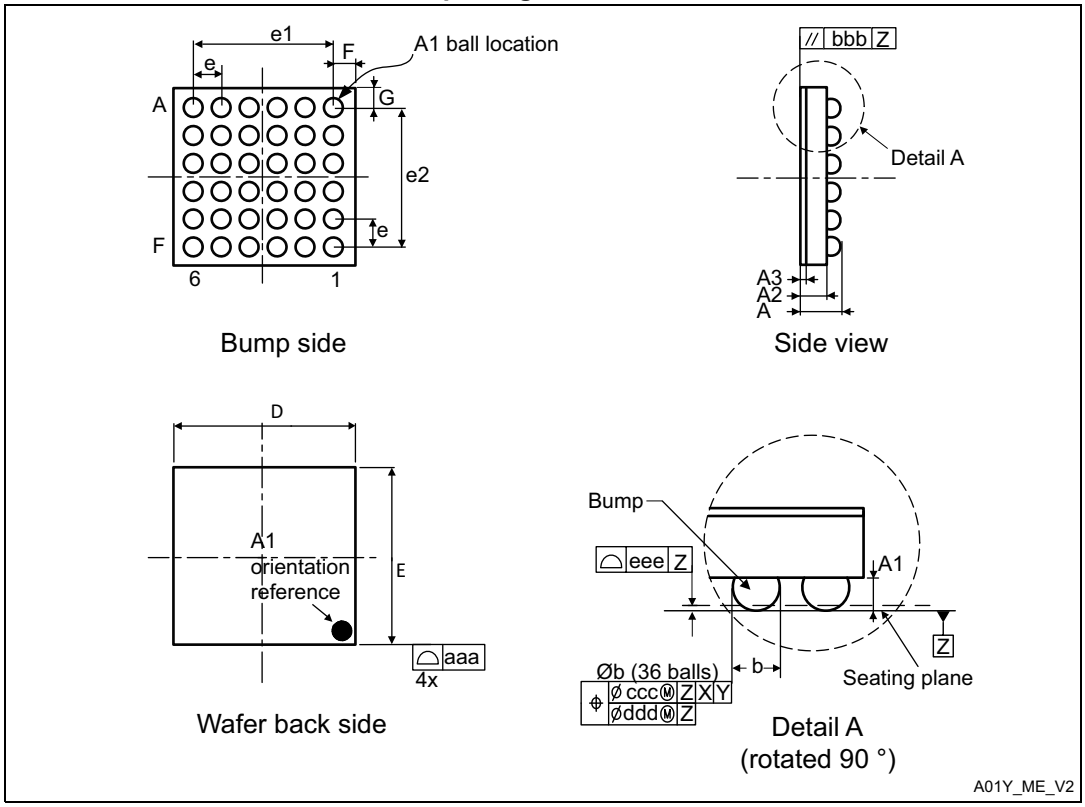
**Figure 45. LQFP48 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.4 Standard WLCSP36 package information

**Figure 46. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline**



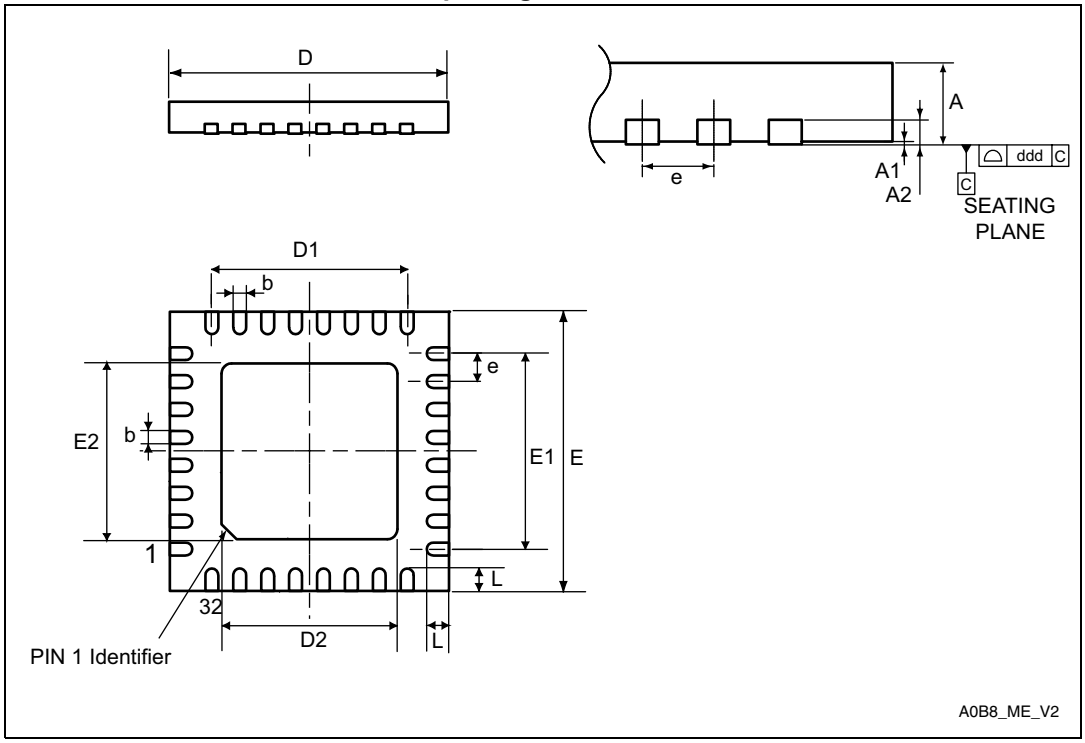

1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z

**Table 78. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 0.59 | - | - | 0.023 |
| A1 | - | 0.18 | - | - | 0.007 | - |
| A2 | - | 0.38 | - | - | 0.015 | - |
| A3 | - | 0.025[2] | - | - | 0.001 | - |
| b | 0.22 | 0.25 | 0.28 | 0.009 | 0.010 | 0.011 |
| D | 2.59 | 2.61 | 2.63 | 0.102 | 0.103 | 0.104 |
| E | 2.86 | 2.88 | 2.90 | 0.112 | 0.113 | 0.114 |
| e | - | 0.40 | - | - | 0.016 | - |
| e1 | - | 2.00 | - | - | 0.079 | - |
| e2 | - | 2.00 | - | - | 0.079 | - |

## 7.7 UFQFPN32 package information

**Figure 54. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline**




1. Drawing is not to scale.

# 8 Part numbering

**Table 85. STM32L051x6/8 ordering information scheme**

Example: STM32 L 051 R 8 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

051 = Access line

Pin count

K = 32 pins

T = 36 pins

C = 48/49 pins

R = 64 pins

Flash memory size

6 = 32 Kbytes

8 = 64 Kbytes

Package

T = LQFP

H = TFBGA

U = UFQFPN

Y = Standard WLCSP pins

F = Thin WLCSP pins

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = $V_{DD}$ range: 1.8 to 3.6 V and BOR enabled

D = $V_{DD}$ range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 9 Revision history

Table 86. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 13-Feb-2014 | 1 | Initial release. |
| 29-Apr-2014 | 2 | Added WLCSP36 package. Updated *Table 2: Ultra-low-power STM32L051x6/x8 device features and peripheral counts*<br>Updated *Table 5: Functionalities depending on the working mode (from Run/active down to standby)*. Added *Section 3.2: Interconnect matrix*.<br>Updated *Figure 4: STM32L051x6/8 TFBGA64 ballout - 5x 5 mm*<br>Replaced TTa I/O structure by TC, updated PA0/4/5, PC5/14, BOOT0 and NRST I/O structure in *Table 15: STM32L051x6/8 pin definitions*.<br>Updated *Table 23: General operating conditions*, *Table 20: Voltage characteristics* and *Table 21: Current characteristics*.<br>Modified conditions in *Table 26: Embedded internal reference voltage*.<br>Updated *Table 27: Current consumption in Run mode, code with data processing running from Flash*, *Table 29: Current consumption in Run mode, code with data processing running from RAM*, *Table 31: Current consumption in Sleep mode*, *Table 32: Current consumption in Low-power run mode*, *Table 33: Current consumption in Low-power sleep mode*, *Table 34: Typical and maximum current consumptions in Stop mode* and *Table 35: Typical and maximum current consumptions in Standby mode*. Added *Figure 14: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS*, *Figure 15: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS*, *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*.<br>Updated *Table 42: HSE oscillator characteristics* and *Table 43: LSE oscillator characteristics*. Added *Figure 23: HSI16 minimum and maximum value versus temperature*.<br>Updated *Table 53: ESD absolute maximum ratings*, *Table 55: I/O current injection susceptibility* and *Table 56: I/O static characteristics*, and added *Figure 24: VIH/VIL versus VDD (CMOS I/Os)* and *Figure 25: VIH/VIL versus VDD (TTL I/Os)*. Updated *Table 57: Output voltage characteristics*, *Table 58: I/O AC characteristics* and *Figure 26: I/O AC characteristics definition*.<br>Updated *Table 60: ADC characteristics*, *Table 62: ADC accuracy*, and *Figure 29: Typical connection diagram using the ADC*. Updated *Table 64: Temperature sensor characteristics*.<br>Updated *Table 70: SPI characteristics in voltage Range 1* and *Table 73: I2S characteristics*.<br>Added *Figure 57: Thermal resistance*. |