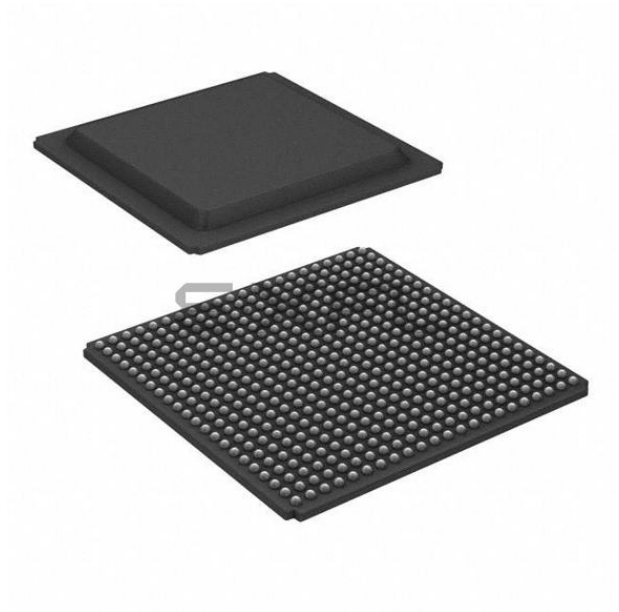
AMD Xilinx - XC7S100-1FGGA484C Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	8000
Number of Logic Elements/Cells	102400
Total RAM Bits	4423680
Number of I/O	338
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s100-1fgga484c

Table 6 shows the minimum current, in addition to I_{CCQ} maximum, that is required by Spartan-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate current drain on these supplies.

Table 6: **Power-On Current**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7S6	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S15	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S25	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S50	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S75	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S100	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S6	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S15	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S25	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S50	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S75	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S100	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}.		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}.		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}.		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}.		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$.	T_J = 125°C(1)	–	300	ms
		T_J = 100°C(1)	–	500	ms
		T_J = 85°C(1)	–	800	ms

Notes:

1. Based on 240,000 power cycles with a nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Table 15: **Networking Applications Interface Performances *(Cont'd)***

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
DDR LVDS receiver(1)	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: **Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator(1)**

Memory Standard	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
4:1 Memory Controllers				
DDR3	800(2)	667	667	Mb/s
DDR3L	800(2)	667	667	Mb/s
DDR2	800(2)	667	667	Mb/s
2:1 Memory Controllers				
DDR3	800(2)	667	667	Mb/s
DDR3L	800(2)	667	667	Mb/s
DDR2	800(2)	667	667	Mb/s
LPDDR2	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 7].
2. The maximum PHY rate is 667 Mb/s in the FTGB196 package.

IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 17: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVTTL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVTTL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns
LVTTL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVTTL_S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVTTL_S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVTTL_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVTTL_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVTTL_F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVTTL_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVTTL_F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns
LVDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MINI_LVDS_25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLVDS_25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RSDS_25 (point to point)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PPDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TMDS_33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns
PCI33_3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HSUL_12_S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HSUL_12_F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
HSTL_II_18_S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HSTL_I_F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns
HSTL_II_F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HSTL_I_18_F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns

Table 18: **IOB 3-state Output Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{IOTPHZ}	T input to pad high-impedance.	2.19	2.37	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output.	2.30	2.60	2.60	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

Table 19: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L[1]	V_H[1]	V_{MEAS}[3][5]	V_{REF}[2][4]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0[5]	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0[5]	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0[5]	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0[5]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0[5]	–
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0[5]	–
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0[5]	–
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0[5]	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0[5]	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0[5]	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0[5]	–

Table 19: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L[(1)]	V_H[(1)]	V_{MEAS}[(3)(5)]	V_{REF}[(2)(4)]
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0[(5)]	–

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
5. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

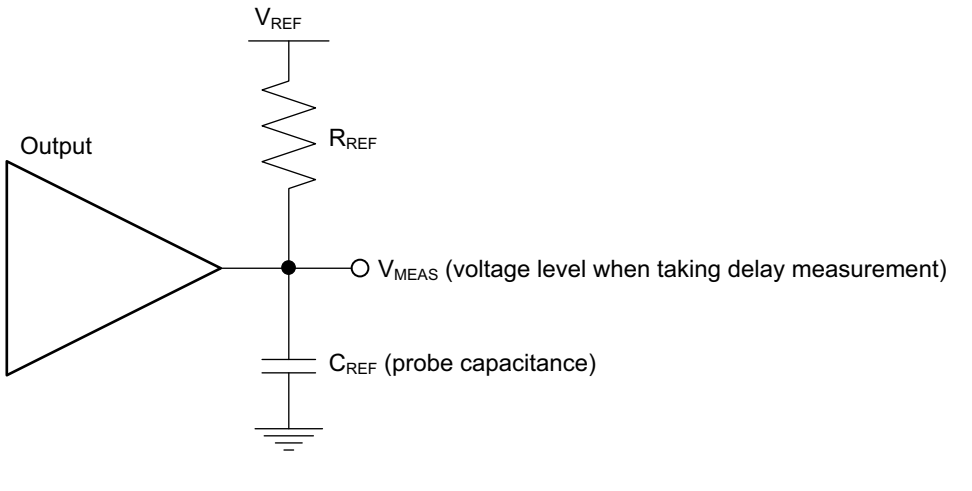

Figure 1: **Single-ended Test Setup**

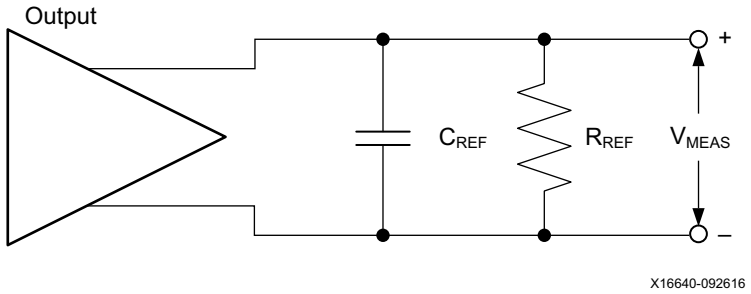

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 20.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 20: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input Serializer/Deserializer Switching Characteristics

Table 23: **ISERDES Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T_{ISCCK_CE}/ T_{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/–0.01	0.72/–0.01	0.72/–0.01	ns
T_{ISCCK_CE2}/ T_{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	–0.10/0.36	–0.10/0.40	–0.10/0.40	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/ T_{ISCKD_D}	D pin setup/hold with respect to CLK.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
T_{ISDCK_DDLY}/ T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY).(1)	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY).(1)	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

1. Recorded at 0 tap value.

Input/Output Delay Switching Characteristics

Table 25: **Input/Output Delay Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00.(1)	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00.(1)	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00.(1)	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution.	1/(32 x 2 x F_{REF})			µs
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 28: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{SHCKO}	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T_{MPW_LRAM}	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T_{MCP}	Minimum clock period.	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: **CLB Shift Register Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{REG}	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/ T_{WH\_SHFREG}$	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
$T_{CECK\_SHFREG}/ T_{CKCE\_SHFREG}$	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
$T_{DS\_SHFREG}/ T_{DH\_SHFREG}$	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width.	0.86	0.98	0.98	ns, Min

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode.(8)	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode.	0.64/0.37	0.74/0.40	0.74/0.40	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM enable (EN) input.	0.39/0.21	0.45/0.23	0.45/0.23	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register.	0.29/0.15	0.36/0.16	0.36/0.16	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input.	0.32/0.07	0.35/0.07	0.35/0.07	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input.	0.34/0.43	0.36/0.46	0.36/0.46	ns, Min
T_{RCCK_WEA}/T_{RCKC_WEA}	Write enable (WE) input (block RAM only).	0.48/0.19	0.54/0.20	0.54/0.20	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs.	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs.	0.43/0.35	0.43/0.43	0.43/0.43	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers.(9)	0.98	1.10	1.10	ns, Max
T_{RREC_RST}/T_{RREM_RST}	FIFO reset recovery and removal timing.(10)	2.07/–0.81	2.37/–0.81	2.37/–0.81	ns, Max
Maximum Frequency					
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses.	404.53	339.67	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode.	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled.	418.59	345.78	345.78	MHz

Table 37: **MMCM Specification *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S15	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S25	2.67/–0.37	3.12/–0.37	3.12/–0.37	ns
		XC7S50	2.66/–0.28	3.11/–0.28	3.11/–0.28	ns
		XC7S75	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XC7S100	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XA7S6	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S15	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S25	2.67/–0.37	3.12/–0.37	N/A	ns
		XA7S50	2.66/–0.28	3.11/–0.28	N/A	ns
		XA7S75	2.91/–0.33	3.36/–0.33	N/A	ns
		XA7S100	2.91/–0.33	3.36/–0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 45: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(3) with MMCM.	XC7S6	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S15	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S25	2.69/–0.61	3.21/–0.61	3.21/–0.61	ns
		XC7S50	2.81/–0.62	3.35/–0.62	3.35/–0.62	ns
		XC7S75	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XC7S100	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XA7S6	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S15	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S25	2.69/–0.61	3.21/–0.61	N/A	ns
		XA7S50	2.81/–0.62	3.35/–0.62	N/A	ns
		XA7S75	2.81/–0.62	3.36/–0.62	N/A	ns
		XA7S100	2.81/–0.62	3.36/–0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 46: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL.	XC7S6	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S15	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S25	3.04/–0.19	3.64/–0.19	3.64/–0.19	ns
		XC7S50	3.15/–0.19	3.77/–0.19	3.77/–0.19	ns
		XC7S75	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XC7S100	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XA7S6	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S15	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S25	3.04/–0.19	3.64/–0.19	N/A	ns
		XA7S50	3.15/–0.19	3.77/–0.19	N/A	ns
		XA7S75	3.15/–0.19	3.78/–0.19	N/A	ns
		XA7S100	3.15/–0.19	3.78/–0.19	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 47: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock.	–0.38/1.46	–0.38/1.73	–0.38/1.76	ns

Table 48: **Sample Window**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{SAMP}	Sampling error at receiver pins.(1)	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO.(2)	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C. Typical values at T_j = +40°C.						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	±1	LSBs
Offset error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain error			–	–	±0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio(2)	SNR	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion(2)	THD	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	70	–	–	dB
Analog Inputs(3)						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
On-chip Sensors						
Temperature sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)