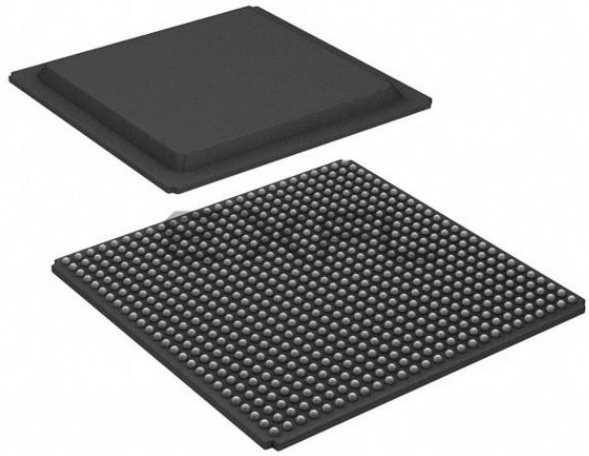

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 8000 |
| Number of Logic Elements/Cells | 102400 |
| Total RAM Bits | 4423680 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7s100-1fgga676c |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$(2)(3)(4) | I/O input voltage. | –0.4 | $V_{CCO}$ + 0.55 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33.(5) | –0.4 | 2.625 | V |
| $V_{CCBATT}$ | Key memory battery backup supply. | –0.5 | 2.0 | V |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC. | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC. | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient). | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies.(6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies.(6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature.(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

*Table 12:* **Speed Specification Version By Device**

| 2018.2.1 | Device |
|---|---|
| 1.23 | XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100 |
| 1.16 | XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100 |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CCINT}$ Operating Voltage and Speed Grade | | | | | | | | | |
| | 1.0V | | 0.95V | 1.0V | | 0.95V | 1.0V | | 0.95V | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVCMOS15_F8 | 0.86 | 0.93 | 0.93 | 1.72 | 1.98 | 1.98 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS15_F12 | 0.86 | 0.93 | 0.93 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| LVCMOS15_F16 | 0.86 | 0.93 | 0.93 | 1.46 | 1.71 | 1.71 | 1.49 | 1.73 | 1.73 | ns |
| LVCMOS12_S4 | 0.95 | 1.02 | 1.02 | 2.69 | 2.95 | 2.95 | 2.72 | 2.96 | 2.96 | ns |
| LVCMOS12_S8 | 0.95 | 1.02 | 1.02 | 2.21 | 2.46 | 2.46 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS12_S12 | 0.95 | 1.02 | 1.02 | 1.91 | 2.17 | 2.17 | 1.94 | 2.18 | 2.18 | ns |
| LVCMOS12_F4 | 0.95 | 1.02 | 1.02 | 2.10 | 2.35 | 2.35 | 2.13 | 2.37 | 2.37 | ns |
| LVCMOS12_F8 | 0.95 | 1.02 | 1.02 | 1.66 | 1.92 | 1.92 | 1.69 | 1.93 | 1.93 | ns |
| LVCMOS12_F12 | 0.95 | 1.02 | 1.02 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_S | 0.75 | 0.82 | 0.82 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| SSTL15_S | 0.68 | 0.75 | 0.75 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| SSTL18_I_S | 0.75 | 0.82 | 0.82 | 1.79 | 2.04 | 2.04 | 1.82 | 2.06 | 2.06 | ns |
| SSTL18_II_S | 0.75 | 0.82 | 0.82 | 1.43 | 1.68 | 1.68 | 1.46 | 1.70 | 1.70 | ns |
| DIFF_SSTL135_S | 0.76 | 0.83 | 0.83 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| DIFF_SSTL15_S | 0.76 | 0.83 | 0.83 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| DIFF_SSTL18_I_S | 0.79 | 0.86 | 0.86 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.79 | 0.86 | 0.86 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL15_F | 0.68 | 0.75 | 0.75 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| SSTL18_I_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL18_II_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL135_F | 0.76 | 0.83 | 0.83 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL15_F | 0.76 | 0.83 | 0.83 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| DIFF_SSTL18_I_F | 0.79 | 0.86 | 0.86 | 1.35 | 1.60 | 1.60 | 1.38 | 1.62 | 1.62 | ns |
| DIFF_SSTL18_II_F | 0.79 | 0.86 | 0.86 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |

Table 18 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

## *Output Delay Measurements*

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

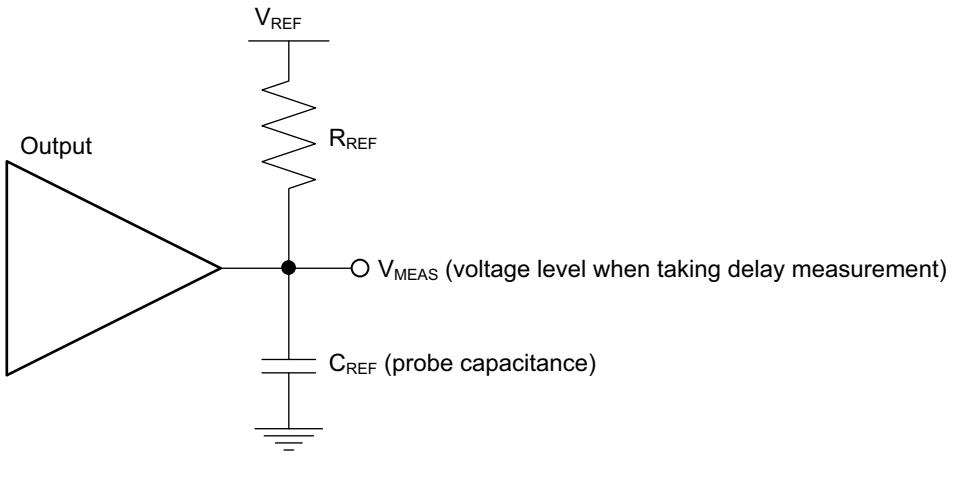


*Figure 1:* **Single-ended Test Setup**

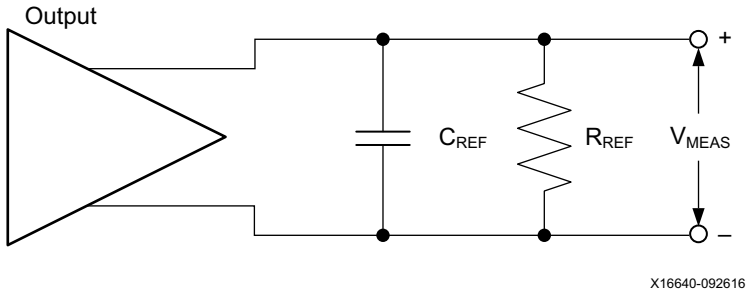


*Figure 2:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 20.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 22:* **OLOGIC Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK. | 0.71/–0.11 | 0.84/–0.11 | 0.84/–0.11 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK. | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK. | 0.44/0.21 | 0.80/0.21 | 0.80/0.21 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK. | 0.73/–0.14 | 0.89/–0.14 | 0.89/–0.14 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK. | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Combinatorial** | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out. | 0.96 | 1.16 | 1.16 | ns |
| **Sequential Delays** | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out. | 0.49 | 0.56 | 0.56 | ns |
| $T_{RQ\_OLOGIC}$ | SR pin to OQ/TQ out. | 0.80 | 0.95 | 0.95 | ns |
| $T_{GSRQ\_OLOGIC}$ | Global set/reset to Q outputs. | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | |
| $T_{RPW\_OLOGIC}$ | Minimum pulse width, SR inputs. | 0.74 | 0.74 | 0.74 | ns, Min |

# Output Serializer/Deserializer Switching Characteristics

*Table 24:* **OSERDES Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{OSDCK\_D}$/ $T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV. | 0.45/0.03 | 0.63/0.03 | 0.63/0.03 | ns |
| $T_{OSDCK\_T}$/ $T_{OSCKD\_T}$ | T input setup/hold with respect to CLK. | 0.73/–0.13 | 0.88/–0.13 | 0.88/–0.13 | ns |
| $T_{OSDCK\_T2}$/ $T_{OSCKD\_T2}$ | T input setup/hold with respect to CLKDIV. | 0.34/–0.13 | 0.39/–0.13 | 0.39/–0.13 | ns |
| $T_{OSCCK\_OCE}$/ $T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK. | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV. | 0.52 | 0.85 | 0.85 | ns |
| $T_{OSCCK\_TCE}$/ $T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK. | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Sequential Delays** | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ. | 0.42 | 0.48 | 0.48 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ. | 0.49 | 0.56 | 0.56 | ns |
| **Combinatorial** | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ out. | 0.92 | 1.11 | 1.11 | ns |

*Table 26:* **IO_FIFO Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **IO_FIFO Clock to Out Delays** | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs. | 0.60 | 0.68 | 0.68 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags. | 0.61 | 0.77 | 0.77 | ns |
| **Setup/Hold** | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK. | 0.51/0.02 | 0.58/0.02 | 0.58/0.02 | ns |
| $T_{IFFCCK\_WREN}$/ $T_{IFFCKC\_WREN}$ | WREN to WRCLK. | 0.47/–0.01 | 0.53/–0.01 | 0.53/–0.01 | ns |
| $T_{OFFCCK\_RDEN}$/ $T_{OFFCKC\_RDEN}$ | RDEN to RDCLK. | 0.58/0.02 | 0.66/0.02 | 0.66/0.02 | ns |
| **Minimum Pulse Width** | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| Maximum Frequency | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK. | 200.00 | 200.00 | 200.00 | MHz |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode.(8) | 1.15/0.59 | 1.32/0.64 | 1.32/0.64 | ns, Min |
| $T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode. | 0.64/0.37 | 0.74/0.40 | 0.74/0.40 | ns, Min |
| $T_{RCCK\_EN}$/$T_{RCKC\_EN}$ | Block RAM enable (EN) input. | 0.39/0.21 | 0.45/0.23 | 0.45/0.23 | ns, Min |
| $T_{RCCK\_REGCE}$/ $T_{RCKC\_REGCE}$ | CE input of output register. | 0.29/0.15 | 0.36/0.16 | 0.36/0.16 | ns, Min |
| $T_{RCCK\_RSTREG}$/ $T_{RCKC\_RSTREG}$ | Synchronous RSTREG input. | 0.32/0.07 | 0.35/0.07 | 0.35/0.07 | ns, Min |
| $T_{RCCK\_RSTRAM}$/ $T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input. | 0.34/0.43 | 0.36/0.46 | 0.36/0.46 | ns, Min |
| $T_{RCCK\_WEA}$/$T_{RCKC\_WEA}$ | Write enable (WE) input (block RAM only). | 0.48/0.19 | 0.54/0.20 | 0.54/0.20 | ns, Min |
| $T_{RCCK\_WREN}$/ $T_{RCKC\_WREN}$ | WREN FIFO inputs. | 0.46/0.35 | 0.47/0.43 | 0.47/0.43 | ns, Min |
| $T_{RCCK\_RDEN}$/ $T_{RCKC\_RDEN}$ | RDEN FIFO inputs. | 0.43/0.35 | 0.43/0.43 | 0.43/0.43 | ns, Min |
| **Reset Delays** | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers.(9) | 0.98 | 1.10 | 1.10 | ns, Max |
| $T_{RREC\_RST}$/$T_{RREM\_RST}$ | FIFO reset recovery and removal timing.(10) | 2.07/–0.81 | 2.37/–0.81 | 2.37/–0.81 | ns, Max |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses. | 404.53 | 339.67 | 339.67 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode. | 418.59 | 345.78 | 345.78 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled. | 418.59 | 345.78 | 345.78 | MHz |

# Clock Buffers and Networks

*Table 32:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1) | CE pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCCK\_S}/T_{BCCKC\_S}$(1) | S pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O. | 0.09 | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFG}$ | Global clock tree (BUFG). | 628.00 | 464.00 | 464.00 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 33:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O. | 1.26 | 1.54 | 1.54 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFIO}$ | I/O clock tree (BUFIO). | 680.00 | 600.00 | 600.00 | MHz |

*Table 34:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O. | 0.76 | 0.99 | 0.99 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set. | 0.39 | 0.52 | 0.52 | ns |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O. | 0.85 | 1.09 | 1.09 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFR}$(1) | Regional clock tree (BUFR). | 375.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO $F_{MAX}$ frequency.

# MMCM Switching Characteristics

*Table 37:* **MMCM Specification**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| MMCM_$F_{INMAX}$ | Maximum input clock frequency. | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{INMIN}$ | Minimum input clock frequency. | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$F_{INJITTER}$ | Maximum input clock period jitter. | < 20% of clock input period or 1 ns Max | | | |
| MMCM_$F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz. | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz. | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz. | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz. | 40 | 40 | 40 | % |
| | Allowable input duty cycle: > 500 MHz. | 45 | 45 | 45 | % |
| MMCM_$F_{MIN_PSCLK}$ | Minimum dynamic phase-shift clock frequency. | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_$F_{MAX_PSCLK}$ | Maximum dynamic phase-shift clock frequency. | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{VCOMIN}$ | Minimum MMCM VCO frequency. | 600.00 | 600.00 | 600.00 | MHz |
| MMCM_$F_{VCOMAX}$ | Maximum MMCM VCO frequency. | 1440.00 | 1200.00 | 1200.00 | MHz |
| MMCM_$F_{BANDWIDTH}$ | Low MMCM bandwidth at typical.(1) | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical.(1) | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_$T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs.(2) | 0.12 | 0.12 | 0.12 | ns |
| MMCM_$T_{OUTJITTER}$ | MMCM output jitter. | Note 3 | | | |
| MMCM_$T_{OUTDUTY}$ | MMCM output clock duty-cycle precision.(4) | 0.20 | 0.20 | 0.20 | ns |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum lock time. | 100.00 | 100.00 | 100.00 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency. | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency.(5)(6) | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation. | < 20% of clock input period or 1 ns Max | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width. | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector. | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector. | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path. | 3 ns Max or one CLKIN cycle | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable. | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |

*Table 37:* **MMCM Specification *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement. | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE. | 0.68 | 0.81 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold. | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY. | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency. | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

# PLL Switching Characteristics

*Table 38:* **PLL Specification**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| PLL_$F_{INMAX}$ | Maximum input clock frequency. | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{INMIN}$ | Minimum input clock frequency. | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$F_{INJITTER}$ | Maximum input clock period jitter. | < 20% of clock input period or 1 ns Max | | | |
| PLL_$F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz. | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz. | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz. | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz. | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz. | 45 | 45 | 45 | % |
| PLL_$F_{VCOMIN}$ | Minimum PLL VCO frequency. | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{VCOMAX}$ | Maximum PLL VCO frequency. | 1866.00 | 1600.00 | 1600.00 | MHz |

*Table 38:* **PLL Specification**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| PLL_$F_{BANDWIDTH}$ | Low PLL bandwidth at typical. | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical.(1) | 4.00 | 4.00 | 4.00 | MHz |
| PLL_$T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs.(2) | 0.12 | 0.12 | 0.12 | ns |
| PLL_$T_{OUTJITTER}$ | PLL output jitter. | Note 3 | | | |
| PLL_$T_{OUTDUTY}$ | PLL output clock duty-cycle precision.(4) | 0.20 | 0.20 | 0.20 | ns |
| PLL_$T_{LOCKMAX}$ | PLL maximum lock time. | 100.00 | 100.00 | 100.00 | µs |
| PLL_$F_{OUTMAX}$ | PLL maximum output frequency. | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{OUTMIN}$ | PLL minimum output frequency.(5) | 6.25 | 6.25 | 6.25 | MHz |
| PLL_$T_{EXTFDVAR}$ | External clock feedback variation. | < 20% of clock input period or 1 ns Max | | | |
| PLL_$RST_{MINPULSE}$ | Minimum reset pulse width. | 5.00 | 5.00 | 5.00 | ns |
| PLL_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector. | 500.00 | 450.00 | 450.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector. | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum delay in the feedback path. | 3 ns Max or one CLKIN cycle | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | |
| $T_{PLLDCK\_DADDR}$/ $T_{PLLCKD\_DADDR}$ | Setup and hold of D address. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLDCK\_DI}$/ $T_{PLLCKD\_DI}$ | Setup and hold of D input. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLDCK\_DEN}$/ $T_{PLLCKD\_DEN}$ | Setup and hold of D enable. | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{PLLDCK\_DWE}$/ $T_{PLLCKD\_DWE}$ | Setup and hold of D write enable. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY. | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency. | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

*Table 40:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)[1]**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.** | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region).[2] | XC7S6 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S15 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S25 | 5.55 | 6.44 | 6.44 | ns |
| | | XC7S50 | 5.71 | 6.62 | 6.62 | ns |
| | | XC7S75 | 6.01 | 7.02 | 7.02 | ns |
| | | XC7S100 | 6.01 | 7.02 | 7.02 | ns |
| | | XA7S6 | 5.55 | 6.50 | N/A | ns |
| | | XA7S15 | 5.55 | 6.50 | N/A | ns |
| | | XA7S25 | 5.55 | 6.44 | N/A | ns |
| | | XA7S50 | 5.71 | 6.62 | N/A | ns |
| | | XA7S75 | 6.01 | 7.02 | N/A | ns |
| | | XA7S100 | 6.01 | 7.02 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

*Table 41:* **Clock-Capable Clock Input to Output Delay With MMCM(1)**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.** | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM.(2) | XC7S6 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S15 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S25 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S50 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S75 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S100 | 1.00 | 1.00 | 1.00 | ns |
| | | XA7S6 | 1.03 | 1.03 | N/A | ns |
| | | XA7S15 | 1.03 | 1.03 | N/A | ns |
| | | XA7S25 | 1.00 | 1.00 | N/A | ns |
| | | XA7S50 | 1.00 | 1.00 | N/A | ns |
| | | XA7S75 | 1.00 | 1.00 | N/A | ns |
| | | XA7S100 | 1.00 | 1.00 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 42:* **Clock-Capable Clock Input to Output Delay With PLL(1)**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.** | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL.(2) | XC7S6 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S15 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S25 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S50 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S75 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S100 | 0.83 | 0.83 | 0.83 | ns |
| | | XA7S6 | 0.85 | 0.85 | N/A | ns |
| | | XA7S15 | 0.85 | 0.85 | N/A | ns |
| | | XA7S25 | 0.83 | 0.83 | N/A | ns |
| | | XA7S50 | 0.83 | 0.83 | N/A | ns |
| | | XA7S75 | 0.83 | 0.83 | N/A | ns |
| | | XA7S100 | 0.83 | 0.83 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 43:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.** | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock. | 5.61 | 6.64 | 6.64 | ns |

*Table 45:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)(2)** | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(3) with MMCM. | XC7S6 | 2.73/–0.59 | 3.27/–0.59 | 3.27/–0.59 | ns |
| | | XC7S15 | 2.73/–0.59 | 3.27/–0.59 | 3.27/–0.59 | ns |
| | | XC7S25 | 2.69/–0.61 | 3.21/–0.61 | 3.21/–0.61 | ns |
| | | XC7S50 | 2.81/–0.62 | 3.35/–0.62 | 3.35/–0.62 | ns |
| | | XC7S75 | 2.81/–0.62 | 3.36/–0.62 | 3.36/–0.62 | ns |
| | | XC7S100 | 2.81/–0.62 | 3.36/–0.62 | 3.36/–0.62 | ns |
| | | XA7S6 | 2.73/–0.59 | 3.27/–0.59 | N/A | ns |
| | | XA7S15 | 2.73/–0.59 | 3.27/–0.59 | N/A | ns |
| | | XA7S25 | 2.69/–0.61 | 3.21/–0.61 | N/A | ns |
| | | XA7S50 | 2.81/–0.62 | 3.35/–0.62 | N/A | ns |
| | | XA7S75 | 2.81/–0.62 | 3.36/–0.62 | N/A | ns |
| | | XA7S100 | 2.81/–0.62 | 3.36/–0.62 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

*Table 46:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)** | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(3) with PLL. | XC7S6 | 3.07/–0.17 | 3.69/–0.17 | 3.69/–0.17 | ns |
| | | XC7S15 | 3.07/–0.17 | 3.69/–0.17 | 3.69/–0.17 | ns |
| | | XC7S25 | 3.04/–0.19 | 3.64/–0.19 | 3.64/–0.19 | ns |
| | | XC7S50 | 3.15/–0.19 | 3.77/–0.19 | 3.77/–0.19 | ns |
| | | XC7S75 | 3.15/–0.19 | 3.78/–0.19 | 3.78/–0.19 | ns |
| | | XC7S100 | 3.15/–0.19 | 3.78/–0.19 | 3.78/–0.19 | ns |
| | | XA7S6 | 3.07/–0.17 | 3.69/–0.17 | N/A | ns |
| | | XA7S15 | 3.07/–0.17 | 3.69/–0.17 | N/A | ns |
| | | XA7S25 | 3.04/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XA7S50 | 3.15/–0.19 | 3.77/–0.19 | N/A | ns |
| | | XA7S75 | 3.15/–0.19 | 3.78/–0.19 | N/A | ns |
| | | XA7S100 | 3.15/–0.19 | 3.78/–0.19 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

*Table 47:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.** | | | | | |
| $T_{PSCS}$/$T_{PHCS}$ | Setup and hold of I/O clock. | –0.38/1.46 | –0.38/1.73 | –0.38/1.76 | ns |

*Table 48:* **Sample Window**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{SAMP}$ | Sampling error at receiver pins.(1) | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO.(2) | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

# XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

*Table 50:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, –55°C ≤ $T_j$ ≤ 125°C. Typical values at $T_j$ = +40°C. | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral nonlinearity(2) | INL | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±2 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±3 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic. | – | – | ±1 | LSBs |
| Offset error | Unipolar | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±8 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±12 | LSBs |
| | Bipolar | –55°C ≤ $T_j$ ≤ 125°C | – | – | ±4 | LSBs |
| Gain error | | | – | – | ±0.5 | % |
| Offset matching | | | – | – | 4 | LSBs |
| Gain matching | | | – | – | 0.3 | % |
| Sample rate | | | – | – | 1 | MS/s |
| Signal to noise ratio(2) | SNR | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 60 | – | – | dB |
| RMS code noise | | External 1.25V reference. | – | – | 2 | LSBs |
| | | On-chip reference. | – | 3 | – | LSBs |
| Total harmonic distortion(2) | THD | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 70 | – | – | dB |
| **Analog Inputs**(3) | | | | | | |
| ADC input ranges | | Unipolar operation. | 0 | – | 1 | V |
| | | Bipolar operation. | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input). | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input). | +0.5 | – | +0.6 | V |
| Maximum external channel input ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels. | –0.1 | – | $V_{CCADC}$ | V |
| Full-resolution bandwidth | FRBW | Auxiliary channel full resolution bandwidth. | 250 | – | – | kHz |
| **On-chip Sensors** | | | | | | |
| Temperature sensor error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±4 | °C |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±6 | °C |
| Supply sensor error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±1 | % |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±2 | % |

# eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

*Table 52:* **eFUSE Programming Conditions(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $T_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

# References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)