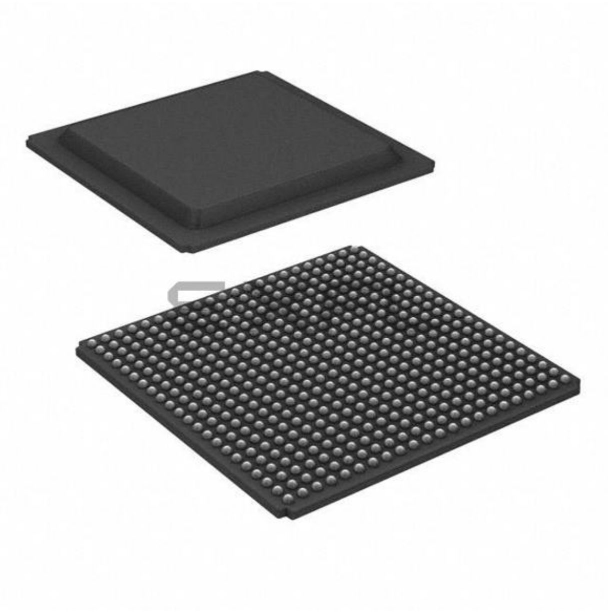
# AMD Xilinx - XC7S100-2FGGA484C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 8000 |
| Number of Logic Elements/Cells | 102400 |
| Total RAM Bits | 4423680 |
| Number of I/O | 338 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7s100-2fgga484c |

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*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | For -2 and -1 (1.0V) devices: internal supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: internal supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage. | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$(3) | For -2 and -1 (1.0V) devices: block RAM supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: block RAM supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCO}$(4)(5) | Supply voltage for HR I/O banks. | 1.14 | – | 3.465 | V |
| $V_{IN}$(6) | I/O input voltage. | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33.(7) | –0.20 | – | 2.625 | V |
| $I_{IN}$(8) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(9) | Battery voltage. | 1.0 | – | 1.89 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC. | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage. | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices. | 0 | – | 85 | °C |
| | Junction temperature operating range for industrial (I) temperature devices. | –40 | – | 100 | °C |
| | Junction temperature operating range for expanded (Q) temperature devices. | –40 | – | 125 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
3. If $V_{CCINT}$ and $V_{CCBRAM}$ are operating at the same voltage, $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
4. Configuration data is retained even if $V_{CCO}$ drops to 0V.
5. Includes $V_{CCO}$ of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.

*Table 5:* **Typical Quiescent Supply Current(1)(2)(3)** ***(Cont'd)***

| **Symbol** | **Description** | **Device** | **Speed Grade** | | | | | | **Units** |
|---|---|---|---|---|---|---|---|---|---|
| | | | **1.0V** | | | | | **0.95V** | |
| | | | **-2C** | **-2I** | **-1C** | **-1I** | **-1Q** | **-1LI** | |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current. | XC7S6 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S15 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S25 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S50 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S75 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XC7S100 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XA7S6 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S15 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S25 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S50 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S75 | N/A | 4 | N/A | 4 | 4 | N/A | mA |
| | | XA7S100 | N/A | 4 | N/A | 4 | 4 | N/A | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current. | XC7S6 | 10 | 10 | 10 | 10 | 10 | 10 | mA |
| | | XC7S15 | 10 | 10 | 10 | 10 | 10 | 10 | mA |
| | | XC7S25 | 13 | 13 | 13 | 13 | 13 | 13 | mA |
| | | XC7S50 | 22 | 22 | 22 | 22 | 22 | 20 | mA |
| | | XC7S75 | 43 | 43 | 43 | 43 | 43 | 43 | mA |
| | | XC7S100 | 43 | 43 | 43 | 43 | 43 | 43 | mA |
| | | XA7S6 | N/A | 10 | N/A | 10 | 10 | N/A | mA |
| | | XA7S15 | N/A | 10 | N/A | 10 | 10 | N/A | mA |
| | | XA7S25 | N/A | 13 | N/A | 13 | 13 | N/A | mA |
| | | XA7S50 | N/A | 22 | N/A | 22 | 22 | N/A | mA |
| | | XA7S75 | N/A | 43 | N/A | 43 | 43 | N/A | mA |
| | | XA7S100 | N/A | 43 | N/A | 43 | 43 | N/A | mA |

## LVDS DC Specifications (LVDS_25)

*Table 11:* **LVDS_25 DC Specifications**(1)

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage. | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage:<br>$(Q - \overline{Q})$, Q = High<br>$(\overline{Q} - Q)$, $\overline{Q}$ = High | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage:<br>$(Q - \overline{Q})$, Q = High<br>$(\overline{Q} - Q)$, $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage. | | 0.300 | 1.200 | 1.500 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

*Table 12:* **Speed Specification Version By Device**

| 2018.2.1 | Device |
|---|---|
| 1.23 | XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100 |
| 1.16 | XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100 |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

# Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Spartan-7 device on a per speed grade basis.

*Table 13:* **Spartan-7 Device Speed Grade Designations**

| Device | Speed Grade, Temperature Range, and $V_{CCINT}$ Operating Voltage | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7S6 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XC7S15 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XC7S25 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XC7S50 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XC7S75 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XC7S100 | | | -2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1) |
| XA7S6 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |
| XA7S15 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |
| XA7S25 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |
| XA7S50 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |
| XA7S75 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |
| XA7S100 | | | -2I (1.0V), -1I (1.0V), -1Q (1.0V) |

**Notes:**

1. The lowest power -1LI devices, where $V_{CCINT}$ = 0.95V, are listed in the Vivado Design Suite as -1IL.

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 14 lists the production released Spartan-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 17:* **IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CCINT}$ Operating Voltage and Speed Grade | | | | | | | | | |
| | 1.0V | | 0.95V | 1.0V | | 0.95V | 1.0V | | 0.95V | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVTTL_S4 | 1.34 | 1.41 | 1.41 | 3.93 | 4.18 | 4.18 | 3.96 | 4.20 | 4.20 | ns |
| LVTTL_S8 | 1.34 | 1.41 | 1.41 | 3.66 | 3.92 | 3.92 | 3.69 | 3.93 | 3.93 | ns |
| LVTTL_S12 | 1.34 | 1.41 | 1.41 | 3.65 | 3.90 | 3.90 | 3.68 | 3.91 | 3.91 | ns |
| LVTTL_S16 | 1.34 | 1.41 | 1.41 | 3.19 | 3.45 | 3.45 | 3.22 | 3.46 | 3.46 | ns |
| LVTTL_S24 | 1.34 | 1.41 | 1.41 | 3.41 | 3.67 | 3.67 | 3.44 | 3.68 | 3.68 | ns |
| LVTTL_F4 | 1.34 | 1.41 | 1.41 | 3.38 | 3.64 | 3.64 | 3.41 | 3.65 | 3.65 | ns |
| LVTTL_F8 | 1.34 | 1.41 | 1.41 | 2.87 | 3.12 | 3.12 | 2.90 | 3.13 | 3.13 | ns |
| LVTTL_F12 | 1.34 | 1.41 | 1.41 | 2.85 | 3.10 | 3.10 | 2.88 | 3.12 | 3.12 | ns |
| LVTTL_F16 | 1.34 | 1.41 | 1.41 | 2.68 | 2.93 | 2.93 | 2.71 | 2.95 | 2.95 | ns |
| LVTTL_F24 | 1.34 | 1.41 | 1.41 | 2.65 | 2.90 | 2.90 | 2.68 | 2.91 | 2.91 | ns |
| LVDS_25 | 0.81 | 0.88 | 0.88 | 1.41 | 1.67 | 1.67 | 1.44 | 1.68 | 1.68 | ns |
| MINI_LVDS_25 | 0.81 | 0.88 | 0.88 | 1.40 | 1.65 | 1.65 | 1.43 | 1.66 | 1.66 | ns |
| BLVDS_25 | 0.81 | 0.88 | 0.88 | 1.96 | 2.21 | 2.21 | 1.99 | 2.23 | 2.23 | ns |
| RSDS_25 (point to point) | 0.81 | 0.88 | 0.88 | 1.40 | 1.65 | 1.65 | 1.43 | 1.66 | 1.66 | ns |
| PPDS_25 | 0.81 | 0.88 | 0.88 | 1.41 | 1.67 | 1.67 | 1.44 | 1.68 | 1.68 | ns |
| TMDS_33 | 0.81 | 0.88 | 0.88 | 1.54 | 1.79 | 1.79 | 1.57 | 1.80 | 1.80 | ns |
| PCI33_3 | 1.32 | 1.39 | 1.39 | 3.22 | 3.48 | 3.48 | 3.25 | 3.49 | 3.49 | ns |
| HSUL_12_S | 0.75 | 0.82 | 0.82 | 1.93 | 2.18 | 2.18 | 1.96 | 2.20 | 2.20 | ns |
| HSUL_12_F | 0.75 | 0.82 | 0.82 | 1.41 | 1.67 | 1.67 | 1.44 | 1.68 | 1.68 | ns |
| DIFF_HSUL_12_S | 0.76 | 0.83 | 0.83 | 1.93 | 2.18 | 2.18 | 1.96 | 2.20 | 2.20 | ns |
| DIFF_HSUL_12_F | 0.76 | 0.83 | 0.83 | 1.41 | 1.67 | 1.67 | 1.44 | 1.68 | 1.68 | ns |
| MOBILE_DDR_S | 0.84 | 0.91 | 0.91 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| MOBILE_DDR_F | 0.84 | 0.91 | 0.91 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| DIFF_MOBILE_DDR_S | 0.78 | 0.85 | 0.85 | 1.82 | 2.07 | 2.07 | 1.85 | 2.09 | 2.09 | ns |
| DIFF_MOBILE_DDR_F | 0.78 | 0.85 | 0.85 | 1.57 | 1.82 | 1.82 | 1.60 | 1.84 | 1.84 | ns |
| HSTL_I_S | 0.75 | 0.82 | 0.82 | 1.74 | 1.99 | 1.99 | 1.77 | 2.01 | 2.01 | ns |
| HSTL_II_S | 0.73 | 0.80 | 0.80 | 1.54 | 1.79 | 1.79 | 1.57 | 1.80 | 1.80 | ns |
| HSTL_I_18_S | 0.75 | 0.82 | 0.82 | 1.41 | 1.67 | 1.67 | 1.44 | 1.68 | 1.68 | ns |
| HSTL_II_18_S | 0.75 | 0.81 | 0.81 | 1.54 | 1.79 | 1.79 | 1.57 | 1.80 | 1.80 | ns |
| DIFF_HSTL_I_S | 0.76 | 0.83 | 0.83 | 1.71 | 1.96 | 1.96 | 1.74 | 1.98 | 1.98 | ns |
| DIFF_HSTL_II_S | 0.76 | 0.83 | 0.83 | 1.63 | 1.88 | 1.88 | 1.66 | 1.90 | 1.90 | ns |
| DIFF_HSTL_I_18_S | 0.79 | 0.86 | 0.86 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| DIFF_HSTL_II_18_S | 0.78 | 0.85 | 0.85 | 1.58 | 1.84 | 1.84 | 1.61 | 1.85 | 1.85 | ns |
| HSTL_I_F | 0.75 | 0.82 | 0.82 | 1.22 | 1.48 | 1.48 | 1.25 | 1.49 | 1.49 | ns |
| HSTL_II_F | 0.73 | 0.80 | 0.80 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| HSTL_I_18_F | 0.75 | 0.82 | 0.82 | 1.26 | 1.51 | 1.51 | 1.29 | 1.52 | 1.52 | ns |

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CCINT}$ Operating Voltage and Speed Grade | | | | | | | | | |
| | 1.0V | | 0.95V | 1.0V | | 0.95V | 1.0V | | 0.95V | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| HSTL_II_18_F | 0.75 | 0.81 | 0.81 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_HSTL_I_F | 0.76 | 0.83 | 0.83 | 1.30 | 1.56 | 1.56 | 1.33 | 1.57 | 1.57 | ns |
| DIFF_HSTL_II_F | 0.76 | 0.83 | 0.83 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |
| DIFF_HSTL_I_18_F | 0.79 | 0.86 | 0.86 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |
| DIFF_HSTL_II_18_F | 0.78 | 0.85 | 0.85 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |
| LVCMOS33_S4 | 1.34 | 1.41 | 1.41 | 3.93 | 4.18 | 4.18 | 3.96 | 4.20 | 4.20 | ns |
| LVCMOS33_S8 | 1.34 | 1.41 | 1.41 | 3.65 | 3.90 | 3.90 | 3.68 | 3.91 | 3.91 | ns |
| LVCMOS33_S12 | 1.34 | 1.41 | 1.41 | 3.21 | 3.46 | 3.46 | 3.24 | 3.48 | 3.48 | ns |
| LVCMOS33_S16 | 1.34 | 1.41 | 1.41 | 3.52 | 3.77 | 3.77 | 3.55 | 3.79 | 3.79 | ns |
| LVCMOS33_F4 | 1.34 | 1.41 | 1.41 | 3.38 | 3.64 | 3.64 | 3.41 | 3.65 | 3.65 | ns |
| LVCMOS33_F8 | 1.34 | 1.41 | 1.41 | 2.87 | 3.12 | 3.12 | 2.90 | 3.13 | 3.13 | ns |
| LVCMOS33_F12 | 1.34 | 1.41 | 1.41 | 2.68 | 2.93 | 2.93 | 2.71 | 2.95 | 2.95 | ns |
| LVCMOS33_F16 | 1.34 | 1.41 | 1.41 | 2.68 | 2.93 | 2.93 | 2.71 | 2.95 | 2.95 | ns |
| LVCMOS25_S4 | 1.20 | 1.27 | 1.27 | 3.26 | 3.51 | 3.51 | 3.29 | 3.52 | 3.52 | ns |
| LVCMOS25_S8 | 1.20 | 1.27 | 1.27 | 3.01 | 3.26 | 3.26 | 3.04 | 3.27 | 3.27 | ns |
| LVCMOS25_S12 | 1.20 | 1.27 | 1.27 | 2.60 | 2.85 | 2.85 | 2.63 | 2.87 | 2.87 | ns |
| LVCMOS25_S16 | 1.20 | 1.27 | 1.27 | 2.94 | 3.20 | 3.20 | 2.97 | 3.21 | 3.21 | ns |
| LVCMOS25_F4 | 1.20 | 1.27 | 1.27 | 2.87 | 3.12 | 3.12 | 2.90 | 3.13 | 3.13 | ns |
| LVCMOS25_F8 | 1.20 | 1.27 | 1.27 | 2.30 | 2.56 | 2.56 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS25_F12 | 1.20 | 1.27 | 1.27 | 2.29 | 2.54 | 2.54 | 2.32 | 2.55 | 2.55 | ns |
| LVCMOS25_F16 | 1.20 | 1.27 | 1.27 | 2.13 | 2.39 | 2.39 | 2.16 | 2.40 | 2.40 | ns |
| LVCMOS18_S4 | 0.83 | 0.89 | 0.89 | 1.74 | 1.99 | 1.99 | 1.77 | 2.01 | 2.01 | ns |
| LVCMOS18_S8 | 0.83 | 0.89 | 0.89 | 2.30 | 2.56 | 2.56 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS18_S12 | 0.83 | 0.89 | 0.89 | 2.30 | 2.56 | 2.56 | 2.33 | 2.57 | 2.57 | ns |
| LVCMOS18_S16 | 0.83 | 0.89 | 0.89 | 1.65 | 1.90 | 1.90 | 1.68 | 1.91 | 1.91 | ns |
| LVCMOS18_S24 | 0.83 | 0.89 | 0.89 | 1.72 | 1.98 | 1.98 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS18_F4 | 0.83 | 0.89 | 0.89 | 1.57 | 1.82 | 1.82 | 1.60 | 1.84 | 1.84 | ns |
| LVCMOS18_F8 | 0.83 | 0.89 | 0.89 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| LVCMOS18_F12 | 0.83 | 0.89 | 0.89 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| LVCMOS18_F16 | 0.83 | 0.89 | 0.89 | 1.52 | 1.77 | 1.77 | 1.55 | 1.79 | 1.79 | ns |
| LVCMOS18_F24 | 0.83 | 0.89 | 0.89 | 1.46 | 1.71 | 1.71 | 1.49 | 1.73 | 1.73 | ns |
| LVCMOS15_S4 | 0.86 | 0.93 | 0.93 | 2.18 | 2.43 | 2.43 | 2.21 | 2.45 | 2.45 | ns |
| LVCMOS15_S8 | 0.86 | 0.93 | 0.93 | 2.21 | 2.46 | 2.46 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS15_S12 | 0.86 | 0.93 | 0.93 | 1.71 | 1.96 | 1.96 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_S16 | 0.86 | 0.93 | 0.93 | 1.71 | 1.96 | 1.96 | 1.74 | 1.98 | 1.98 | ns |
| LVCMOS15_F4 | 0.86 | 0.93 | 0.93 | 1.97 | 2.23 | 2.23 | 2.00 | 2.24 | 2.24 | ns |

*Table 19:* **Input Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $V_L$[1] | $V_H$[1] | $V_{MEAS}$[3][5] | $V_{REF}$[2][4] |
|---|---|---|---|---|---|
| PPDS_25 | PPDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0[5] | – |
| RSDS_25 | RSDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0[5] | – |
| TMDS_33 | TMDS_33 | 3 – 0.125 | 3 + 0.125 | 0[5] | – |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 1.
5. The value given is the differential input voltage.

## Input/Output Logic Switching Characteristics

*Table 21:* **ILOGIC Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK. | 0.54/0.02 | 0.76/0.02 | 0.76/0.02 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin setup/hold with respect to CLK. | 0.70/0.01 | 1.13/0.01 | 1.13/0.01 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin setup/hold with respect to CLK without delay. | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY). | 0.02/0.29 | 0.02/0.33 | 0.02/0.33 | ns |
| **Combinatorial** | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no delay. | 0.11 | 0.13 | 0.13 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY). | 0.12 | 0.14 | 0.14 | ns |
| **Sequential Delays** | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without delay. | 0.44 | 0.51 | 0.51 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY). | 0.44 | 0.51 | 0.51 | ns |
| $T_{ICKQ}$ | CLK to Q outputs. | 0.57 | 0.66 | 0.66 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out. | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global set/reset to Q outputs. | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum pulse width, SR inputs. | 0.72 | 0.72 | 0.72 | ns, Min |

# Input/Output Delay Switching Characteristics

*Table 25:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **IDELAYCTRL** | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to ready for IDELAYCTRL. | 3.67 | 3.67 | 3.67 | µs |
| $F_{IDELAYCTRL\_REF}$ | Attribute REFCLK frequency = 200.00.(1) | 200.00 | 200.00 | 200.00 | MHz |
| | Attribute REFCLK frequency = 300.00.(1) | 300.00 | 300.00 | 300.00 | MHz |
| | Attribute REFCLK frequency = 400.00.(1) | 400.00 | N/A | N/A | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum reset pulse width. | 59.28 | 59.28 | 59.28 | ns |
| **IDELAY** | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY chain delay resolution. | 1/(32 x 2 x $F_{REF}$) | | | µs |
| $T_{IDELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3) | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4) | ±9 | ±9 | ±9 | ps per tap |
| $T_{IDELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IDELAY. | 680.00 | 600.00 | 600.00 | MHz |
| $T_{IDCCK\_CE}$ / $T_{IDCKC\_CE}$ | CE pin setup/hold with respect to C for IDELAY. | 0.16/0.13 | 0.21/0.16 | 0.21/0.16 | ns |
| $T_{IDCCK\_INC}$/ $T_{IDCKC\_INC}$ | INC pin setup/hold with respect to C for IDELAY. | 0.14/0.18 | 0.16/0.22 | 0.16/0.22 | ns |
| $T_{IDCCK\_RST}$/ $T_{IDCKC\_RST}$ | RST pin setup/hold with respect to C for IDELAY. | 0.16/0.11 | 0.18/0.14 | 0.18/0.14 | ns |
| $T_{IDDO\_IDATAIN}$ | Propagation delay through IDELAY. | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

## CLB Switching Characteristics

*Table 27:* **CLB Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Combinatorial Delays** | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A. | 0.11 | 0.13 | 0.13 | ns, Max |
| $T_{ILO\_2}$ | An – Dn LUT address to AMUX/CMUX. | 0.30 | 0.36 | 0.36 | ns, Max |
| $T_{ILO\_3}$ | An – Dn LUT address to BMUX_A. | 0.46 | 0.55 | 0.55 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs. | 1.05 | 1.27 | 1.27 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output. | 0.69 | 0.84 | 0.84 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output. | 0.66 | 0.83 | 0.83 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output. | 0.68 | 0.82 | 0.82 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output. | 0.75 | 0.90 | 0.90 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output. | 0.57 | 0.69 | 0.69 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output. | 0.69 | 0.82 | 0.82 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output. | 0.48 | 0.58 | 0.58 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output. | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output. | 0.58 | 0.70 | 0.70 | ns, Max |
| **Sequential Delays** | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs. | 0.44 | 0.53 | 0.53 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs. | 0.53 | 0.66 | 0.66 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | |
| $T_{AS}/T_{AH}$ | AN – DN input to CLK on A – D flip-flops. | 0.09/0.14 | 0.11/0.18 | 0.11/0.18 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | AX – DX input to CLK on A – D flip-flops. | 0.07/0.21 | 0.09/0.26 | 0.09/0.26 | ns, Min |
| | AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops. | 0.66/0.09 | 0.81/0.11 | 0.81/0.11 | ns, Min |
| $T_{CECK\_CLB}/T_{CKCE\_CLB}$ | CE input to CLK on A – D flip-flops. | 0.17/0.00 | 0.21/0.01 | 0.21/0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops. | 0.43/0.04 | 0.53/0.05 | 0.53/0.05 | ns, Min |
| **Set/Reset** | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width. | 0.78 | 1.04 | 1.04 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops. | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops. | 0.58 | 0.70 | 0.70 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control). | 1286 | 1098 | 1098 | MHz |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B. | 362.19 | 297.35 | 297.35 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration. | 365.10 | 297.53 | 297.53 | MHz |

**Notes:**

1. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
6. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{DSPDCK\_CEM\_MREG}$/<br>$T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK. | 0.21/<br>0.20 | 0.27/<br>0.23 | 0.27/<br>0.23 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/<br>$T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK. | 0.43/<br>0.01 | 0.53/<br>0.01 | 0.53/<br>0.01 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/<br>$T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK. | 0.46/<br>0.13 | 0.55/<br>0.15 | 0.55/<br>0.15 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/<br>$T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK. | 0.08/<br>0.11 | 0.09/<br>0.12 | 0.09/<br>0.12 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/<br>$T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.50/<br>0.08 | 0.59/<br>0.09 | 0.59/<br>0.09 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/<br>$T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.23/<br>0.24 | 0.27/<br>0.28 | 0.27/<br>0.28 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/<br>$T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.30/<br>0.01 | 0.35/<br>0.01 | 0.35/<br>0.01 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier. | 4.35 | 5.18 | 5.18 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier. | 4.26 | 5.07 | 5.07 | ns |
| $T_{DSPDO\_B\_P}$ | B input to P output not using multiplier. | 1.75 | 2.08 | 2.08 | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output. | 1.53 | 1.82 | 1.82 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output. | 0.63 | 0.74 | 0.74 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier. | 4.65 | 5.54 | 5.54 | ns |
| $T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$ | D input to CARRYCASCOUT output using multiplier. | 4.54 | 5.40 | 5.40 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier. | 2.03 | 2.41 | 2.41 | ns |
| $T_{DSPDO\_C\_CARRYCASCOUT}$ | C input to CARRYCASCOUT output. | 1.81 | 2.15 | 2.15 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | |
| $T_{DSPDO\_ACIN\_P\_MULT}$ | ACIN input to P output using multiplier. | 4.19 | 5.00 | 5.00 | ns |
| $T_{DSPDO\_ACIN\_P}$ | ACIN input to P output not using multiplier. | 1.57 | 1.88 | 1.88 | ns |
| $T_{DSPDO\_ACIN\_ACOUT}$ | ACIN input to ACOUT output. | 0.44 | 0.53 | 0.53 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier. | 4.47 | 5.33 | 5.33 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier. | 1.85 | 2.21 | 2.21 | ns |
| $T_{DSPDO\_PCIN\_P}$ | PCIN input to P output. | 1.28 | 1.52 | 1.52 | ns |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{DSPDO\_PCIN\_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output. | 1.56 | 1.85 | 1.85 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK PREG to P output. | 0.37 | 0.44 | 0.44 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_PREG}$ | CLK PREG to CARRYCASCOUT output. | 0.59 | 0.69 | 0.69 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output. | 1.93 | 2.31 | 2.31 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output. | 2.21 | 2.64 | 2.64 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier. | 3.10 | 3.69 | 3.69 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier. | 3.38 | 4.02 | 4.02 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier. | 4.51 | 5.37 | 5.37 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier. | 1.87 | 2.22 | 2.22 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier. | 1.93 | 2.30 | 2.30 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier. | 4.48 | 5.32 | 5.32 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output. | 0.73 | 0.87 | 0.87 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier. | 4.79 | 5.70 | 5.70 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier. | 2.15 | 2.55 | 2.55 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier. | 4.76 | 5.65 | 5.65 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output. | 2.21 | 2.63 | 2.63 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | With all registers used. | 550.66 | 464.25 | 464.25 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 465.77 | 392.93 | 392.93 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 305.62 | 257.47 | 257.47 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 277.62 | 233.92 | 233.92 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 227.01 | 190.69 | 190.69 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 211.15 | 177.43 | 177.43 | MHz |

# Clock Buffers and Networks

*Table 32:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BCCCK\_CE}$/$T_{BCCKC\_CE}$(1) | CE pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCCK\_S}$/ $T_{BCCKC\_S}$(1) | S pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O. | 0.09 | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFG}$ | Global clock tree (BUFG). | 628.00 | 464.00 | 464.00 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 33:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O. | 1.26 | 1.54 | 1.54 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFIO}$ | I/O clock tree (BUFIO). | 680.00 | 600.00 | 600.00 | MHz |

*Table 34:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O. | 0.76 | 0.99 | 0.99 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set. | 0.39 | 0.52 | 0.52 | ns |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O. | 0.85 | 1.09 | 1.09 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFR}$(1) | Regional clock tree (BUFR). | 375.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO $F_{MAX}$ frequency.

## Device Pin-to-Pin Output Parameter Guidelines

*Table 39:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[(1)]**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.** | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[(2)] | XC7S6 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S15 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S25 | 5.55 | 6.44 | 6.44 | ns |
| | | XC7S50 | 5.71 | 6.62 | 6.62 | ns |
| | | XC7S75 | 5.73 | 6.71 | 6.71 | ns |
| | | XC7S100 | 5.73 | 6.71 | 6.71 | ns |
| | | XA7S6 | 5.55 | 6.50 | N/A | ns |
| | | XA7S15 | 5.55 | 6.50 | N/A | ns |
| | | XA7S25 | 5.55 | 6.44 | N/A | ns |
| | | XA7S50 | 5.71 | 6.62 | N/A | ns |
| | | XA7S75 | 5.73 | 6.71 | N/A | ns |
| | | XA7S100 | 5.73 | 6.71 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

# XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

*Table 50:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $-55°C \le T_j \le 125°C$. Typical values at $T_j$ = +40°C. | | | | | | |
| **ADC Accuracy**[1] | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral nonlinearity[2] | INL | $-40°C \le T_j \le 100°C$ | – | – | ±2 | LSBs |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±3 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic. | – | – | ±1 | LSBs |
| Offset error | Unipolar | $-40°C \le T_j \le 100°C$ | – | – | ±8 | LSBs |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±12 | LSBs |
| | Bipolar | $-55°C \le T_j \le 125°C$ | – | – | ±4 | LSBs |
| Gain error | | | – | – | ±0.5 | % |
| Offset matching | | | – | – | 4 | LSBs |
| Gain matching | | | – | – | 0.3 | % |
| Sample rate | | | – | – | 1 | MS/s |
| Signal to noise ratio[2] | SNR | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 60 | – | – | dB |
| RMS code noise | | External 1.25V reference. | – | – | 2 | LSBs |
| | | On-chip reference. | – | 3 | – | LSBs |
| Total harmonic distortion[2] | THD | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 70 | – | – | dB |
| **Analog Inputs**[3] | | | | | | |
| ADC input ranges | | Unipolar operation. | 0 | – | 1 | V |
| | | Bipolar operation. | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input). | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input). | +0.5 | – | +0.6 | V |
| Maximum external channel input ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels. | –0.1 | – | $V_{CCADC}$ | V |
| Full-resolution bandwidth | FRBW | Auxiliary channel full resolution bandwidth. | 250 | – | – | kHz |
| **On-chip Sensors** | | | | | | |
| Temperature sensor error | | $-40°C \le T_j \le 100°C$ | – | – | ±4 | °C |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±6 | °C |
| Supply sensor error | | $-40°C \le T_j \le 100°C$ | – | – | ±1 | % |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±2 | % |

# Configuration Switching Characteristics

*Table 51:* **Configuration Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Power-up Timing Characteristics** | | | | | |
| $T_{PL}$(1) | Program latency. | 5.00 | 5.00 | 5.00 | ms, Max |
| $T_{POR}$(2) | Power-on reset (50 ms ramp rate time). | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time). | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| $T_{PROGRAM}$ | Program pulse width. | 250.00 | 250.00 | 250.00 | ns, Min |
| **CCLK Output (Master Mode)** | | | | | |
| $T_{ICCK}$ | Master CCLK output delay. | 150.00 | 150.00 | 150.00 | ns, Min |
| $T_{MCCKL}$ | Master CCLK clock Low time duty cycle. | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $T_{MCCKH}$ | Master CCLK clock High time duty cycle. | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $F_{MCCK}$ | Master CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| | Master CCLK frequency for AES encrypted x16.(2) | 50.00 | 50.00 | 50.00 | MHz, Max |
| $F_{MCCK\_START}$ | Master CCLK frequency at start of configuration. | 3.00 | 3.00 | 3.00 | MHz, Typ |
| $F_{MCCKTOL}$ | Frequency tolerance, master mode with respect to nominal CCLK. | ±50 | ±50 | ±50 | %, Max |
| **CCLK Input (Slave Modes)** | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{SCCK}$ | Slave CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **EMCCLK Input (Master Mode)** | | | | | |
| $T_{EMCCKL}$ | External master CCLK Low time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{EMCCKH}$ | External master CCLK High time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{EMCCK}$ | External master CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Internal Configuration Access Port** | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | |
| $T_{DCCK}$/ $T_{CCKD}$ | $D_{IN}$ setup/hold. | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | ns, Min |
| $T_{CCO}$ | $D_{OUT}$ clock to out. | 8.00 | 8.00 | 8.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | |
| $T_{SMDCCK}$/ $T_{SMCCKD}$ | D[31:00] setup/hold. | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | ns, Min |

*Table 51:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{SMCSCCK}$/<br>$T_{SMCCKCS}$ | CSI_B setup/hold. | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | ns, Min |
| $T_{SMWCCK}$/<br>$T_{SMCCKW}$ | RDWR_B setup/hold. | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required). | 7.00 | 7.00 | 7.00 | ns, Max |
| $T_{SMCO}$ | D[31:00] clock to out in readback. | 8.00 | 8.00 | 8.00 | ns, Max |
| $F_{RBCCK}$ | Readback frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | |
| $T_{TAPTCK}$/<br>$T_{TCKTAP}$ | TMS and TDI setup/hold. | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output. | 7.00 | 7.00 | 7.00 | ns, Max |
| $F_{TCK}$ | TCK frequency. | 66.00 | 66.00 | 66.00 | MHz, Max |
| **SPI Flash Master Mode Programming Switching** | | | | | |
| $T_{SPIDCC}$/<br>$T_{SPICCD}$ | D[03:00] setup/hold. | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | ns, Min |
| $T_{SPICCM}$ | MOSI clock to out. | 8.00 | 8.00 | 8.00 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out. | 8.00 | 8.00 | 8.00 | ns, Max |
| **STARTUPE2 Ports** | | | | | |
| $T_{USRCCLKO}$ | STARTUPE2 USRCCLKO input to CCLK output. | 0.50/6.70 | 0.50/7.50 | 0.50/7.50 | ns, Min/Max |
| $F_{CFGMCLK}$ | STARTUPE2 CFGMCLK output frequency. | 65.00 | 65.00 | 65.00 | MHz, Typ |
| $F_{CFGMCLKTOL}$ | STARTUPE2 CFGMCLK output frequency tolerance. | ±50 | ±50 | ±50 | %, Max |
| **Device DNA Access Port** | | | | | |
| $F_{DNACK}$ | DNA access port (DNA_PORT). | 100.00 | 100.00 | 100.00 | MHz, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].
2. See the *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] for a list of devices that support bitstream encryption.

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