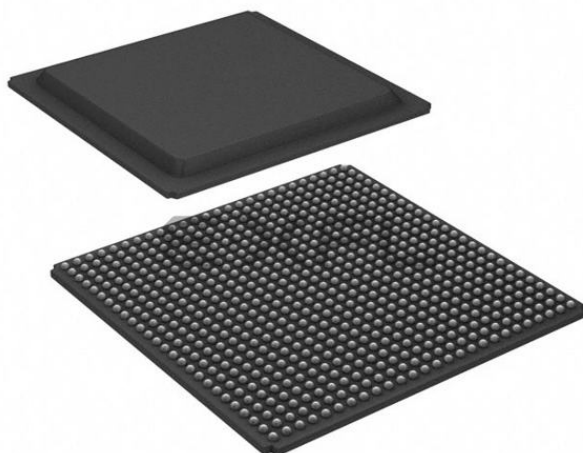




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8000
Number of Logic Elements/Cells	102400
Total RAM Bits	4423680
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s100-2fgga676c

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.10	-0.10
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 5	Note 5
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 6	Note 6
LVC MOS25	-0.300	0.7	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 6	Note 6
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.10	-0.10
PCI33_3	-0.400	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.50	-0.50
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.00	-13.00
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.90	-8.90
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.00	-13.00
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.90	-8.90
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.00	-8.00
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.40	-13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.

LVDS DC Specifications (LVDS_25)

Table 11: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage.		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	247	350	600	mV
V_{OCM}	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage.		0.300	1.200	1.500	V

Notes:

- Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

Table 14: Spartan-7 Device Production Software and Speed Specification Release

Device	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range					
	1.0V					0.95V
	-2C	-2I	-1C	-1I	-1Q	-1LI
XC7S6	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S15	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S25	Vivado tools 2017.4 v1.20				Vivado tools 2018.1 v1.21	Vivado tools 2017.4 v1.20
XC7S50	Vivado tools 2017.2 v1.17				Vivado tools 2017.3 v1.19	Vivado tools 2017.2 v1.17
XC7S75	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XC7S100	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XA7S6	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S15	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S25	N/A	Vivado tools 2018.1 v1.15	N/A	Vivado tools 2018.1 v1.15		N/A
XA7S50	N/A	Vivado tools 2017.3 v1.12	N/A	Vivado tools 2017.3 v1.12		N/A
XA7S75	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S100	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics, page 12](#).

Table 15: Networking Applications Interface Performances

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver ⁽¹⁾	680	600	600	Mb/s

Table 19: Input Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁵⁾	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁵⁾	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0 ⁽⁵⁾	–

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in [Figure 1](#).
5. The value given is the differential input voltage.

Table 20: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0 ⁽²⁾	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 ⁽²⁾	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0 ⁽²⁾	0
PPDS_25	PPDS_25	100	0	0 ⁽²⁾	0
RS DS_25	RS DS_25	100	0	0 ⁽²⁾	0
TMDS_33	TMDS_33	50	0	0 ⁽²⁾	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Table 22: OLOGIC Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK.	0.71/−0.11	0.84/−0.11	0.84/−0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK.	0.73/−0.14	0.89/−0.14	0.89/−0.14	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out.	0.49	0.56	0.56	ns
T _{RQ_OLOGIC}	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T _{GSRQ_OLOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T _{RPW_OLOGIC}	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 24: OSERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T _{OSDCK_D} / T _{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T _{OSDCK_T} / T _{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/−0.13	0.88/−0.13	0.88/−0.13	ns
T _{OSDCK_T2} / T _{OSCKD_T2}	T input setup/hold with respect to CLKDIV.	0.34/−0.13	0.39/−0.13	0.39/−0.13	ns
T _{OSCKCK_OCE} / T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSCKCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T _{OSCKCK_TCE} / T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ out.	0.92	1.11	1.11	ns

CLB Switching Characteristics

Table 27: CLB Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T _{ILO}	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T _{AXA}	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T _{AXB}	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T _{AXC}	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T _{AXD}	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max
T _{BXB}	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T _{BXD}	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T _{CXC}	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T _{CXD}	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T _{DXD}	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max
Sequential Delays					
T _{CKO}	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T _{AS} /T _{AH}	AN – DN input to CLK on A – D flip-flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D flip-flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T _{SRMIN}	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F _{TOG}	Toggle frequency (for export control).	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 28: CLB Distributed RAM Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T _{SHCKO}	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
T _{CECK_LRAM} /T _{CKCE_LRAM}	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T _{MPW_LRAM}	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T _{MCP}	Minimum clock period.	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: CLB Shift Register Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T _{REG}	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T _{MPW_SHFREG}	Minimum pulse width.	0.86	0.98	0.98	ns, Min

Table 30: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
F _{MAX_CAS_RF_DELAYED_WRITE}	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

Notes:

1. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
6. T_{RCKO_POINTERS} includes both T_{RCKO_RDCOUNT} and T_{RCKO_WRCOUNT}.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{DSPDO_PCIN_CARRYCASCOUT}	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
T _{DSPCKO_P_PREG}	CLK PREG to P output.	0.37	0.44	0.44	ns
T _{DSPCKO_CARRYCASCOUT_PREG}	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
T _{DSPCKO_P_MREG}	CLK MREG to P output.	1.93	2.31	2.31	ns
T _{DSPCKO_CARRYCASCOUT_MREG}	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
T _{DSPCKO_CARRYCASCOUT_ADREG_MULT}	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
T _{DSPCKO_CARRYCASCOUT_{AREG; BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					
F _{MAX}	With all registers used.	550.66	464.25	464.25	MHz
F _{MAX_PATDET}	With pattern detector.	465.77	392.93	392.93	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	305.62	257.47	257.47	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG.	346.26	290.44	290.44	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

Table 35: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BHCKO_O}	BUFH delay from I to O.	0.11	0.13	0.13	ns
T _{BHCKK_CE} / T _{BHCKC_CE}	CE pin setup and hold.	0.22/0.15	0.28/0.21	0.28/0.21	ns
Maximum Frequency					
F _{MAX_BUFH}	Horizontal clock buffer (BUFH).	628.00	464.00	464.00	MHz

Table 36: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
T _{DCD_CLK}	Global clock tree duty-cycle distortion. ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew. ⁽²⁾	XC7S6	0.05	0.06	0.06	ns
		XC7S15	0.05	0.06	0.06	ns
		XC7S25	0.26	0.26	0.26	ns
		XC7S50	0.26	0.26	0.26	ns
		XC7S75	0.33	0.36	0.36	ns
		XC7S100	0.33	0.36	0.36	ns
		XA7S6	0.05	0.06	N/A	ns
		XA7S15	0.05	0.06	N/A	ns
		XA7S25	0.26	0.26	N/A	ns
		XA7S50	0.26	0.26	N/A	ns
		XA7S75	0.33	0.36	N/A	ns
		XA7S100	0.33	0.36	N/A	ns
T _{DCD_BUFIO}	I/O clock tree duty cycle distortion.	All	0.14	0.14	0.14	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region.	All	0.03	0.03	0.03	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion.	All	0.18	0.18	0.18	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx timing analysis tools to evaluate clock skew specific to your application.

Table 37: MMCM Specification (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DEN} / T _{MMCMCKD_DEN}	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T _{MMCMDCK_DWE} / T _{MMCMCKD_DWE}	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: PLL Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F _{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 38: PLL Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3			
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision. ⁽⁴⁾	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency. ⁽⁵⁾	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DI} / T _{PLLCKD_DI}	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/−0.40	3.17/−0.40	3.17/−0.40	ns
		XC7S15	2.76/−0.40	3.17/−0.40	3.17/−0.40	ns
		XC7S25	2.67/−0.37	3.12/−0.37	3.12/−0.37	ns
		XC7S50	2.66/−0.28	3.11/−0.28	3.11/−0.28	ns
		XC7S75	2.91/−0.33	3.36/−0.33	3.36/−0.33	ns
		XC7S100	2.91/−0.33	3.36/−0.33	3.36/−0.33	ns
		XA7S6	2.76/−0.40	3.17/−0.40	N/A	ns
		XA7S15	2.76/−0.40	3.17/−0.40	N/A	ns
		XA7S25	2.67/−0.37	3.12/−0.37	N/A	ns
		XA7S50	2.66/−0.28	3.11/−0.28	N/A	ns
		XA7S75	2.91/−0.33	3.36/−0.33	N/A	ns
		XA7S100	2.91/−0.33	3.36/−0.33	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input flip-flop or latch.

Table 48: Sample Window

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{SAMP}	Sampling error at receiver pins. ⁽¹⁾	0.64	0.70	0.70	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO. ⁽²⁾	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 51: Configuration Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{SMCSCCK} / T _{SMCCKCS}	CSI_B setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T _{SMWCCK} / T _{SMCCKW}	RDWR_B setup/hold.	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required).	7.00	7.00	7.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F _{RBCK}	Readback frequency.	100.00	100.00	100.00	MHz, Max
Boundary-Scan Port Timing Specifications					
T _{TAPTCK} / T _{TCKTAP}	TMS and TDI setup/hold.	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F _{TCK}	TCK frequency.	66.00	66.00	66.00	MHz, Max
SPI Flash Master Mode Programming Switching					
T _{SPIDCC} / T _{SPICCD}	D[03:00] setup/hold.	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out.	8.00	8.00	8.00	ns, Max
T _{SPICFC}	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
STARTUPE2 Ports					
T _{USRCCLKO}	STARTUPE2 USRCCLKO input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
F _{CFGMCLK}	STARTUPE2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
F _{CFGMCLKTOL}	STARTUPE2 CFGMCLK output frequency tolerance.	±50	±50	±50	%, Max
Device DNA Access Port					
F _{DNACK}	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max

Notes:

- To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].
- See the *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] for a list of devices that support bitstream encryption.

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the [Clocking Wizard](#) in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12 , updated Vivado tools version to 2018.2.1. In Table 13 , moved all speed grades for all devices to Production. In Table 14 , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12 , updated Vivado tools version to 2018.2. In Table 13 , moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14 , added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5 , updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6 , updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13 , moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14 , added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36 , Table 39 , Table 40 , Table 41 , Table 42 , Table 44 , Table 45 , and Table 46 , changed parameter value for XA7S50 to N/A. In Table 49 , added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12 , updated Vivado tools version to 2017.4. In Table 13 , moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14 , added Vivado tools version for XC7S25. Added Note 2 to Table 16 . In Table 49 , added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction . Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2 . Added -1Q (1.0V) speed grade to Table 5 , and Table 13 to Table 16 . In Table 12 , updated Vivado tools version to 2017.3. In Table 49 , added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added <i>XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171)</i> to References .
06/20/2017	1.2	Updated paragraph before Table 6 . In Table 12 , updated Vivado tools version to 2017.2. In Table 13 , moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1 . In Table 14 , added Vivado tools version for XC7S50. In Table 49 , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2 . In Table 12 , updated Vivado tools version to 2016.4. In Table 13 , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15 . In Table 25 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed BUFMR from Note 1 in Table 34 . In Table 49 , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.