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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8000
Number of Logic Elements/Cells	102400
Total RAM Bits	4423680
Number of I/O	338
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s100-l1fgga484i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
$V_{IN}^{(2)(3)(4)}$	I/O input voltage.	−0.4	$V_{CCO} + 0.55$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33. ⁽⁵⁾	−0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply.	−0.5	2.0	V
XADC				
V_{CCADC}	XADC supply relative to GNDADC.	−0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC.	−0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient).	−65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies. ⁽⁶⁾	—	+220	°C
	Maximum soldering temperature for Pb-free component bodies. ⁽⁶⁾	—	+260	°C
T_j	Maximum junction temperature. ⁽⁶⁾	—	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
- See Table 9 for TMDS_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
$V_{CCINT}^{(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
$V_{CCBRAM}^{(3)}$	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
$V_{CCO}^{(4)(5)}$	Supply voltage for HR I/O banks.	1.14	–	3.465	V
$V_{IN}^{(6)}$	I/O input voltage.	–0.20	–	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMD5_33. ⁽⁷⁾	–0.20	–	2.625	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(9)}$	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices.	–40	–	125	°C

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
- If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- The lower absolute voltage specification always applies.
- See Table 9 for TMD5_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

LVDS DC Specifications (LVDS_25)

Table 11: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage.		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	247	350	600	mV
V_{OCM}	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage.		0.300	1.200	1.500	V

Notes:

- Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

Table 15: Networking Applications Interface Performances (Cont'd)

Description	V _{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
DDR LVDS receiver ⁽¹⁾	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator⁽¹⁾

Memory Standard	V _{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
4:1 Memory Controllers				
DDR3	800 ⁽²⁾	667	667	Mb/s
DDR3L	800 ⁽²⁾	667	667	Mb/s
DDR2	800 ⁽²⁾	667	667	Mb/s
2:1 Memory Controllers				
DDR3	800 ⁽²⁾	667	667	Mb/s
DDR3L	800 ⁽²⁾	667	667	Mb/s
DDR2	800 ⁽²⁾	667	667	Mb/s
LPDDR2	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 7].
2. The maximum PHY rate is 667 Mb/s in the FTGB196 package.

IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPi} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOPo} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTp} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTp} when the INTERMDISABLE pin is used.

Table 17: IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	V _{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVTTL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVTTL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns
LVTTL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVTTL_S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVTTL_S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVTTL_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVTTL_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVTTL_F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVTTL_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVTTL_F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns
LVDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MINI_LVDS_25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLVDS_25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RSDS_25 (point to point)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PPDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TMDS_33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns
PCI33_3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HSUL_12_S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HSUL_12_F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
HSTL_II_18_S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HSTL_I_F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns
HSTL_II_F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HSTL_I_18_F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	V _{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
HSTL_II_18_F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_HSTL_I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVC MOS33_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVC MOS33_S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVC MOS33_S12	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVC MOS33_S16	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns
LVC MOS33_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVC MOS33_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS33_F12	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS33_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS25_S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVC MOS25_S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns
LVC MOS25_S12	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVC MOS25_S16	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVC MOS25_F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS25_F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS25_F12	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns
LVC MOS25_F16	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVC MOS18_S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVC MOS18_S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS18_S12	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS18_S16	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns
LVC MOS18_S24	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS18_F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVC MOS18_F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F12	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F16	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns
LVC MOS18_F24	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS15_S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVC MOS15_S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS15_S12	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_S16	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

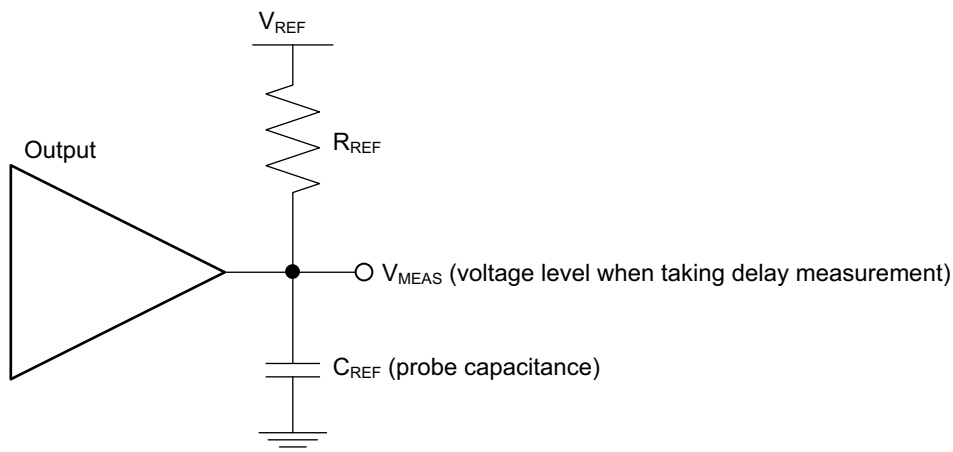
Table 19 shows the test setup parameters used for measuring input delay.

Table 19: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	—
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	—
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	—
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	—
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	—
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	—
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	—
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	—
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	$V_{REF} - 0.575$	$V_{REF} + 0.575$	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(5)}$	—
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	$0.675 - 0.125$	$0.675 + 0.125$	$0^{(5)}$	—
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(5)}$	—
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
LVDS_25, 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(5)}$	—
BLVDS_25, 2.5V	BLVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	$0^{(5)}$	—
MINI_LVDS_25, 2.5V	MINI_LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	$0^{(5)}$	—

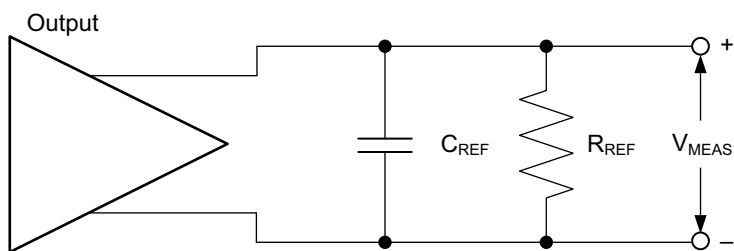
Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-092616

Figure 1: Single-ended Test Setup



X16640-092616

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 20](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Input Serializer/Deserializer Switching Characteristics

Table 23: ISERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
T _{ISCKK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/−0.01	0.72/−0.01	0.72/−0.01	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	−0.10/0.36	−0.10/0.40	−0.10/0.40	ns
Setup/Hold for Data Lines					
T _{ISDCK_D} / T _{ISCKD_D}	D pin setup/hold with respect to CLK.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY). ⁽¹⁾	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin setup/hold with respect to CLK at DDR mode.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin setup/hold with respect to CLK at DDR mode (using IDELAY). ⁽¹⁾	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T _{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T _{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

- Recorded at 0 tap value.

Output Serializer/Deserializer Switching Characteristics

Table 24: OSERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T _{OSDCK_D} / T _{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T _{OSDCK_T} / T _{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/−0.13	0.88/−0.13	0.88/−0.13	ns
T _{OSDCK_T2} / T _{OSCKD_T2}	T input setup/hold with respect to CLKDIV.	0.34/−0.13	0.39/−0.13	0.39/−0.13	ns
T _{OSCKCK_OCE} / T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSCKCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T _{OSCKCK_TCE} / T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ out.	0.92	1.11	1.11	ns

Input/Output Delay Switching Characteristics

Table 25: Input/Output Delay Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.00. ⁽¹⁾	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00. ⁽¹⁾	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00. ⁽¹⁾	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
T _{IDELAYRESOLUTION}	IDELAY chain delay resolution.	1/(32 x 2 x F _{REF})			μs
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T _{IDCCK_INC} /T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T _{IDCCK_RST} /T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Block RAM and FIFO Switching Characteristics

Table 30: Block RAM and FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T _{RCKO_DO} and T _{RCKO_DO_REG}	Clock CLK to DOUT output (without output register). ⁽¹⁾⁽²⁾	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register). ⁽³⁾⁽⁴⁾	0.74	0.89	0.89	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register). ⁽¹⁾⁽²⁾	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register). ⁽³⁾⁽⁴⁾	0.81	0.94	0.94	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with cascade (without output register). ⁽¹⁾	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register). ⁽³⁾	1.28	1.46	1.46	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs. ⁽⁵⁾	0.87	1.05	1.05	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs. ⁽⁶⁾	1.02	1.15	1.15	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{TRCKC_ADDRA} /T _{TRCKC_ADDRA}	ADDR inputs. ⁽⁷⁾	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
T _{TRDCK_DI_WF_NC} /T _{TRCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode. ⁽⁸⁾	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
T _{TRDCK_DI_RF} /T _{TRCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode. ⁽⁸⁾	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
T _{TRDCK_DI_ECC} /T _{TRCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode. ⁽⁸⁾	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
T _{TRDCK_DI_ECCW} /T _{TRCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only. ⁽⁸⁾	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

Clock Buffers and Networks

Table 32: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BCCCK_CE} /T _{BCCCK_CE} ⁽¹⁾	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCK_S} /T _{BCCCK_S} ⁽¹⁾	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCKO_O} ⁽²⁾	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F _{MAX_BUFG}	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 33: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					
F _{MAX_BUFIO}	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BRCKO_O}	Clock to out delay from I to O.	0.76	0.99	0.99	ns
T _{BRCKO_O_BYP}	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T _{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F _{MAX_BUFR} ⁽¹⁾	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

MMCM Switching Characteristics

Table 37: MMCM Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F _{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty-cycle precision. ⁽⁴⁾	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time.	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Device Pin-to-Pin Output Parameter Guidelines

Table 39: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs <i>without</i> MMCM/PLL (near clock region). ⁽²⁾	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/−0.40	3.17/−0.40	3.17/−0.40	ns
		XC7S15	2.76/−0.40	3.17/−0.40	3.17/−0.40	ns
		XC7S25	2.67/−0.37	3.12/−0.37	3.12/−0.37	ns
		XC7S50	2.66/−0.28	3.11/−0.28	3.11/−0.28	ns
		XC7S75	2.91/−0.33	3.36/−0.33	3.36/−0.33	ns
		XC7S100	2.91/−0.33	3.36/−0.33	3.36/−0.33	ns
		XA7S6	2.76/−0.40	3.17/−0.40	N/A	ns
		XA7S15	2.76/−0.40	3.17/−0.40	N/A	ns
		XA7S25	2.67/−0.37	3.12/−0.37	N/A	ns
		XA7S50	2.66/−0.28	3.11/−0.28	N/A	ns
		XA7S75	2.91/−0.33	3.36/−0.33	N/A	ns
		XA7S100	2.91/−0.33	3.36/−0.33	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input flip-flop or latch.

Table 48: Sample Window

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{SAMP}	Sampling error at receiver pins. ⁽¹⁾	0.64	0.70	0.70	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO. ⁽²⁾	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12 , updated Vivado tools version to 2018.2.1. In Table 13 , moved all speed grades for all devices to Production. In Table 14 , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12 , updated Vivado tools version to 2018.2. In Table 13 , moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14 , added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5 , updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6 , updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13 , moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14 , added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36 , Table 39 , Table 40 , Table 41 , Table 42 , Table 44 , Table 45 , and Table 46 , changed parameter value for XA7S50 to N/A. In Table 49 , added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12 , updated Vivado tools version to 2017.4. In Table 13 , moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14 , added Vivado tools version for XC7S25. Added Note 2 to Table 16 . In Table 49 , added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction . Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2 . Added -1Q (1.0V) speed grade to Table 5 , and Table 13 to Table 16 . In Table 12 , updated Vivado tools version to 2017.3. In Table 49 , added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added <i>XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171)</i> to References .
06/20/2017	1.2	Updated paragraph before Table 6 . In Table 12 , updated Vivado tools version to 2017.2. In Table 13 , moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1 . In Table 14 , added Vivado tools version for XC7S50. In Table 49 , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2 . In Table 12 , updated Vivado tools version to 2016.4. In Table 13 , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15 . In Table 25 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed BUFMR from Note 1 in Table 34 . In Table 49 , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.