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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	368640
Number of I/O	100
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s15-1csga225c

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
$V_{CCINT}^{(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
$V_{CCBRAM}^{(3)}$	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
$V_{CCO}^{(4)(5)}$	Supply voltage for HR I/O banks.	1.14	–	3.465	V
$V_{IN}^{(6)}$	I/O input voltage.	–0.20	–	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33. ⁽⁷⁾	–0.20	–	2.625	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(9)}$	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices.	–40	–	125	°C

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
- If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- The lower absolute voltage specification always applies.
- See Table 9 for TMDS_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V _{DRINT}	Data retention V _{CCINT} voltage (below which configuration data might be lost).	0.75	–	–	V
V _{DRI}	Data retention V _{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I _{REF}	V _{REF} leakage current per pin.	–	–	15	μA
I _L	Input or output leakage current per pin (sample-tested).	–	–	15	μA
C _{IN} ⁽²⁾	Die input capacitance at the pad.	–	–	8	pF
I _{RPU}	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 3.3V.	90	–	330	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 2.5V.	68	–	250	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.8V.	34	–	220	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.5V.	23	–	150	μA
	Pad pull-up (when selected) at V _{IN} = 0V, V _{CCO} = 1.2V.	12	–	120	μA
I _{RPD}	Pad pull-down (when selected) at V _{IN} = 3.3V.	68	–	330	μA
I _{CCADC}	Analog supply current, analog circuits in powered up state.	–	–	25	mA
I _{BATT} ⁽³⁾	Battery supply current.	–	–	150	nA
R _{IN_TERM} ⁽⁴⁾	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_40).	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_50).	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_60).	44	60	83	Ω
n	Temperature diode ideality factor.	–	1.010	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 13](#) correlates the current status of each Spartan-7 device on a per speed grade basis.

Table 13: Spartan-7 Device Speed Grade Designations

Device	Speed Grade, Temperature Range, and V _{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S6			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S15			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S25			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S50			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S75			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S100			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XA7S6			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S15			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S25			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S50			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S75			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S100			-2I (1.0V), -1I (1.0V), -1Q (1.0V)

Notes:

1. The lowest power -1LI devices, where V_{CCINT} = 0.95V, are listed in the Vivado Design Suite as -1IL.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

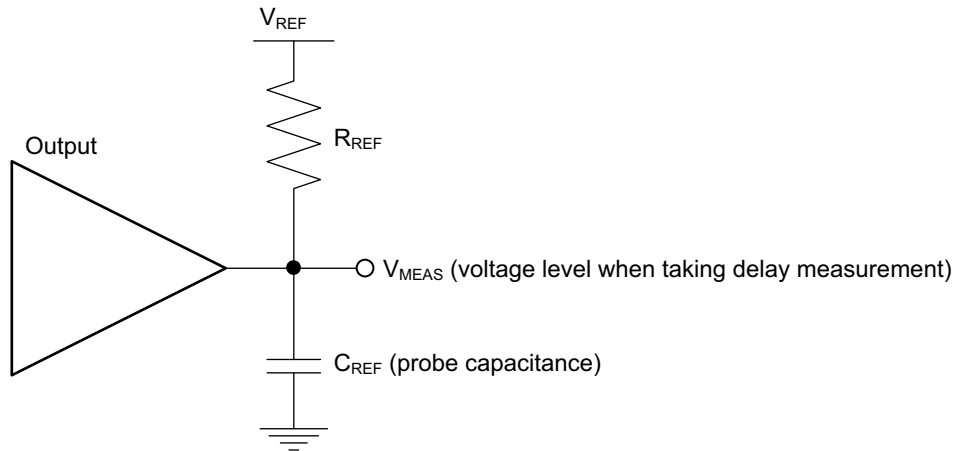
[Table 14](#) lists the production released Spartan-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	V _{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
HSTL_II_18_F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_HSTL_I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVC MOS33_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVC MOS33_S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVC MOS33_S12	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVC MOS33_S16	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns
LVC MOS33_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVC MOS33_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS33_F12	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS33_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS25_S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVC MOS25_S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns
LVC MOS25_S12	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVC MOS25_S16	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVC MOS25_F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS25_F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS25_F12	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns
LVC MOS25_F16	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVC MOS18_S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVC MOS18_S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS18_S12	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS18_S16	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns
LVC MOS18_S24	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS18_F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVC MOS18_F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F12	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F16	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns
LVC MOS18_F24	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS15_S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVC MOS15_S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS15_S12	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_S16	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns

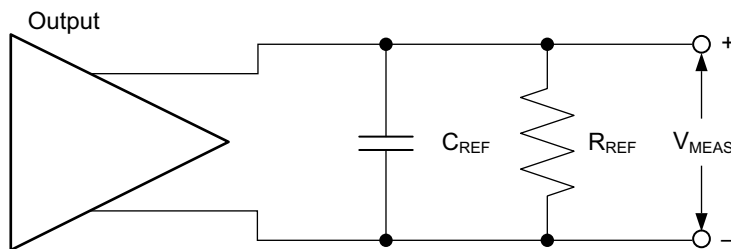
Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-092616

Figure 1: Single-ended Test Setup



X16640-092616

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 20](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 22: OLOGIC Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK.	0.71/–0.11	0.84/–0.11	0.84/–0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK.	0.73/–0.14	0.89/–0.14	0.89/–0.14	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out.	0.49	0.56	0.56	ns
T _{RQ_OLOGIC}	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T _{GSRQ_OLOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T _{RPW_OLOGIC}	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 23: ISERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
T _{ISCKK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/−0.01	0.72/−0.01	0.72/−0.01	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	−0.10/0.36	−0.10/0.40	−0.10/0.40	ns
Setup/Hold for Data Lines					
T _{ISDCK_D} / T _{ISCKD_D}	D pin setup/hold with respect to CLK.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY). ⁽¹⁾	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin setup/hold with respect to CLK at DDR mode.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin setup/hold with respect to CLK at DDR mode (using IDELAY). ⁽¹⁾	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T _{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T _{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

- Recorded at 0 tap value.

Table 26: IO_FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs.	0.60	0.68	0.68	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
T _{IFFCK_WREN} / T _{IFFKC_WREN}	WREN to WRCLK.	0.47/-0.01	0.53/-0.01	0.53/-0.01	ns
T _{OFFCK_RDEN} / T _{OFFKC_RDEN}	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

Block RAM and FIFO Switching Characteristics

Table 30: Block RAM and FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T _{RCKO_DO} and T _{RCKO_DO_REG}	Clock CLK to DOUT output (without output register). ⁽¹⁾⁽²⁾	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register). ⁽³⁾⁽⁴⁾	0.74	0.89	0.89	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register). ⁽¹⁾⁽²⁾	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register). ⁽³⁾⁽⁴⁾	0.81	0.94	0.94	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with cascade (without output register). ⁽¹⁾	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register). ⁽³⁾	1.28	1.46	1.46	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs. ⁽⁵⁾	0.87	1.05	1.05	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs. ⁽⁶⁾	1.02	1.15	1.15	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{RCKC_ADDRA} / T _{RCKC_ADDRA}	ADDR inputs. ⁽⁷⁾	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode. ⁽⁸⁾	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
T _{RDCK_DI_RF} / T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode. ⁽⁸⁾	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
T _{RDCK_DI_ECC} / T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode. ⁽⁸⁾	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
T _{RDCK_DI_ECCW} / T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only. ⁽⁸⁾	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

DSP48E1 Switching Characteristics

Table 31: DSP48E1 Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK.	0.30/ 0.13	0.37/ 0.14	0.37/ 0.14	ns
T _{DSPDCK_B_BREG} / T _{DSPCKD_B_BREG}	B input to B register CLK.	0.38/ 0.16	0.45/ 0.18	0.45/ 0.18	ns
T _{DSPDCK_C_CREG} / T _{DSPCKD_C_CREG}	C input to C register CLK.	0.20/ 0.19	0.24/ 0.21	0.24/ 0.21	ns
T _{DSPDCK_D_DREG} / T _{DSPCKD_D_DREG}	D input to D register CLK.	0.32/ 0.27	0.42/ 0.27	0.42/ 0.27	ns
T _{DSPDCK_ACIN_AREG} / T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK.	0.27/ 0.13	0.32/ 0.14	0.32/ 0.14	ns
T _{DSPDCK_BCIN_BREG} / T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK.	0.29/ 0.16	0.36/ 0.18	0.36/ 0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
T _{DSPDCK_{A,B}_MREG_MULT} / T _{DSPCKD_{A,B}_MREG_MULT}	{A, B} input to M register CLK using multiplier.	2.76/ -0.01	3.29/ -0.01	3.29/ -0.01	ns
T _{DSPDCK_{A,D}_ADREG} / T _{DSPCKD_{A,D}_ADREG}	{A, D} input to AD register CLK.	1.48/ -0.02	1.76/ -0.02	1.76/ -0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
T _{DSPDCK_{A,B}_PREG_MULT} / T _{DSPCKD_{A,B}_PREG_MULT}	{A, B} input to P register CLK using multiplier.	4.60/ -0.28	5.48/ -0.28	5.48/ -0.28	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier.	4.50/ -0.73	5.35/ -0.73	5.35/ -0.73	ns
T _{DSPDCK_{A,B}_PREG} / T _{DSPCKD_{A,B}_PREG}	A or B input to P register CLK not using multiplier.	1.98/ -0.28	2.35/ -0.28	2.35/ -0.28	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier.	1.76/ -0.26	2.10/ -0.26	2.10/ -0.26	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK.	1.51/ -0.15	1.80/ -0.15	1.80/ -0.15	ns
Setup and Hold Times of the CE Pins					
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK.	0.42/ 0.08	0.52/ 0.11	0.52/ 0.11	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK.	0.34/ 0.11	0.42/ 0.13	0.42/ 0.13	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK.	0.43/ -0.03	0.52/ -0.03	0.52/ -0.03	ns

Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
Setup and Hold Times of the RST Pins					
T _{DSPDCK_{RSTA; RSTB}_{AREG; BREG}} / T _{DSPCKD_{RSTA; RSTB}_{AREG; BREG}}	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
T _{DSPDCK_RSTC_CREG} / T _{DSPCKD_RSTC_CREG}	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
T _{DSPDCK_RSTD_DREG} / T _{DSPCKD_RSTD_DREG}	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
T _{DSPDCK_RSTM_MREG} / T _{DSPCKD_RSTM_MREG}	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
T _{DSPDCK_RSTP_PREG} / T _{DSPCKD_RSTP_PREG}	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
T _{DSPDO_A_CARRYOUT_MULT}	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
T _{DSPDO_D_P_MULT}	D input to P output using multiplier.	4.26	5.07	5.07	ns
T _{DSPDO_B_P}	B input to P output not using multiplier.	1.75	2.08	2.08	ns
T _{DSPDO_C_P}	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
T _{DSPDO_{A; B}_{ACOUT; BCOUT}}	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
T _{DSPDO_{A; B}_CARRYCASCOUT_MULT}	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
T _{DSPDO_D_CARRYCASCOUT_MULT}	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
T _{DSPDO_{A; B}_CARRYCASCOUT}	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
T _{DSPDO_C_CARRYCASCOUT}	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
T _{DSPDO_ACIN_P_MULT}	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
T _{DSPDO_ACIN_P}	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
T _{DSPDO_ACIN_ACOUT}	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
T _{DSPDO_ACIN_CARRYCASCOUT_MULT}	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
T _{DSPDO_ACIN_CARRYCASCOUT}	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
T _{DSPDO_PCIN_P}	PCIN input to P output.	1.28	1.52	1.52	ns

Clock Buffers and Networks

Table 32: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BCCCK_CE} /T _{BCCCK_CE} ⁽¹⁾	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCK_S} /T _{BCCCK_S} ⁽¹⁾	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCKO_O} ⁽²⁾	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F _{MAX_BUFG}	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCCKO_O} values.

Table 33: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					
F _{MAX_BUFIO}	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BRCKO_O}	Clock to out delay from I to O.	0.76	0.99	0.99	ns
T _{BRCKO_O_BYP}	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T _{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F _{MAX_BUFR} ⁽¹⁾	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 35: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BHCKO_O}	BUFH delay from I to O.	0.11	0.13	0.13	ns
T _{BHCKC_CE} / T _{BHCKC_CE}	CE pin setup and hold.	0.22/0.15	0.28/0.21	0.28/0.21	ns
Maximum Frequency					
F _{MAX_BUFH}	Horizontal clock buffer (BUFH).	628.00	464.00	464.00	MHz

Table 36: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
T _{DCD_CLK}	Global clock tree duty-cycle distortion. ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew. ⁽²⁾	XC7S6	0.05	0.06	0.06	ns
		XC7S15	0.05	0.06	0.06	ns
		XC7S25	0.26	0.26	0.26	ns
		XC7S50	0.26	0.26	0.26	ns
		XC7S75	0.33	0.36	0.36	ns
		XC7S100	0.33	0.36	0.36	ns
		XA7S6	0.05	0.06	N/A	ns
		XA7S15	0.05	0.06	N/A	ns
		XA7S25	0.26	0.26	N/A	ns
		XA7S50	0.26	0.26	N/A	ns
		XA7S75	0.33	0.36	N/A	ns
XA7S100	0.33	0.36	N/A	ns		
T _{DCD_BUFIO}	I/O clock tree duty cycle distortion.	All	0.14	0.14	0.14	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region.	All	0.03	0.03	0.03	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion.	All	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx timing analysis tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 37: MMCM Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F _{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty-cycle precision. ⁽⁴⁾	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time.	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Table 37: MMCM Specification (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DEN} / T _{MMCMCKD_DEN}	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T _{MMCMDCK_DWE} / T _{MMCMCKD_DWE}	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{MMCMCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: PLL Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F _{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 45: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.⁽¹⁾⁽²⁾						
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽³⁾ with MMCM.	XC7S6	2.73/-0.59	3.27/-0.59	3.27/-0.59	ns
		XC7S15	2.73/-0.59	3.27/-0.59	3.27/-0.59	ns
		XC7S25	2.69/-0.61	3.21/-0.61	3.21/-0.61	ns
		XC7S50	2.81/-0.62	3.35/-0.62	3.35/-0.62	ns
		XC7S75	2.81/-0.62	3.36/-0.62	3.36/-0.62	ns
		XC7S100	2.81/-0.62	3.36/-0.62	3.36/-0.62	ns
		XA7S6	2.73/-0.59	3.27/-0.59	N/A	ns
		XA7S15	2.73/-0.59	3.27/-0.59	N/A	ns
		XA7S25	2.69/-0.61	3.21/-0.61	N/A	ns
		XA7S50	2.81/-0.62	3.35/-0.62	N/A	ns
		XA7S75	2.81/-0.62	3.36/-0.62	N/A	ns
		XA7S100	2.81/-0.62	3.36/-0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 46: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.⁽¹⁾⁽²⁾						
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽³⁾ with PLL.	XC7S6	3.07/-0.17	3.69/-0.17	3.69/-0.17	ns
		XC7S15	3.07/-0.17	3.69/-0.17	3.69/-0.17	ns
		XC7S25	3.04/-0.19	3.64/-0.19	3.64/-0.19	ns
		XC7S50	3.15/-0.19	3.77/-0.19	3.77/-0.19	ns
		XC7S75	3.15/-0.19	3.78/-0.19	3.78/-0.19	ns
		XC7S100	3.15/-0.19	3.78/-0.19	3.78/-0.19	ns
		XA7S6	3.07/-0.17	3.69/-0.17	N/A	ns
		XA7S15	3.07/-0.17	3.69/-0.17	N/A	ns
		XA7S25	3.04/-0.19	3.64/-0.19	N/A	ns
		XA7S50	3.15/-0.19	3.77/-0.19	N/A	ns
		XA7S75	3.15/-0.19	3.78/-0.19	N/A	ns
		XA7S100	3.15/-0.19	3.78/-0.19	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 47: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _{PHCS}	Setup and hold of I/O clock.	-0.38/1.46	-0.38/1.73	-0.38/1.76	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12 , updated Vivado tools version to 2018.2.1. In Table 13 , moved all speed grades for all devices to Production. In Table 14 , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12 , updated Vivado tools version to 2018.2. In Table 13 , moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14 , added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5 , updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6 , updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13 , moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14 , added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36 , Table 39 , Table 40 , Table 41 , Table 42 , Table 44 , Table 45 , and Table 46 , changed parameter value for XA7S50 to N/A. In Table 49 , added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12 , updated Vivado tools version to 2017.4. In Table 13 , moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14 , added Vivado tools version for XC7S25. Added Note 2 to Table 16 . In Table 49 , added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction . Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2 . Added -1Q (1.0V) speed grade to Table 5 , and Table 13 to Table 16 . In Table 12 , updated Vivado tools version to 2017.3. In Table 49 , added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added <i>XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171)</i> to References .
06/20/2017	1.2	Updated paragraph before Table 6 . In Table 12 , updated Vivado tools version to 2017.2. In Table 13 , moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1 . In Table 14 , added Vivado tools version for XC7S50. In Table 49 , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2 . In Table 12 , updated Vivado tools version to 2016.4. In Table 13 , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15 . In Table 25 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed BUFMR from Note 1 in Table 34 . In Table 49 , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.

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