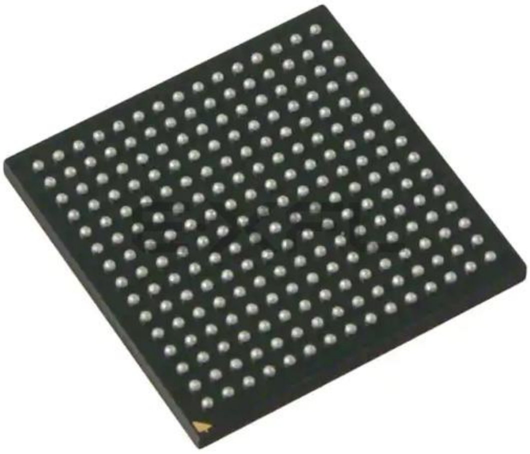
AMD Xilinx - XC7S15-1CSGA225I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	368640
Number of I/O	100
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s15-1csga225i

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Table 5: **Typical Quiescent Supply Current[(1)][(2)][(3)]** ***(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Spartan-7 device on a per speed grade basis.

Table 13: **Spartan-7 Device Speed Grade Designations**

Device	Speed Grade, Temperature Range, and V_{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S6			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S15			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S25			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S50			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S75			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XC7S100			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V)(1)
XA7S6			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S15			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S25			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S50			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S75			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S100			-2I (1.0V), -1I (1.0V), -1Q (1.0V)

Notes:

1. The lowest power -1LI devices, where V_{CCINT} = 0.95V, are listed in the Vivado Design Suite as -1IL.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 14 lists the production released Spartan-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 17: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVTTL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVTTL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns
LVTTL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVTTL_S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVTTL_S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVTTL_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVTTL_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVTTL_F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVTTL_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVTTL_F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns
LVDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MINI_LVDS_25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLVDS_25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RSDS_25 (point to point)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PPDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TMDS_33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns
PCI33_3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HSUL_12_S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HSUL_12_F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
HSTL_II_18_S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HSTL_I_F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns
HSTL_II_F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HSTL_I_18_F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns

Table 18: **IOB 3-state Output Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{IOTPHZ}	T input to pad high-impedance.	2.19	2.37	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output.	2.30	2.60	2.60	ns

Table 22: **OLOGIC Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK.	0.71/–0.11	0.84/–0.11	0.84/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK.	0.73/–0.14	0.89/–0.14	0.89/–0.14	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out.	0.49	0.56	0.56	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

Table 26: **IO_FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T_{OFFCKO_DO}	RDCLK to Q outputs.	0.60	0.68	0.68	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
T_{IFFCCK_WREN}/ T_{IFFCKC_WREN}	WREN to WRCLK.	0.47/–0.01	0.53/–0.01	0.53/–0.01	ns
T_{OFFCCK_RDEN}/ T_{OFFCKC_RDEN}	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
Maximum Frequency					
F_{MAX}	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

Block RAM and FIFO Switching Characteristics

Table 30: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (without output register).(1)(2)	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register).(3)(4)	0.74	0.89	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register).(1)(2)	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register).(3)(4)	0.81	0.94	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register).(1)	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register).(3)	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs.(5)	0.87	1.05	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs.(6)	1.02	1.15	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs.(7)	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.(8)	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode.(8)	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode.(8)	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only.(8)	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

Notes:

1. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
6. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier.	4.26	5.07	5.07	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier.	1.75	2.08	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output.	1.28	1.52	1.52	ns

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output.	0.37	0.44	0.44	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output.	1.93	2.31	2.31	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					
F_{MAX}	With all registers used.	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector.	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG.	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG.	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

MMCM Switching Characteristics

Table 37: **MMCM Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time.	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Table 37: **MMCM Specification *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Device Pin-to-Pin Output Parameter Guidelines

Table 39: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**[(1)]

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).(2)	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM[(1)]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 42: **Clock-Capable Clock Input to Output Delay With PLL**(1)

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.						
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL.(2)	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
$T_{ICKOFCS}$	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Table 45: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(3) with MMCM.	XC7S6	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S15	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S25	2.69/–0.61	3.21/–0.61	3.21/–0.61	ns
		XC7S50	2.81/–0.62	3.35/–0.62	3.35/–0.62	ns
		XC7S75	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XC7S100	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XA7S6	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S15	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S25	2.69/–0.61	3.21/–0.61	N/A	ns
		XA7S50	2.81/–0.62	3.35/–0.62	N/A	ns
		XA7S75	2.81/–0.62	3.36/–0.62	N/A	ns
		XA7S100	2.81/–0.62	3.36/–0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C. Typical values at T_j = +40°C.						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	±1	LSBs
Offset error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain error			–	–	±0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio(2)	SNR	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion(2)	THD	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	70	–	–	dB
Analog Inputs(3)						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
On-chip Sensors						
Temperature sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%

Configuration Switching Characteristics

Table 51: **Configuration Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Power-up Timing Characteristics					
T_{PL}(1)	Program latency.	5.00	5.00	5.00	ms, Max
T_{POR}(2)	Power-on reset (50 ms ramp rate time).	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time).	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width.	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)					
T_{ICCK}	Master CCLK output delay.	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency.	100.00	100.00	100.00	MHz, Max
	Master CCLK frequency for AES encrypted x16.(2)	50.00	50.00	50.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%, Max
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time.	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency.	100.00	100.00	100.00	MHz, Max
EMCCLK Input (Master Mode)					
T_{EMCCKL}	External master CCLK Low time.	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time.	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency.	100.00	100.00	100.00	MHz, Max
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency.	100.00	100.00	100.00	MHz, Max
Master/Slave Serial Mode Programming Switching					
T_{DCCK}/ T_{CCKD}	D_{IN} setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{CCO}	D_{OUT} clock to out.	8.00	8.00	8.00	ns, Max
SelectMAP Mode Programming Switching					
T_{SMDCCK}/ T_{SMCCKD}	D[31:00] setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min

Table 51: **Configuration Switching Characteristics *(Cont'd)***

Symbol	**Description**	**V_{CCINT} Operating Voltage and Speed Grade**			**Units**
		1.0V		**0.95V**	
		-2	**-1**	**-1L**	
$T_{SMCSCCK}$/ $T_{SMCCKCS}$	CSI_B setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{SMWCCK}/ T_{SMCCKW}	RDWR_B setup/hold.	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required).	7.00	7.00	7.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F_{RBCCK}	Readback frequency.	100.00	100.00	100.00	MHz, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/ T_{TCKTAP}	TMS and TDI setup/hold.	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency.	66.00	66.00	66.00	MHz, Max
SPI Flash Master Mode Programming Switching					
T_{SPIDCC}/ T_{SPICCD}	D[03:00] setup/hold.	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out.	8.00	8.00	8.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
STARTUPE2 Ports					
$T_{USRCCLKO}$	STARTUPE2 USRCCLKO input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE2 CFGMCLK output frequency tolerance.	±50	±50	±50	%, Max
Device DNA Access Port					
F_{DNACK}	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].
2. See the *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] for a list of devices that support bitstream encryption.

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)