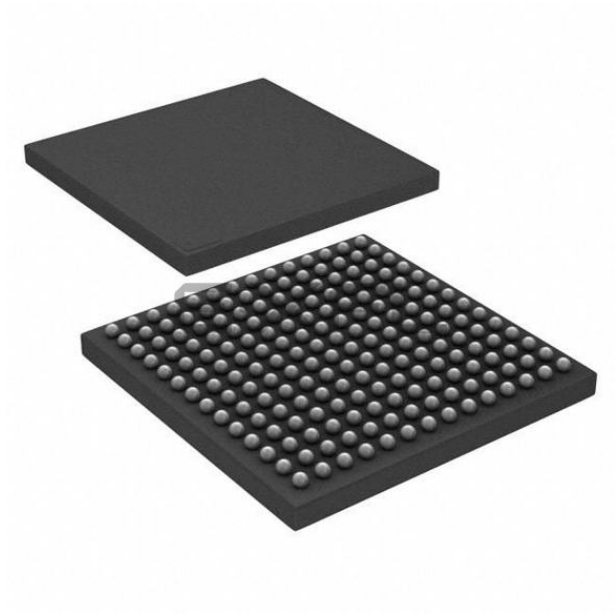
AMD Xilinx - XC7S15-2FTGB196I Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	368640
Number of I/O	100
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	196-LBGA, CSPBGA
Supplier Device Package	196-CSBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s15-2ftgb196i

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{IN}(2)(3)(4)	I/O input voltage.	–0.4	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33.(5)	–0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply.	–0.5	2.0	V
XADC				
V_{CCADC}	XADC supply relative to GNDADC.	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC.	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies.(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies.(6)	–	+260	°C
T_j	Maximum junction temperature.(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

Table 12: **Speed Specification Version By Device**

2018.2.1	Device
1.23	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
1.16	XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

Table 17: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVCMOS15_F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVCMOS15_F12	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVCMOS15_F16	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVCMOS12_S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVCMOS12_S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVCMOS12_S12	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns
LVCMOS12_F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVCMOS12_F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVCMOS12_F12	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SSTL15_S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SSTL18_I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns
SSTL18_II_S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIFF_SSTL135_S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIFF_SSTL15_S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIFF_SSTL18_I_S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIFF_SSTL18_II_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL15_F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SSTL18_I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL18_II_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL135_F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL15_F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns
DIFF_SSTL18_I_F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns
DIFF_SSTL18_II_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

Table 18 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

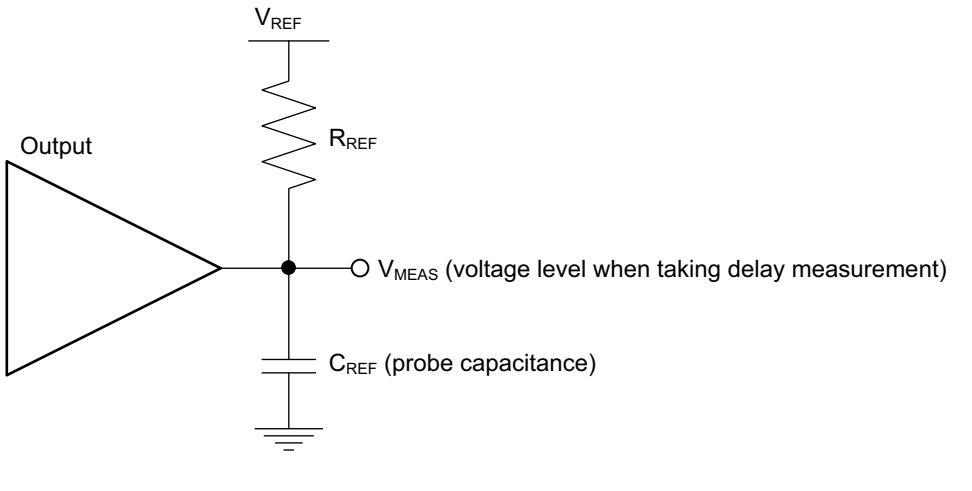

Figure 1: **Single-ended Test Setup**

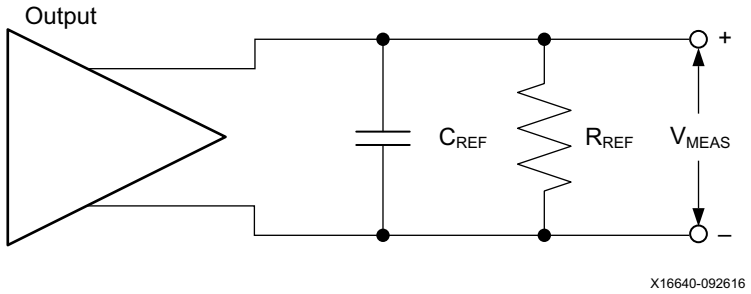

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 20.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 20: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Output Serializer/Deserializer Switching Characteristics

Table 24: **OSERDES Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{OSDCK_D}/ T_{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T_{OSDCK_T}/ T_{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/–0.13	0.88/–0.13	0.88/–0.13	ns
T_{OSDCK_T2}/ T_{OSCKD_T2}	T input setup/hold with respect to CLKDIV.	0.34/–0.13	0.39/–0.13	0.39/–0.13	ns
T_{OSCCK_OCE}/ T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T_{OSCCK_TCE}/ T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ out.	0.92	1.11	1.11	ns

Input/Output Delay Switching Characteristics

Table 25: **Input/Output Delay Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00.(1)	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00.(1)	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00.(1)	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution.	1/(32 x 2 x F_{REF})			µs
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

Notes:

1. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
6. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Clock Buffers and Networks

Table 32: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 33: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O.	0.76	0.99	0.99	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T_{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F_{MAX_BUFR}(1)	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

MMCM Switching Characteristics

Table 37: **MMCM Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time.	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Table 37: **MMCM Specification *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical.(1)	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3			
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency.(5)	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T_{PLLDCK_DADDR}/ T_{PLLCKD_DADDR}	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLDCK_DI}/ T_{PLLCKD_DI}	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLDCK_DEN}/ T_{PLLCKD_DEN}	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T_{PLLDCK_DWE}/ T_{PLLCKD_DWE}	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 39: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S15	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S25	2.67/–0.37	3.12/–0.37	3.12/–0.37	ns
		XC7S50	2.66/–0.28	3.11/–0.28	3.11/–0.28	ns
		XC7S75	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XC7S100	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XA7S6	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S15	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S25	2.67/–0.37	3.12/–0.37	N/A	ns
		XA7S50	2.66/–0.28	3.11/–0.28	N/A	ns
		XA7S75	2.91/–0.33	3.36/–0.33	N/A	ns
		XA7S100	2.91/–0.33	3.36/–0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 46: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL.	XC7S6	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S15	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S25	3.04/–0.19	3.64/–0.19	3.64/–0.19	ns
		XC7S50	3.15/–0.19	3.77/–0.19	3.77/–0.19	ns
		XC7S75	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XC7S100	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XA7S6	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S15	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S25	3.04/–0.19	3.64/–0.19	N/A	ns
		XA7S50	3.15/–0.19	3.77/–0.19	N/A	ns
		XA7S75	3.15/–0.19	3.78/–0.19	N/A	ns
		XA7S100	3.15/–0.19	3.78/–0.19	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 47: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock.	–0.38/1.46	–0.38/1.73	–0.38/1.76	ns

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: **Package Skew**[1]

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew.[2]	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

1. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

Configuration Switching Characteristics

Table 51: **Configuration Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Power-up Timing Characteristics					
T_{PL} (1)	Program latency.	5.00	5.00	5.00	ms, Max
T_{POR} (2)	Power-on reset (50 ms ramp rate time).	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time).	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width.	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)					
T_{ICCK}	Master CCLK output delay.	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency.	100.00	100.00	100.00	MHz, Max
	Master CCLK frequency for AES encrypted x16. (2)	50.00	50.00	50.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%, Max
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time.	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency.	100.00	100.00	100.00	MHz, Max
EMCCLK Input (Master Mode)					
T_{EMCCKL}	External master CCLK Low time.	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time.	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency.	100.00	100.00	100.00	MHz, Max
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency.	100.00	100.00	100.00	MHz, Max
Master/Slave Serial Mode Programming Switching					
T_{DCCK}/ T_{CCKD}	D_{IN} setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{CCO}	D_{OUT} clock to out.	8.00	8.00	8.00	ns, Max
SelectMAP Mode Programming Switching					
T_{SMDCCK}/ T_{SMCCKD}	D[31:00] setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)